

HM624100 Series

Preliminary

1,048,576-Word x 4-Bit High Speed CMOS Static Ram

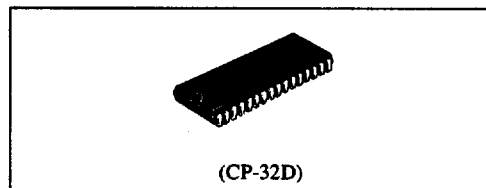
T-46-23-10

■ FEATURES

- High Speed:
Fast access time 25/30/35/45 ns(max.) (P-version)
30/35/45 ns(max.) (LP-version)
- Completely static memory
No clock or timing strobe required
- Equal access and cycle time
- TTL compatible—All inputs and outputs
- Thin plastic package for high density mounting

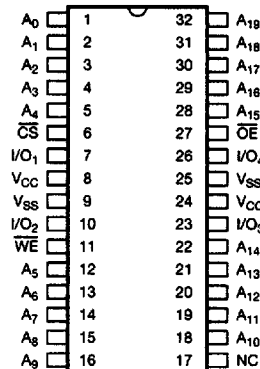
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM624100JP-25	25 ns	400 mil 32-pin SOJ (CP-32D)
HM624100JP-30	30 ns	
HM624100JP-35	35 ns	
HM624100JP-40	45 ns	
HM624100JLP-30	30ns	32-pin TSOP (II)
HM624100JLP-35	35ns	
HM624100JLP-45	45ns	
HM624100P-25	25ns	
HM624100P-30	30ns	32-pin TSOP (II)
HM624100P-35	35ns	
HM624100P-45	45ns	
HM624100LP-30	30ns	
HM624100LP-35	35ns	32-pin TSOP (II)
HM624100LP-45	45ns	



■ PIN ARRANGEMENT

HM624100 Series



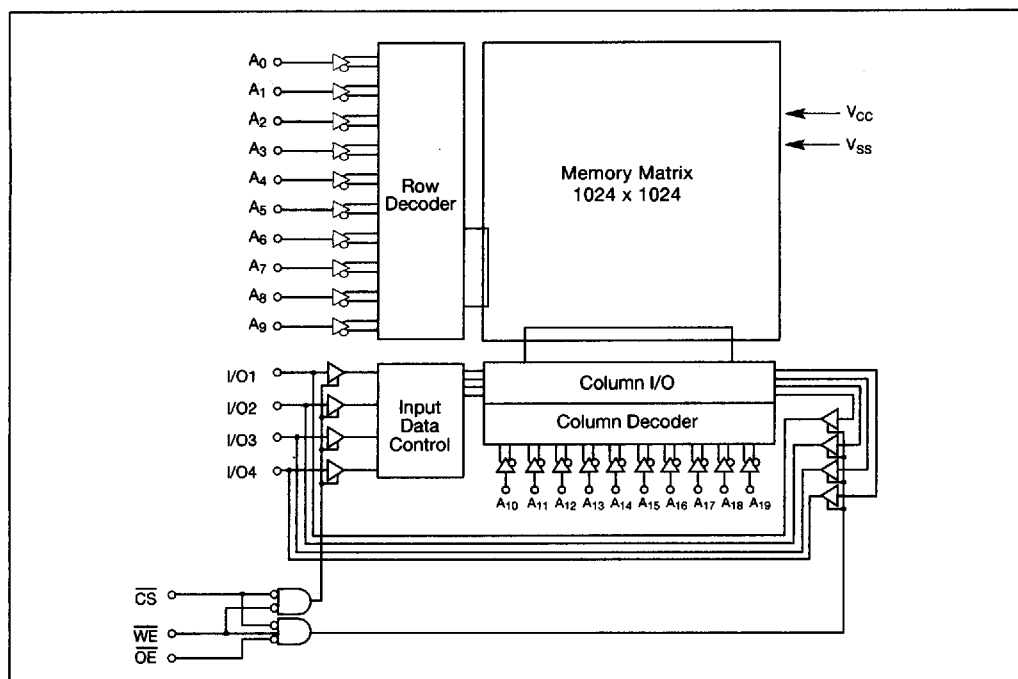
■ PIN DESCRIPTION

Pin Name	Function
A0-A19	Address Input
I/O1-I/O4	Data Input/Output
CS	Chip Select
WE	Write Enable
OE	Output Enable
VCC	Power Supply
VSS	Ground
NC	No Connection



T-46-23-1C

■ BLOCK DIAGRAM



■ FUNCTION TABLE

CS	OE	WE	Mode	VCC Current	I/O Pin	Ref. Cycle
H	X	X	Deselect	ISB, ISB1	High-Z	—
L	L	H	Read	ICC	Dout	Read Cycle 1, 2, 3
L	H	L	Write	ICC	Din	Write Cycle 1
L	L	L	Write	ICC	Din	Write Cycle 2

Note: X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to VSS	VT	-0.5 ¹ to +7.0	V
Power Dissipation	PT	1.0	W
Operating Temperature	T _{opr}	0 to +70	°C
Storage Temperature	T _{stg}	-55 to +125	°C
Storage Temperature Under Bias	T _{bias}	-10 to +85	°C

Note: 1. VT min = -2.0 V for pulse width ≤ 10 ns.



■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
	VSS	0	0	0	V
Input High Voltage	V _{IH}	2.2	—	6.0	V
Input Low Voltage	V _{IL}	-0.5 ¹	—	0.8	V

Note: 1. V_{IL} min = -2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, VCC = 5V ± 10%, VSS = 0V)

Item	Symbol	HM624100P			HM624100LP			Unit	Test Conditions
		Min.	Typ	Max.	Min.	Typ	Max.		
Input Leakage Current	I _{LI}	—	—	2.0	—	—	2.0	μA	VCC = Max., V _{in} = VSS to VCC
Output Leakage Current	I _{LO}	—	—	2.0	—	—	2.0	μA	$\overline{\text{CS}} = \text{V}_{\text{IH}}$ V _{I/O} = VSS to VCC
Operating VCC Current	I _{CC}	—	—	150	—	—	140	mA	$\overline{\text{CS}} = \text{V}_{\text{IL}}$, I _{I/O} = 0 mA, Cycle = 25 ns. (P), 35 ns. (LP)
Standby VCC Current	I _{SB}	—	—	60	—	—	5	mA	$\overline{\text{CS}} = \text{V}_{\text{IH}}$ Cycle = 25 ns. (P), 35 ns. (LP)
	I _{SB1}	—	—	10	—	—	0.1	mA	$\overline{\text{CS}} \geq \text{VCC} - 0.2\text{V}$ $0\text{V} \leq \text{V}_{\text{in}} \leq 0.2\text{V}$ or $\text{V}_{\text{in}} \geq \text{VCC} - 0.2\text{V}$
Output Low Voltage	V _{OL}	—	—	0.4	—	—	0.4	V	I _{OL} = 8mA
	V _{OH}	2.4	—	—	2.4	—	—	V	I _{OH} = -4mA

■ CAPACITANCE ($T_a = 25^\circ\text{C}$, f = 1 MHz)

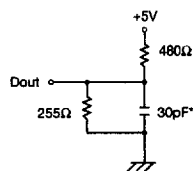
Item	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C _{in}	—	5	pF	V _{in} = 0 V
Output Capacitance	C _{I/O}	—	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, VCC = 5V ± 10%, unless otherwise noted.)

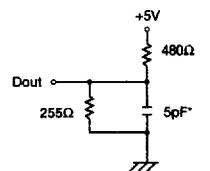
Test Conditions

- Input pulse levels: VSS to 3.0 V
- Input rise and fall times: 4 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See Figures



Output Load (A)

* Including scope & jig.



Output Load (B)

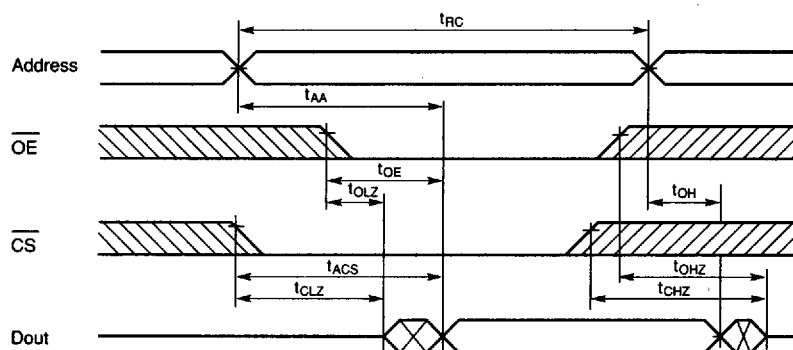
(for t_{CHZ}, t_{CLZ}, t_{WHZ} & t_{OW})



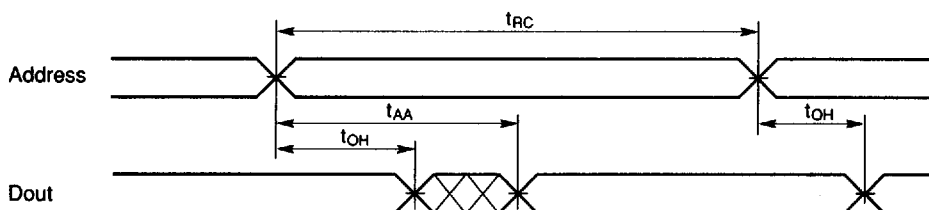
■ READ CYCLE

Item	Symbol	HM624100-25 P		HM624100-30 P/LP		HM624100-35 P/L		HM624100-45 P/LP		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25	—	30	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	30	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	—	35	—	45	ns
Chip Selection to Output in Low-Z	t_{CLZ}^1	5	—	5	—	5	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	10	—	13	—	15	—	20	ns
Output Enable to Output in Low-Z	t_{OLZ}^1	0	—	0	—	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}^1	0	10	0	10	0	15	0	15	ns
Chip Disable to Output in High-Z	t_{OHZ}^1	0	10	0	10	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	30	—	20	ns

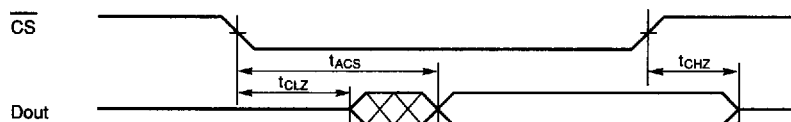
■ READ TIMING WAVEFORM (1) 1, 2



■ READ TIMING WAVEFORM (2) 2, 3, 5



■ READ TIMING WAVEFORM (3) 1, 2, 4, 5



- Notes:
1. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled not 100% tested.
 2. $\overline{WE}$ is high for read cycle.
 3. $\overline{CS}$ is low.
 4. Address valid prior to or coincident with $\overline{CS}$ transition low.
 5. $OE = V_{IL}$.

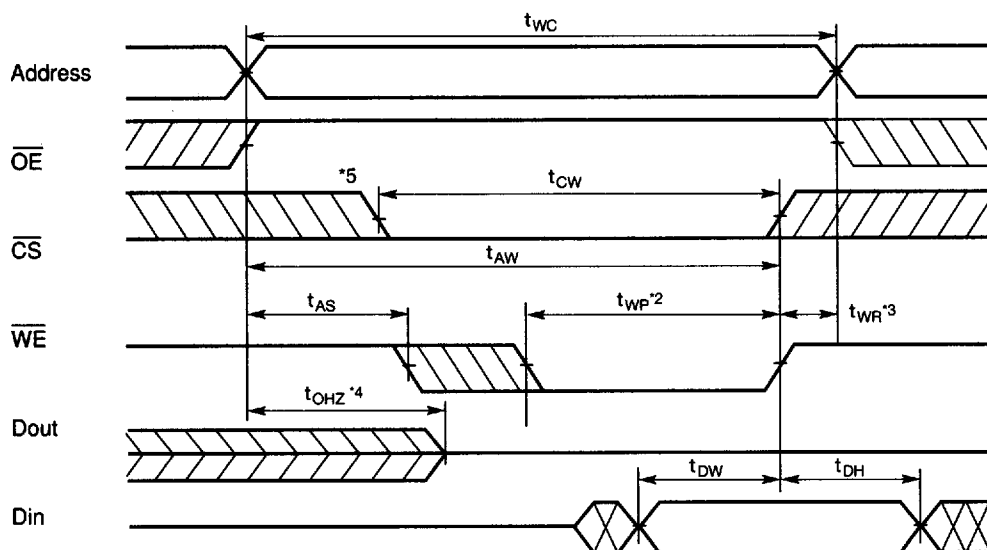


■ WRITE CYCLE

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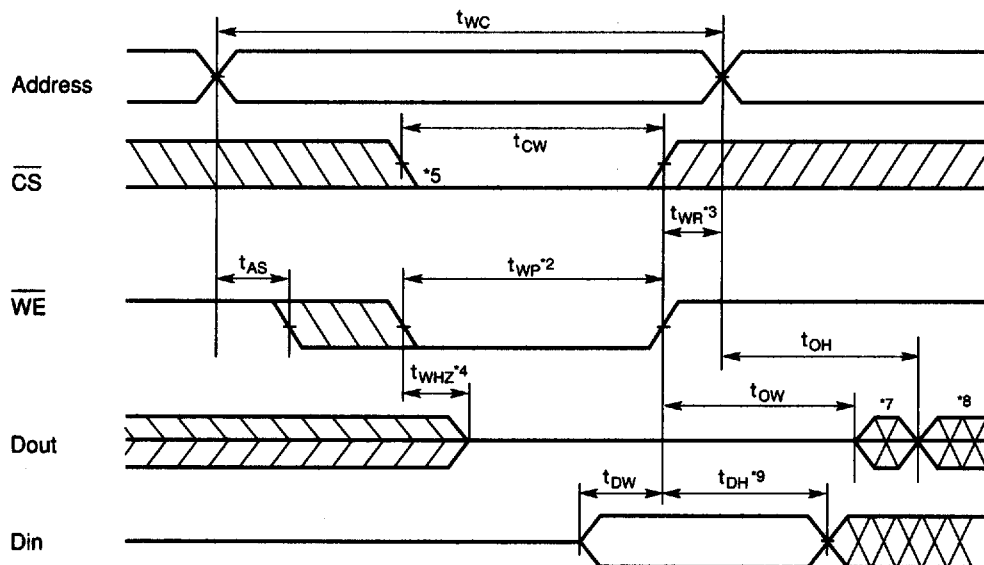
Parameter	Symbol	HM624100-25 P		HM624100-30 P/LP		HM624100-35 P/L		HM624100-45 P/LP		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25	—	30	—	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	15	—	20	—	25	—	35	—	ns
Address Valid to End of Write	t_{AW}	15	—	20	—	25	—	35	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	15	—	20	—	25	—	35	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	0	—	ns
Output Disable to Output in High-Z	t_{OHZ}	0	10	0	10	0	15	0	15	ns
Write to Output in High-Z ¹	t_{WHZ}	0	10	0	10	0	15	0	15	ns
Data to Write Time Overlap	t_{DW}	12	—	15	—	20	—	30	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	0	—	ns

■ WRITE TIMING WAVEFORM (1)



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WRITE TIMING WAVEFORM (2) ⁶



- Notes:
1. Transition is measured ± 200 mV from high impedance voltage with Load (B). This parameter is sampled not 100% tested.
 2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
 3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
 4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
 5. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain a high impedance state.
 6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
 7. Dout is the same phase of write data of this write cycle.
 8. Dout is the read data of next address.
 9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied.



■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$)

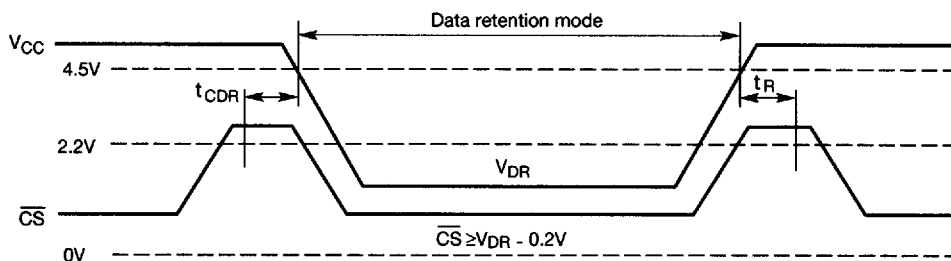
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This characteristic is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Condition
VCC for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2\text{V}$, $V_{in} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq V_{in} \leq 0.2\text{V}$
Data Retention Current	I_{CCDR}	—	—	100 ¹	μA	
Chip Select to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

Note: $V_{CC} = 3.0\text{V}$.

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM



2

