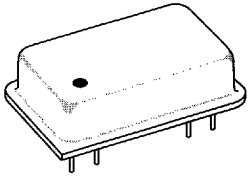
HC1360

466.667 MHz Digital Clock

- *Quartz Frequency Stability*
- *Excellent Jitter and Symmetry Performance*
- *Rugged, Hermetic Metal DIP Case*

The HC1360 digital clock is designed for use with high speed CPUs operating at 93.3334, 116.6668, 155.5557 or 233.3335 MHz. The 466.667 MHz fundamental oscillation mode, made possible by surface acoustic wave (SAW) technology, provides low jitter, compact size, and low power consumption. The differential outputs are capable of driving CMOS, 100K ECL, ECLinPS™ and other logic families.



DIP14S-8 Case (pin-out B)

ABSOLUTE MAXIMUM RATINGS

Rating		Value	Units
Power Supply Voltage (Pin 1 to Case Ground)		0 to +8	VDC
Input Voltage (ENABLE, Pin 14)		0 to V_{CC}	VDC
Output Current (CLOCK, Pin 7 or CLOCK, Pin 8)		50	mA
Case Temperature	Powered	0 to +70	°C
	Storage	-40 to +85	

ELECTRICAL CHARACTERISTICS

Characteristic		Sym	Notes	Minimum	Typical	Maximum	Units
Output Frequency	Absolute Frequency	F_O	1	466.5737	—	466.7603	MHz
	Relative to 466.667 MHz	ΔF_O		—	—	±200	ppm
Output (Enabled)	Output HIGH Voltage	V_{OH}	2	+3.98	—	+4.28	V
	Output LOW Voltage	V_{OL}		+3.05	—	+3.39	V
	Rise or Fall Time (20-80%)	t_r or t_f		—	343	—	ps
	Symmetry		3	45	—	55	%
	Period or Delay Jitter (rms)		4	—	1	—	ps
Output (Disabled)	Amplitude		5	—	70	150	mV_{P-P}
ENABLE Characteristics	Input HIGH Voltage	V_{IH}	2,5	+3.83	—	+4.28	V
	Input LOW Voltage	V_{IL}		+3.05	—	+3.53	V
	Input HIGH Current	I_{IH}		—	—	150	µA
	Input LOW Current	I_{IL}		0.5	—	—	µA
	Propagation Delay	t_{pd}	6	—	—	20	ns
DC Power Supply	Operating Voltage	V_{CC}	1,2	+4.75	+5	+5.25	VDC
	Operating Current	I_{CC}		—	85	110	mA
Operating Ambient Temperature		T_A	1	0	—	+70	°C

Lid Symbolization (YY = year, WW = week number)	RFM HC1360 466.667 MHz YYWW

1. Unless noted otherwise, all specifications apply with CLOCK and CLOCK terminated in 50 Ω to +3.0 VDC per the specified test fixture for any combination of V_{CC} and T_A within the specified operating ranges.
2. Input/output voltage limits apply only for V_{CC} = 5.00 ±0.01 VDC. Additional V_{CC} variation (within specification) must be added to these limits.
3. Symmetry is defined as the pulse width (in percent of total period) measured at the 50% points of CLOCK and CLOCK.
4. Applies to delay jitter between CLOCK and CLOCK after 20 cycles and to period jitter of CLOCK or CLOCK. Measurements are made with the Tektronix CSA803 communications signal analyzer with at least 1000 samples. Jitter induced by electrical noise on the V_{CC} input or mechanical vibration is not included. Dedicated external voltage regulation and careful PCB layout are recommended for minimum jitter.
5. The output is disabled (with CLOCK at logic HIGH) for ENABLE at logic HIGH and enabled for ENABLE at logic LOW or unterminated.
6. Propagation delay is defined as the time from the 50% point of ENABLE to the 50% point of the leading edge of the first pulse or the trailing edge of the last pulse. The minimum width of the first or last pulse is not specified.
7. The design, manufacturing process, and specifications of this device are subject to change without notice.
8. One or more of the following U. S. patents apply: 4,616,197, 4,670,681, and 4,760,352.
9. ECLinPS™ is a trademark of Motorola, Inc. RFM® is a registered trademark of RF Monolithics, Inc.
10. CAUTION: ELECTROSTATIC SENSITIVE DEVICE. Observe precautions for handling.