FM24C08 FRAM® Serial Memory

Product Preview

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Features

- 8Kbit Nonvolatile Ferroelectric RAM Organized as 1,024 x 8
- Very Low Power CMOS Technology
  - 100µA Active (Read or Write)
  - 10µA Standby Over Commercial Temperature Range
- Reliable Thin Film Ferroelectric Technology
  - 10 Billion (10^{10}) Cycle Read/Write Endurance
  - 10 Year Data Retention
- High Performance
  - No Write Delay
  - 1Kbyte Sequential Write
- Two Wire I²C Serial Interface
  - 100KHz and 400KHz Modes
  - Replacement for Xicor X24C08
- True 5V Only Operation
- 8-Pin Mini DIP and SOIC Packages
- -40° to +85°C Operating Range

Description

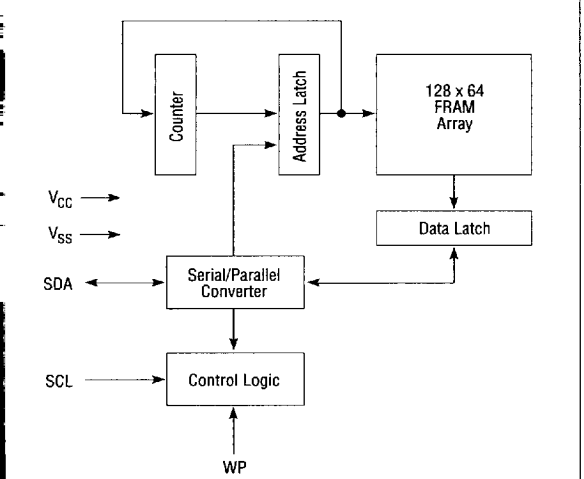
Ramtron's FM24C08 ferroelectric random access memory, or FRAM® memory provides nonvolatile data integrity in a compact package. A two wire serial interface provides access to any byte within the memory while reducing the cost of the processor interface. The FM24C08 is useful in a wide variety of applications for the storage of configuration information, user programmable data/features, and calibration data.

With Ramtron's ferroelectric technology, all writes are nonvolatile, eliminating long delays, extra page mode control, or high voltage pins. The technology is designed for highly reliable operation, offering extended endurance and 10 year data retention.

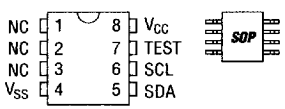
The FM24C08 is not recommended for use in systems that contain more than one I²C EEPROM device.

The part uses the industry standard two wire protocol for serial chip communication and is pin compatible with a number of parts from other vendors. It is available in 300 mil mini-DIP and 150 mil SOP packages.

Functional Diagram



Pin Configurations



Pin Names

Pin Names	Function
SDA	Serial Data/Address
SCL	Serial Clock
TEST	Connect to V_{SS}
V_{SS}	Ground
V_{CC}	Supply Voltage

This document describes a product under development. Ramtron reserves the right to change or discontinue this product without notice.

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Absolute Maximum Ratings

Description	Ratings
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	-40°C to +85°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V
D.C. Output Current	5mA
Lead Temperature (Soldering, 10 Seconds)	300°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Operating Conditions

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Unless Otherwise Specified

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	V_{CC} Supply Current		60	100	µA	SCL @ 100KHz, Read or Write SCL CMOS Levels, All Other Inputs = V_{SS} or V_{CC} - 0.3V
I_{CC}	V_{CC} Supply Current		180	300	µA	SCL @ 400KHz, Read or Write SCL CMOS Levels, All Other Inputs = V_{SS} or V_{CC} - 0.3V
I_{SB}(2)	Standby Current 0 to 70°C		8	25	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC}
I_{SB}(2)	Standby Current -40 to 85°C		16	60	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}	Input Low Voltage	-1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage			0.4	V	I_{OL} = 3mA
V_{OL2}	Output Low Voltage			0.6	V	I_{OL} = 6mA
V_{HYS}(3)	Input Hysteresis	V_{CC} x .05			V	

(1) Typical values are measured at 25°C, 5.0V.
(2) Must perform a stop command prior to measurement.
(3) This parameter is periodically sampled and not 100% tested.

Endurance and Data Retention

Parameter	Min	Max	Units
Endurance	10 Billion		R/W Cycles
Data Retention	10		Years

Power-Up Timing (4)

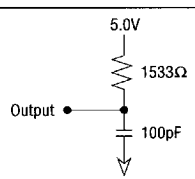
Symbol	Parameter	Max	Units
t_{PUR}(4)	Power Up to Read Operation	1	µs
t_{PUW}(4)	Power Up to Write Operation	1	µs

(4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

AC Conditions of Test

AC Conditions	Test
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

Equivalent AC Load Circuit



Capacitance

T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Test	Max	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (SCL, WP)	6	pF	V_{IN} = 0V

(3) This parameter is periodically sampled and not 100% tested.

Pin Descriptions

SCL — Serial Clock

When high, the SCL clocks data into and out of the FM24C08. It is an input only. This input is built with a Schmitt trigger to provide increased noise immunity.

SDA — Serial Data Address

This bi-directional pin is used to transfer addresses to the FM24C08 and data to or from the FM24C08. It is an open drain output and intended to be wire-ORed with all other devices on the serial bus using an external pull-up resistor. The input circuitry on this pin is built with a Schmitt trigger to reduce noise sensitivity. The output section incorporates slope control for the falling edges.

Test

This input is used for testing during manufacturing of the part. It is to be tied to V_{SS} in all systems.

Bus Protocol

The FM24C08 employs a bi-directional two wire bus protocol requiring a minimum of processor I/O pins. Figure 1 shows a typical system configuration connecting a microcontroller with an FM24C08 and another I²C bus slave. The FM24C08 is not recommended for use in systems in which other bus slaves are EEPROM, regardless of their density.

By convention, any device sending data onto the bus is the transmitter, while the device that is getting the data is the receiver. The device controlling the bus is the master and provides the clock signal for all operations. Devices being controlled are the slaves. The FM24C08 is always a slave device.

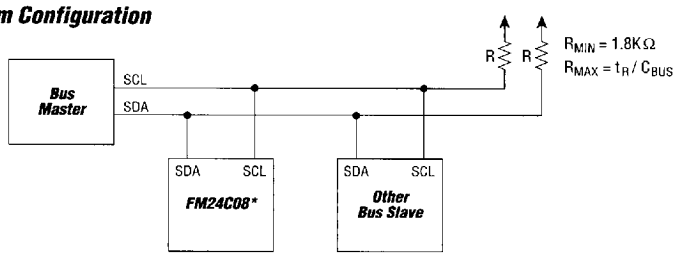
Transitions or states on the SDA and SCL lines denote one of four conditions: a *start, stop, data bit,* or *acknowledge*. Figure 2 shows the signaling for these conditions, while the following four sections describe their function.

Figure 3 shows the detailed timing specifications for the bus. Note that all SCL specifications and the *start* and *stop* specifications apply to both read and write operations. They are shown on one or the other for clarity. Also, the write timing specifications apply to all transmissions to the FM24C08, including the slave and word address, as well as write data sent to the FM24C08 from the bus master.

Start Condition

A *start* condition is indicated to the FM24C08 when there is a high to low transition of SDA while SCL is high. All commands to the FM24C08 must be preceded by a *start*. In addition, a *start* condition occurring at any point within an operation will abort that operation and ready the FM24C08 to start a new one.

Figure 1. Typical System Configuration



*Only one 24C08 is allowed on a single I²C bus.

Figure 2. Data Transfer Protocol

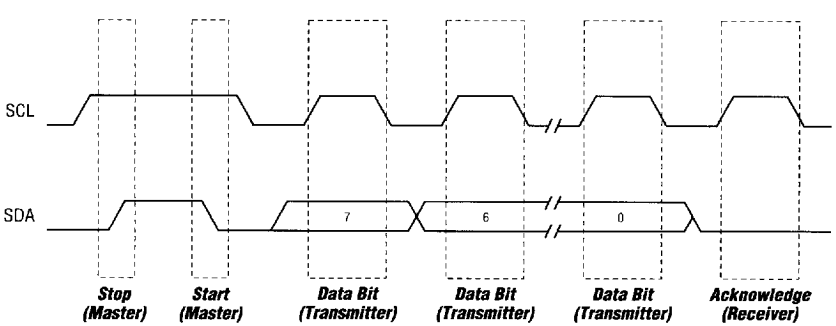
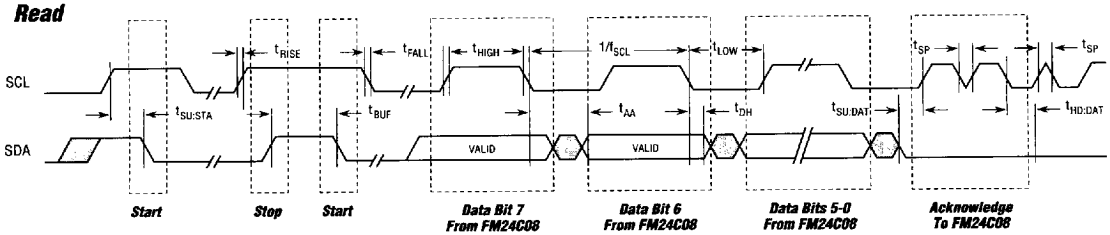
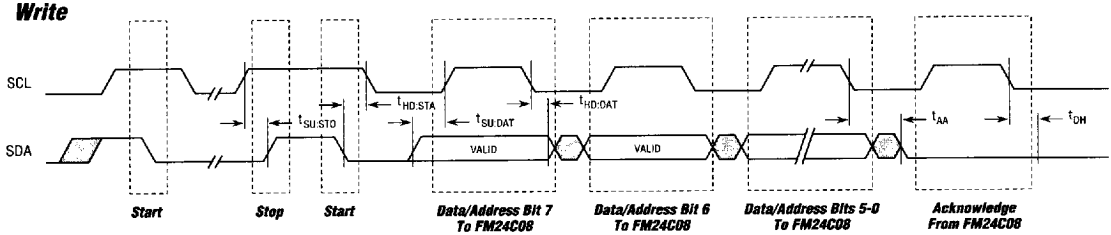


Figure 3. Bus Timing

Read



Write



Notes:

All start and stop timings apply to both read and write cycles identically.

Clock specifications are the same for both read and write.

Write timing specifications apply to slave address, word address, and write data.

These timing diagrams provide representative timing relationships of the signals. They are not intended to provide functional relationships between the signals. These are provided in Figures 5 through 9.

Read and Write Cycle AC Parameters

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Unless Otherwise Specified

Symbol	Parameter	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	KHz
t_{SP}	Noise Suppression Time Constant at SCL, SDA Inputs		50		50	ns
t_{AA}	SCL Low to SDA Data Out Valid		3		0.9	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.3		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_{RISE} (3)	SDA and SCL Rise Time		1000	20+0.1C_b (5)	300	ns
t_{FALL} (3)	SDA and SCL Fall Time		300	20+0.1C_b (5)	300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.0		0.6		µs
t_{DH}	Data Out Hold Time (From SCL @ V_{IL})	0		0		ns
t_{OF}	Output Fall Time (V_{IH} Min to V_{IL} Max)		250	20+0.1C_b (3)	250	ns

(3) This parameter is periodically sampled and not 100% tested.

(5) C_b = Total Capacitance of One Bus Line in pF

Stop Condition

A *stop* condition is indicated to the FM24C08 when there is a low to high transition of SDA while SCL is high. All operations to the FM24C08 should end with a *stop*. In addition, any operation will be aborted at any point when this condition occurs.

Data/Address Transfers

Data/address transfers take place during the period when SCL is high. Except under the two conditions described above, the state of the SDA line may not change while SCL is high. Address transfers are always sent to the FM24C08, while data transfers may either be sent to the FM24C08 (for a write) or to the bus master (for a read).

Acknowledge

Acknowledge transfers take place on the ninth clock cycle after each eight-bit address or data transfer. During this clock cycle, the transmitter will release the SDA bus to allow the receiver to drive the bus low to acknowledge receipt of the byte.

If the receiver does not acknowledge any byte, the operation is aborted.

Device Operation

Low Voltage Protection

When powering up, the FM24C08 will automatically perform an internal reset and await a *start* signal from the bus master. The bus master should wait T_{PUR} (or T_{PLW}) after V_{CC} reaches 4.5V before issuing the *start* for the first read or write access. Additionally, whenever V_{CC} falls below 3.5V (typical), the part goes into its low voltage protection mode. In this mode, all accesses to the part are inhibited and the part performs an internal reset. If an access was in progress when the power supply fails, it will be automatically aborted by the FM24C08. When power rises back above 4.5V, a *start* signal must be issued by the bus master to initiate an access.

Slave Address

Following a *start*, the FM24C08 will expect a slave address byte to appear on the bus. This byte consists of four parts as shown in Figure 4.

- Bits 7 through 4 are the device type identifier which must be binary 1010 as shown.
- Bit 3 is the device select bit. The FM24C08 will perform an access regardless of the state of A2, however, for proper operation it must be set to 0. *Ramtron cannot guarantee the results of reads or writes that take place with this bit set to 1.*
- Bits 1 and 2 are the page select bits. They select which 256-byte block of memory will be accessed by this operation.
- Bit 0 is the read/write bit. If set to a 1, a read operation is being performed by the master; otherwise, a write is intended.

Word Address

After a slave device *acknowledges* the slave address on a write operation, the master will place the word address on the bus. This byte, in addition to the two page select bits from the slave address byte, forms the address of the byte within the memory that is to be written. This 10-bit value is latched in the internal address latch. There is no word address specified during a read operation, although the upper two bits of the internal latch are set to the page select values in the slave address.

During the transmission of each data byte and before the acknowledge cycle, the address in the internal latch is incremented to allow the following byte to be accessed immediately. When the last byte in the memory is accessed (at address hex 3FF), the address is not reset to 0, therefore, a new write block must be started at address 0. There is no alignment requirement for the first byte of a block cycle — any address may be specified. There is also no limit to the number of bytes that may be accessed in a single read or write operation.

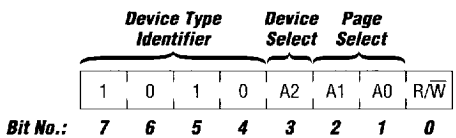
Data Transfer

After all address bytes have been transmitted, data will be transferred between the FM24C08 and the bus master. In the case of a read, the FM24C08 will place each of the eight bits on the bus and then wait for an acknowledge from the bus master before performing a read on the subsequent address. For a write operation, the FM24C08 will accept eight bits from the bus master and then drive the acknowledge on the bus.

All data and address bytes are transmitted most significant bit (bit 7) first.

After the acknowledge of a data byte transfer, the bus master may either begin another read or write on the subsequent byte, issue a *stop* command to terminate the block operation, or issue a *start* command to terminate the current operation and start a new one.

Figure 4. Slave Address



Write Operations

All write operations start with a slave and word address transmission to the FM24C08. In the slave address, bit 0 should be set to a 0 to denote a write operation. After they are acknowledged, the bus master transmits each data byte(s) to the FM24C08. After each byte, the FM24C08 will generate an acknowledge signal. Any number of bytes may be written in a single write sequence. After the last byte in the memory (address hex 3FF) is written, the address counter does not wrap around to zero.

There is no write delay on the FM24C08. Any operation, either a read or write to some other address, may immediately follow a write. Acknowledge polling, a sequence used with EEPROM devices to let the bus master know when a write cycle is complete, will return done immediately (the FM24C08 will acknowledge the first correct slave address).

If a write cycle must be aborted (with a *start* or *stop* condition), this should take place *before* the transmission of the eighth bit in order that the memory not be altered.

Figure 5. Byte Write

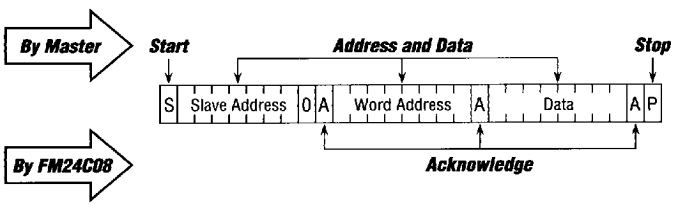
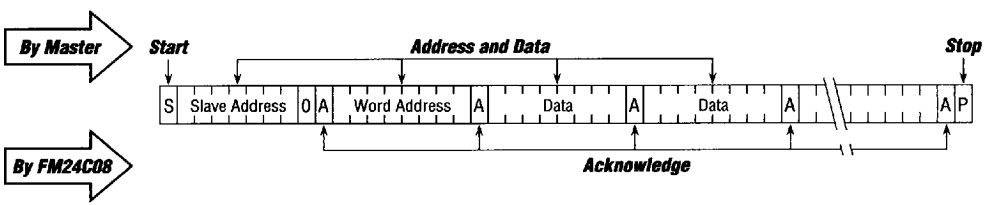


Figure 6. Multiple Byte Write



Read Operations

Current Address or Sequential Read

Sequential read operations take place from the address currently held in the internal address latch, and so require only that the bus master provide a slave address transfer before the FM24C08 begins the transfer of data to the master. In this slave address, bit 0 should be set to a 1 to denote a read operation. Note that the most significant two bits of the 10-bit internal address latch are specified by the slave address word, and are therefore *always* set during a read, regardless of which page the previous access referenced.

One or multiple bytes may be read from the FM24C16 in a single read operation. In a multi-byte read, each acknowledge from the bus master indicates to the slave that another byte is being requested.

The read operation must be properly terminated after the final 8-bit byte has been read. The bus master can end the read sequence in one of four ways:

(1) The first and recommended way is for the bus master to issue a no acknowledge in the ninth clock cycle and a stop in the tenth clock cycle. This is shown in Figures 7 through 9.
(2) The second method is for the bus master to issue a no acknowledge in the ninth clock cycle and a start in the tenth clock cycle.
(3) The bus master issues a stop in the ninth clock cycle.
(4) The bus master issues a start in the ninth clock cycle.

After the last byte in the memory (address hex 3FF) is read, the address counter does not wrap around to zero. These sequences are shown below in Figures 7 and 8.

Selective (Random) Read

Selective, or random, read operations are possible on the FM24C08 by using the first two bytes of the *write* operation to load the internal address. The slave address for the part is sent out with bit 0 ($R/\overline{W}$) set to 0 to denote a write operation, and the word address is set to specify the least significant 8 bits of the desired address.

After the FM24C08 acknowledges this word address, the bus master should abort the *write* and begin the read with a *start* command. A new slave address is then sent out, this time with the $R/\overline{W}$ bit set to 1. Following the slave address and acknowledge, the FM24C08 will immediately begin transmission of the requested data. Figure 9 shows this operation.

Figure 7. Current Address Read

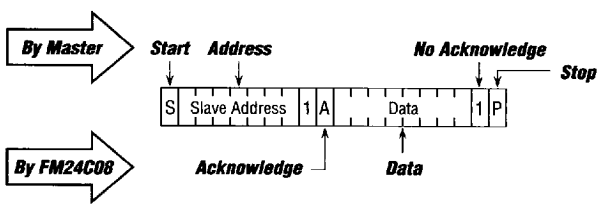


Figure 8. Sequential Read

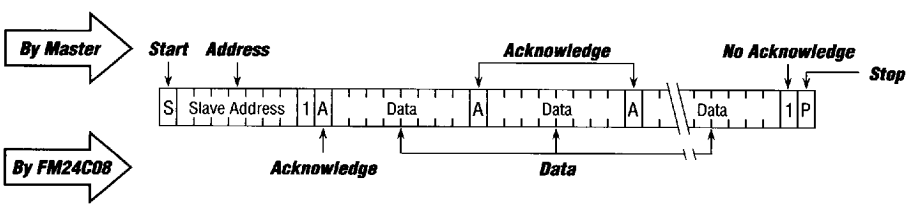
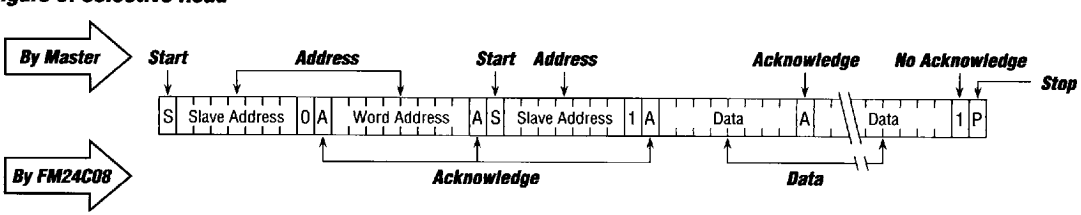
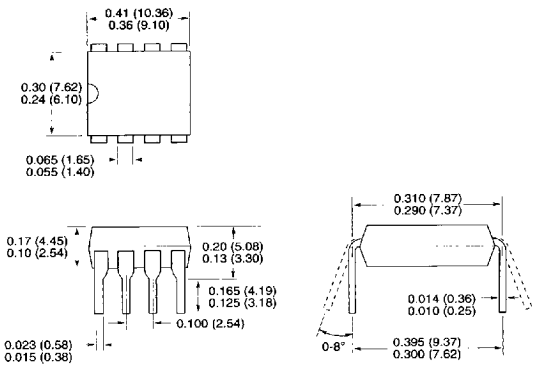


Figure 9. Selective Read

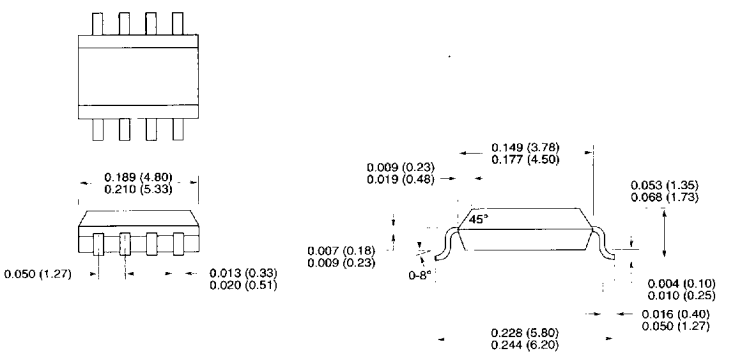


Packaging Information

8-Pin Plastic or Ceramic DIP



8-Pin SO (JEDEC)



Ordering Information