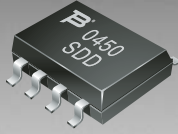


*RoHS COMPLIANT



BOURNS®

Features

- Lead free device (RoHS compliant*)
- Protects up to 4 I/O ports
- Bidirectional configuration
- ESD protection
- Low capacitance 6 pF

Applications

- Ethernet – 10/100/1000 Base T
- Personal digital assistant
- Handheld electronics
- Cellular phones
- Video cards

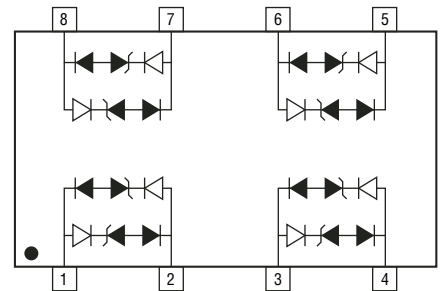
CDNBS08-SLVU2.8-8 – Low Capacitance TVS Array

General Information

The markets of portable communications, computing and video equipment are challenging the semiconductor industry to develop increasingly smaller electronic components.

Bourns offers Transient Voltage Suppressor Array combination diodes for surge and ESD protection applications in an 8 Lead Narrow Body SOIC package size format. Bourns Chip Diodes conform to JEDEC standards, are easy to handle on standard pick and place equipment and their flat configuration minimizes roll away.

The Bourns® device will meet IEC 61000-4-2 (ESD), IEC 61000-4-4 (EFT) and IEC 61000-4-5 (Surge) requirements.



Electrical Characteristics (@ T_A = 25 °C Unless Otherwise Noted)

| Parameter | Symbol | Min. | Nom. | Max. | Unit |
|--|--------------------------|----------------|------|------|------|
| Peak Pulse Current (t _p = 8/20 μs) | I _{PP} | | 30 | | A |
| Peak Pulse Power (t _p = 8/20 μs) ¹ | P _{PP} | | 600 | | W |
| Working Voltage | V _{WM} | | | 2.8 | V |
| Breakdown Voltage @ 1 mA | V _{BR} | 3.0 | | | V |
| Leakage Current @ V _{WM} | I _D | | | 1.0 | μA |
| Capacitance @ 0 V, 1 MHz | C | | 6 | | pF |
| Snapback Voltage | | 2.8 | | | V |
| Clamping Voltage | @ I _{PP} = 2 A | V _C | | 5.5 | V |
| | @ I _{PP} = 5 A | V _C | | 8.5 | V |
| | @ I _{PP} = 24 A | V _C | | 15 | V |
| | @ I _{PP} = 30 A | V _C | | 17 | V |

Note:

1. See Peak Pulse Power vs. Pulse Time.

Thermal Characteristics (@ T_A = 25 °C Unless Otherwise Noted)

| Parameter | Symbol | Min. | Nom. | Max. | Unit |
|-----------------------|------------------|------|------|------|------|
| Operating Temperature | T _J | -55 | +25 | +150 | °C |
| Storage Temperature | T _{STG} | -55 | +25 | +150 | °C |

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex.
 Specifications are subject to change without notice.
 Customers should verify actual device performance in their specific applications.

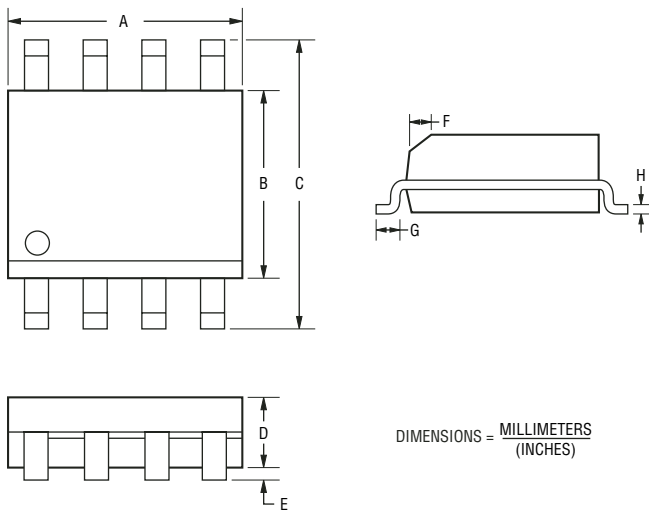
CDNBS08-SLVU2.8-8 – Low Capacitance TVS Array



Mechanical Characteristics

This is a molded JEDEC Narrow Body SO-8 package with lead free 100 % Sn plating on the lead frame. It weighs approximately 15 mg and has a flammability rating of UL 94V-0.

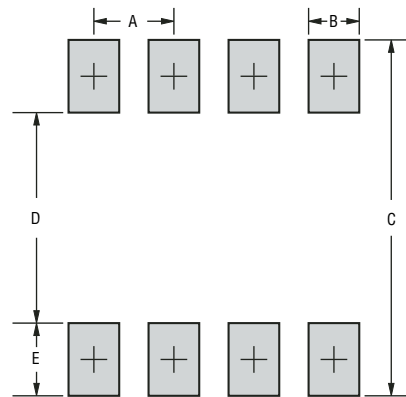
Product Dimensions



DIMENSIONS = MILLIMETERS
(INCHES)

| Dimensions | |
|------------|--|
| A | $\frac{4.80 - 5.00}{(0.189 - 0.196)}$ |
| B | $\frac{3.80 - 4.00}{(0.150 - 0.157)}$ |
| C | $\frac{5.80 - 6.20}{(0.229 - 0.244)}$ |
| D | $\frac{1.35 - 1.75}{(0.054 - 0.068)}$ |
| E | $\frac{0.10 - 0.25}{(0.004 - 0.008)}$ |
| F | $\frac{0.25 - 0.50}{(0.010 - 0.019)}$ |
| G | $\frac{0.40 - 1.250}{(0.016 - 0.049)}$ |
| H | $\frac{0.18 - 0.25}{(0.007 - 0.009)}$ |

Recommended Footprint



| Dimensions | |
|------------|---|
| A | $\frac{1.143 - 1.397}{(0.045 - 0.055)}$ |
| B | $\frac{0.635 - 0.889}{(0.025 - 0.035)}$ |
| C | $\frac{6.223}{(0.245)}$ Min. |
| D | $\frac{3.937 - 4.191}{(0.155 - 0.165)}$ |
| E | $\frac{1.016 - 1.27}{(0.040 - 0.050)}$ |

How To Order

Common Code CD NBS08 - SLVU 2.8 - 8
 CD = Chip Diode
 Package NBS08 = Narrow Body SOIC8 Package
 Model SLVU = Low Capacitance TVS Array
 Working Peak Reverse Voltage 2.8 = 2.8 V_{RM} (Volts)
 Number of Diodes 8

Typical Part Marking

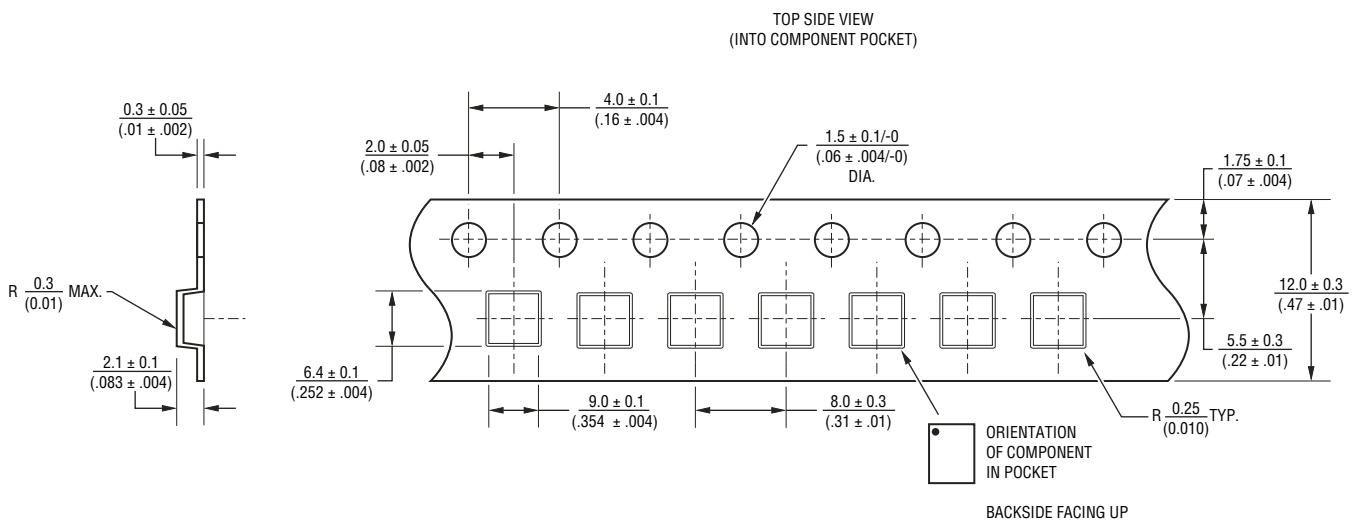
CDNBS08-SLVU2.8-8 **SL8**

CDNBS08-SLVU2.8-8 – Low Capacitance TVS Array

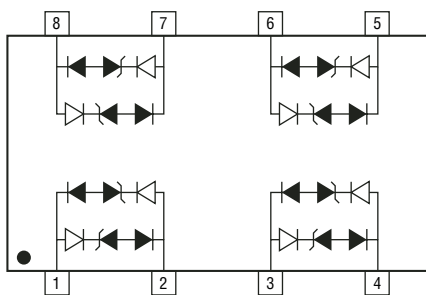


Packaging

The surface mount product is packaged in a 8 mm x 4 mm Tape and Reel format per EIA-481 standard.



Block Diagram

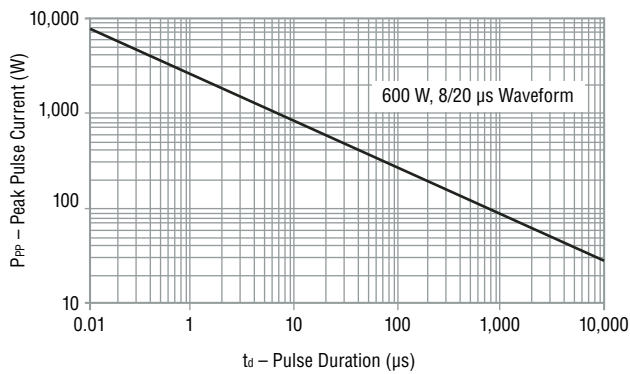


Device Pinout

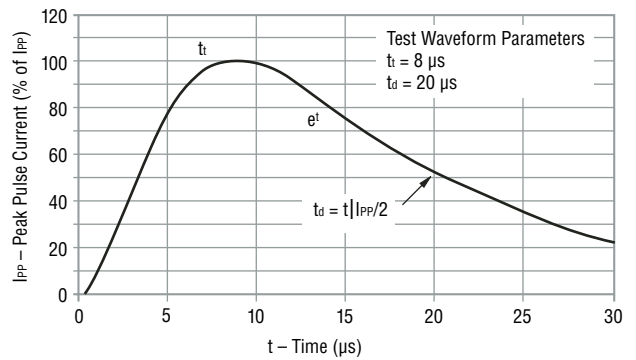
| Pin | Bidirectional Common Mode | Bidirectional Differential Mode |
|-----|---------------------------|---------------------------------|
| 1 | Line 1 | Line Pair 1 |
| 2 | GND | Line Pair 1 |
| 3 | GND | Line Pair 2 |
| 4 | Line 4 | Line Pair 2 |
| 5 | Line 3 | Line Pair 4 |
| 6 | GND | Line Pair 4 |
| 7 | GND | Line Pair 3 |
| 8 | Line 2 | Line Pair 3 |

Performance Graphs

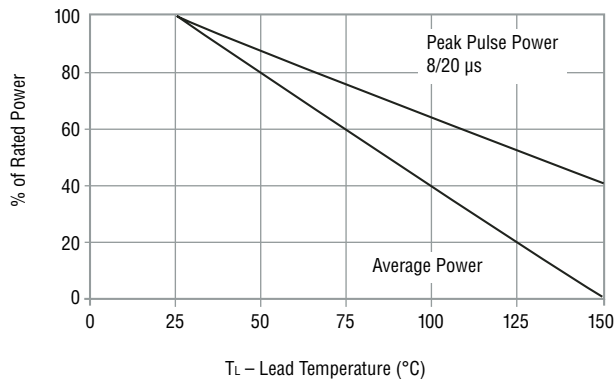
Peak Pulse Power vs Pulse Time



Pulse Wave Form



Power Derating Curve



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