REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
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SHEET	15	16																	

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-12-04

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 16K X 4 SRAM WITH SEPARATE I/O AND TRANSPARENT WRITE, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90594
A	67268	

SHEET 1 OF 16

DESC FORM 193
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5962-E496

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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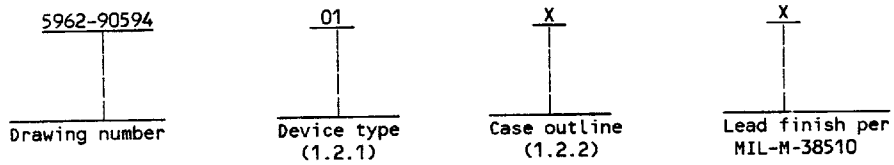
1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		16K x 4 SRAM separate I/O and transparent write	45 ns
02		16K x 4 SRAM separate I/O and transparent write	35 ns
03		16K x 4 SRAM separate I/O and transparent write	25 ns
04		16K x 4 SRAM separate I/O and transparent write	20 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Descriptive designator	Terminals	Package Style
X	CDIP3-T28 or GDIP4-T28	28	dual-in-line
Y	GDFP2-F28	28	flat pack
Z	CQCC4-N28	28	rectangular leadless chip carrier
U	CQCC3-N28	28	rectangular leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage range applied to outputs in High Z state	-0.5 V dc to +7.0 V dc
DC Input voltage range (V_{IN}) 2/	-0.5 V dc to +7.0 V dc
DC output current	20 mA
Maximum power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X, Y, and Z	See MIL-STD-1835
Junction temperature (T_J) 3/	+150°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND) (V_{SS})	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.
2/ V_{IL} minimum = -3.0 V for pulse width less than 20 ns.
3/ Maximum junction temperature may be increased to 175°C during burn-in and steady state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification and standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMDs).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All		0.4	V
Input high voltage	V_{IH} 3/		1, 2, 3	All	2.2		V
Input low voltage	V_{IL} 3/		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-10	10	µA
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, $\overline{CE} = V_{IL}$, I_{OUT} = 0 mA, f = f_{MAX} 4/	1, 2, 3	01,02		140	mA
				03		155	
				04		175	
Standby power supply current TTL	I_{CC2}	V_{CC} = 5.5 V, $\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, I_{OUT} = 0 mA, f = 0 4/	1, 2, 3	01,02		50	mA
				03		60	
				04		70	
Standby power supply current CMOS	I_{CC3}	$\overline{CE} \ge (V_{CC} - 0.2\ V)$, all other inputs ≤ 0.2 V or $\ge (V_{CC} - 0.2\ V)$, V_{CC} = 5.5 V, f = 0 4/	1, 2, 3	01-03		20	mA
				04		25	
Input capacitance	C_{IN} 5/	V_{CC} = 5.0 V, V_{IN} = 0 V T_A = 25°C, f = 1 MHz (see 4.3.1c)	4	All		8	pF
Output capacitance	C_{OUT} 5/	V_{CC} = 5.0 V, V_{OUT} = 0 V T_A = 25°C, f = 1 MHz (see 4.3.1c)	4	All		8	pF
Functional tests		See 4.3.1d	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Read cycle time	t_{AVAV}	See figures 3 and 4	9, 10, 11	01	45		ns
				02	35		
				03	25		
				04	20		
Address access time	t_{AVQV}		9, 10, 11	01		45	ns
				02		35	
				03		25	
				04		20	
Output hold from address change	t_{AVQX}		9, 10, 11	All	5		ns
Chip enable access time	t_{ELQV}		9, 10, 11	01		45	ns
				02		35	
				03		25	
				04		20	
Chip enable to 5/ 6/ output active	t_{ELQX}		9, 10, 11	All	5		ns
Chip select to 5/ 6/ output inactive	t_{EHQZ}		9, 10, 11	01,02		15	ns
				03		10	
				04		8	
Output enable to output valid	t_{OLQV}		9, 10, 11	01		25	ns
				02		20	
				03		12	
				04		10	
Output enable to 5/ 6/ output active	t_{OLQX}		9, 10, 11	All	3		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output enable to 5/ 6/ output inactive	t_{OHQZ}	See figures 3 and 4	9, 10, 11	01,02		15	ns
				03		10	
				04		8	
Chip enable to 5/ power up	t_{ELPU}		9, 10, 11	All	0		ns
Chip enable to 5/ power down	t_{EHPD}		9, 10, 11	01		45	ns
				02		35	
				03		25	
				04		20	
Write cycle time	t_{AVAV}		9, 10, 11	01	40		ns
				02	30		
				03	20		
				04	20		
Chip enable to write end	t_{ELWH} t_{ELEH}		9, 10, 11	01	35		ns
				02	25		
				03	20		
				04	17		
Address set-up to end of write	t_{AVWH} t_{AVEH}		9, 10, 11	01	35		ns
				02	25		
				03	20		
				04	17		
Address hold from write end	t_{WHAX} t_{EHAX}		9, 10, 11	All	0		ns
Address set-up to write start	t_{AVWL} t_{AVEL}		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Write enable pulse width	t_{WLWH} t_{WLEH}	See figures 3 and 4	9, 10, 11	01	35		ns
				02	25		
				03	20		
				04	17		
Data set-up to write end	t_{DVWH} t_{DVEH}		9, 10, 11	01	20		ns
				02	15		
				03	13		
				04	10		
Data hold from write end	t_{WHDX} t_{EHDX}		9, 10, 11	All	0		ns
Write enable low 5/ to output valid	t_{WLQV}		9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
Data valid to 5/ output valid	t_{DVQV}		9, 10, 11	01		35	ns
				02		30	
				03,04		20	

1/ AC tests are performed with transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3, circuit A.

2/ Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in table I.

3/ These are absolute values with respect to device ground and all overshoots and undershoots due to system or tester noise are included.

4/ At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency of $1/t_{AVAV}$.

5/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

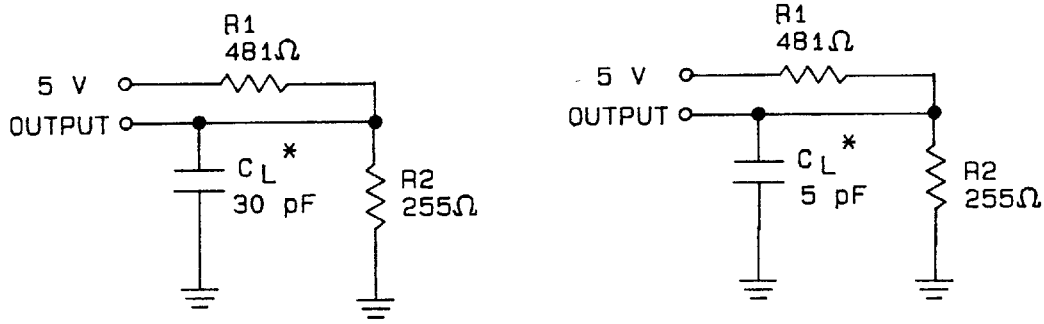
6/ Transition is measured at steady state high level -500 mV or steady state low level +500 mV on the output from the 1.5 V level on the input, C_L = 5 pF (including scope and jig). See figure 3, circuit B.

Device types	All
Case outlines	X, Y, Z, and U
Terminal number	Terminal symbol
1	A
2	A
3	A
4	A
5	A
6	A
7	A
8	A
9	A
10	I_0
11	I_1
12	$\overline{CE}_1$
13	$\overline{OE}$
14	GND
15	$\overline{CE}_2$
16	$\overline{WE}$
17	O_0
18	O_1
19	O_2
20	O_3
21	I_2
22	I_3
23	A
24	A
25	A
26	A
27	A
28	V_{CC}

FIGURE 1. Terminal connections.

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Mode	D_{OUT}	Power
H	X	X	X	Not selected	High Z	Standby
X	H	X	X	Not selected	High Z	Standby
L	L	L	L	Write	D_{OUT}	Active
L	L	L	H	Write	High Z	Active
L	L	H	L	Read	D_{OUT}	Active
L	L	H	H	Output disable	High Z	Active

FIGURE 2. Truth table.



Circuit A
Output load

Circuit B
Output load

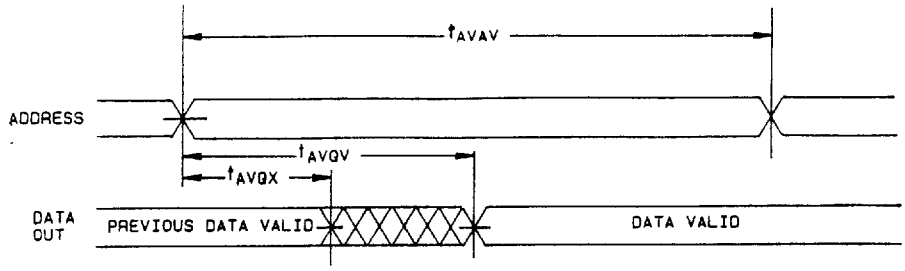
*Including scope and jig. (minimum values)

AC test conditions

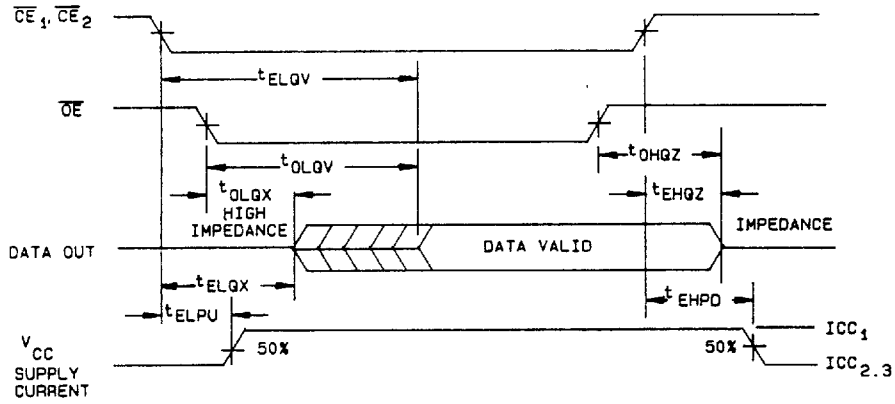
Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and test conditions.

Read cycle number 1



Read cycle number 2



Write cycle number 1 ($\overline{WE}$ controlled)

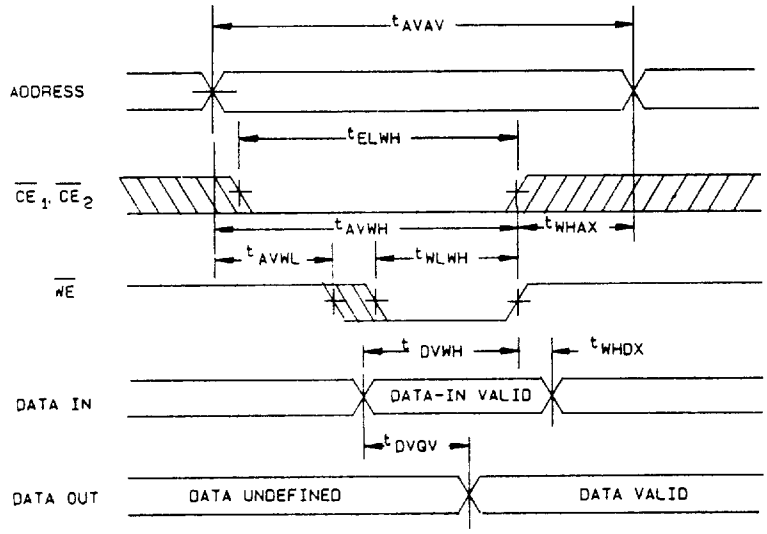


Figure 4. Timing waveforms.

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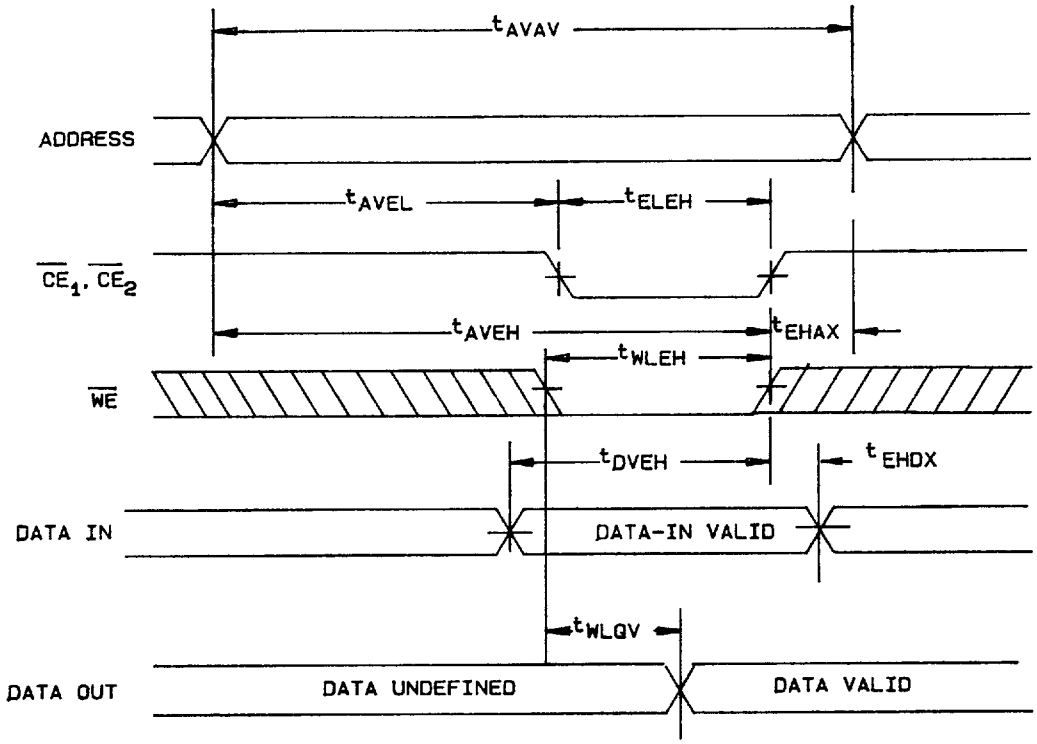
Write cycle number 2 ($\overline{CE}$ controlled)



Notes on read operation:
1. WE is high for read cycles.
2. For read cycle number 1, device is continously selected, $\overline{CE}_1$, $\overline{CE}_2$, $\overline{OE}$ = V_{IL}.
3. For read cycle number 2, addresses are valid prior to or coincident with $\overline{CE}_1$ and or $\overline{CE}_2$ transition low.

Notes on write operation:
1. WE or $\overline{CE}_1$ or $\overline{CE}_2$ must be high during address transitions.
2. A write occurs during the overlap of $\overline{CE}_1$ and $\overline{CE}_2$ low and $\overline{WE}$ low. All signals must be low to initiate a write and any signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

FIGURE 4. Timing waveforms - Continued.

3.2.4 Functional tests. Various functional tests used to test this device are contained in appendix A. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-M-38510) shall be subjected to and pass the internal moisture content test at 5000 ppm (method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (See 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8A, 8B,9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7***, (8A,8B)***, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

* PDA applies to subgroups 1 and 7.
** For subgroup see 4.3.1c.
*** For subgroups 7, 8A, and 8B, see 4.3.1d.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after any process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroup 7 and 8A, 8B tests shall be sufficient to verify the truth tables.

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. Procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. JEDEC Standard No. 17 may be used as a guideline when performing O/V testing.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions; method 1005 of MIL-STD-883:

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMDs. All proposed changes to existing SMDs will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for, each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.2.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.

Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.