MOS INTEGRATED CIRCUIT
µPD9388A

Y/C SEPARATION AND
MOTION DETECTION LSI FOR EDTV

The µPD9388A is the LSI for Y/C separation and motion detection for EDTV. Using a built-in optimum filter, the LSI separates luminance and color signals (Y/C-signals) from a composite video signal converted into digital data by an 8-bit high-speed A/D converter, in accordance with the state of a screen. It also incorporates motion detectors to check the screen state. These allow the LSI to implement Y/C-signal separation for EDTV independently as a signal processing LSI.

In combination with other three LSIs (YCP II, YCI II, and TIG II), this LSI makes up an EDTV signal processing system.

The µPD9388A includes improved motion detector on µPD9380. ,
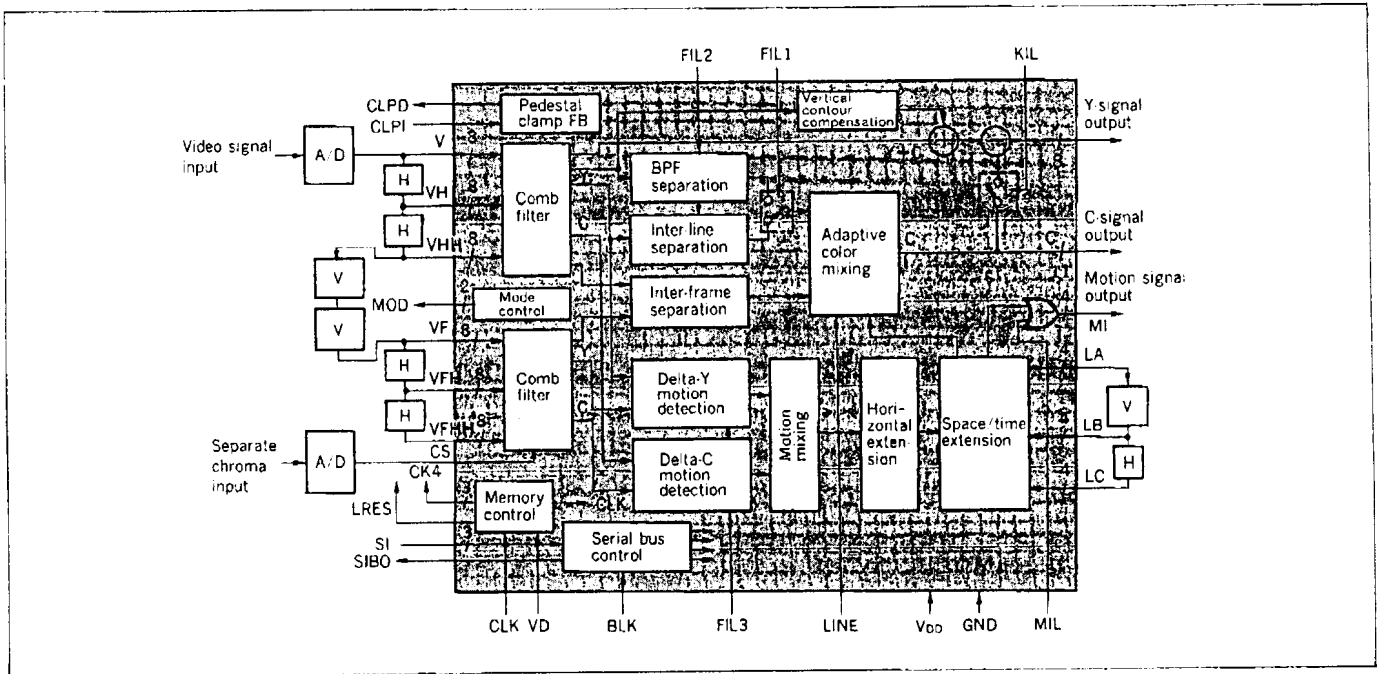
FEATURES:

- Y/C separation and motion detection functions built in a single chip
- Optimum Y/C separation filter selected according to the screen state: inter-frame Y/C separation, inter-line Y/C separation, and frequency separation filters
- Capable of S-terminal input
- Built-in circuit for vertical contour compensation
- One-frame difference detection (color/luminance signal difference detection) by motion detectors
- Built-in circuits for motion signal extension in the horizontal, vertical, and time-base directions
- Built-in function for floating the external memories
- Setting data under serial bus control
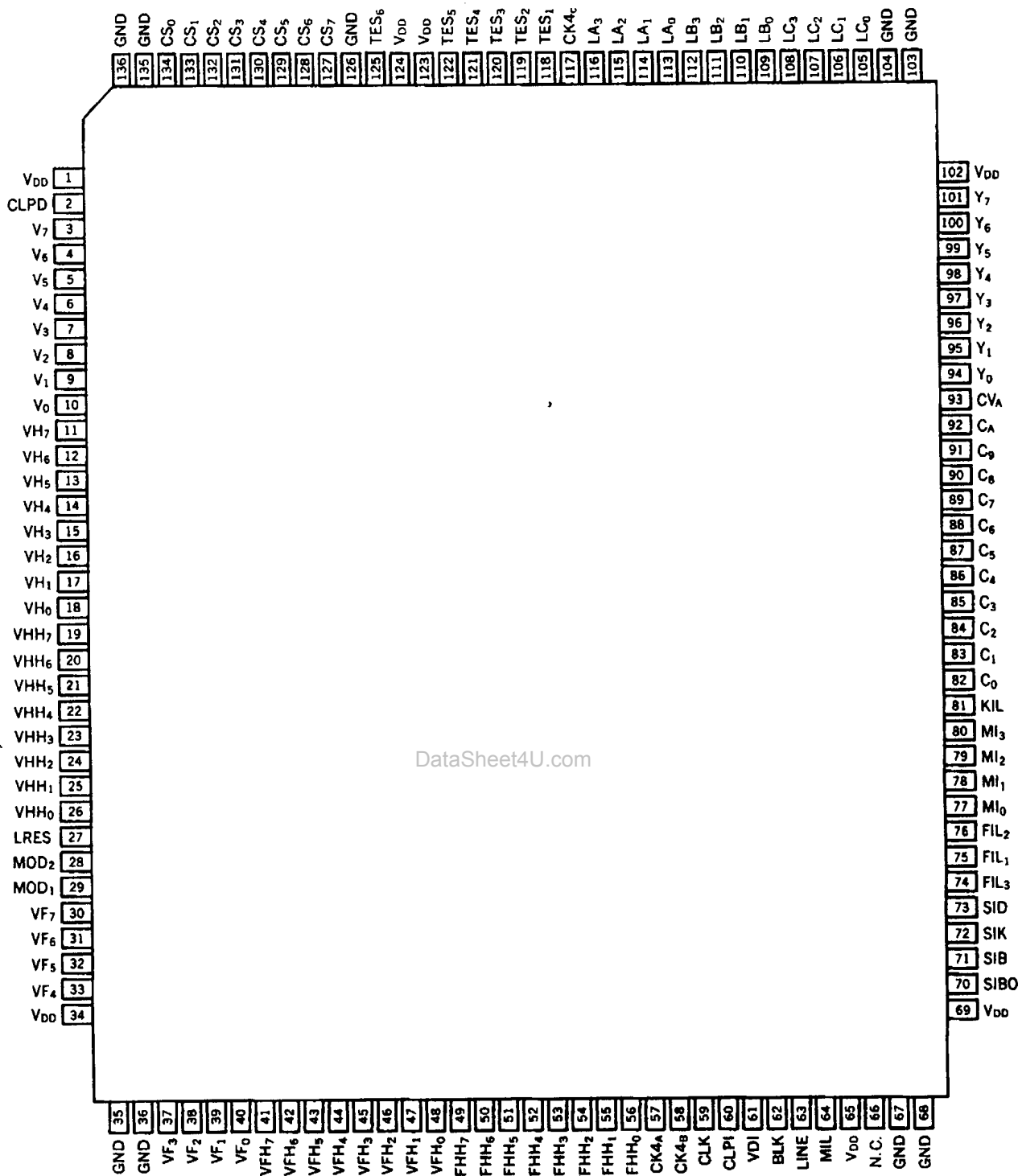- Single 5 V power supply
- CMOS process

BLOCK DIAGRAM

FIL2 FIL1   KIL

CLPD
CLPI

Video signal input — A/D — V — Pedestal clamp FB

Vertical contour compensation — Y signal output

H — VH

Comb filter — BPF separation

H — VHH

Inter-line separation — Adaptive color mixing — C signal output

V — MOD — Mode control

Inter-frame separation — Motion signal output — MI

V — VF

Comb filter — Delta-Y motion detection — Motion mixing — Horizontal extension — Space/time extension — LA

H — VFH

LB — V

H — VFHH

Delta-C motion detection — LC — H

Separate chroma input — A/D — CS
CK4

LRES

Memory control

SI
SIBO — Serial bus control

CLK VD   BLK   FIL3   LINE   Vdd   GND   MIL

ORDERING INFORMATION

ORDER NAME	PACKAGE	QUALITY GRADE
μPD9388AGD-5BC	136-pin plastic QFP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.
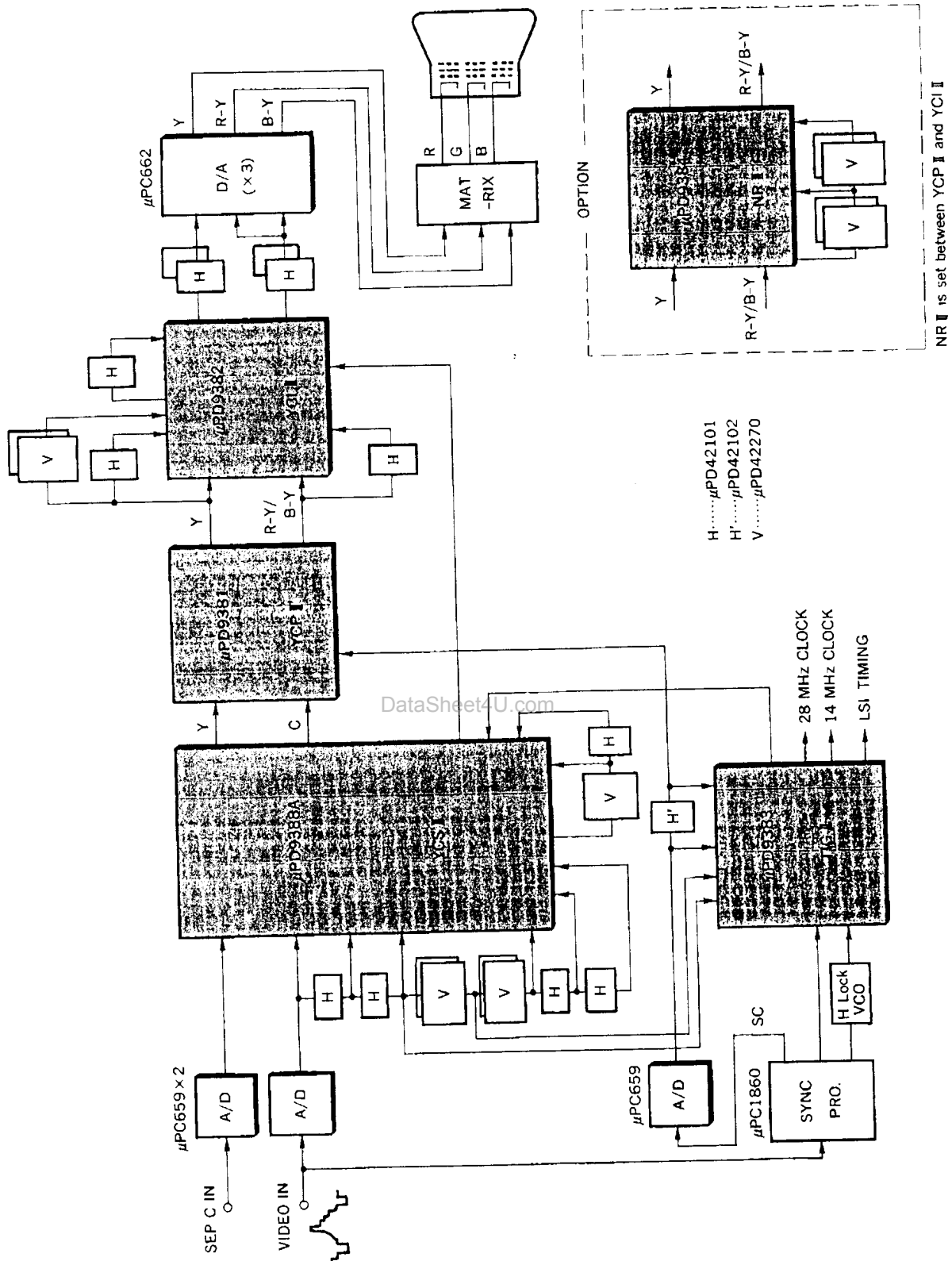
PIN CONNECTION DIAGRAM (Top View)

Top side pins (136 down to 103):
GND 136, GND 135, CS$_0$ 134, CS$_1$ 133, CS$_2$ 132, CS$_3$ 131, CS$_4$ 130, CS$_5$ 129, CS$_6$ 128, CS$_7$ 127, GND 126, TES$_6$ 125, V$_{DD}$ 124, V$_{DD}$ 123, TES$_5$ 122, TES$_4$ 121, TES$_3$ 120, TES$_2$ 119, TES$_1$ 118, CK4$_c$ 117, LA$_3$ 116, LA$_2$ 115, LA$_1$ 114, LA$_0$ 113, LB$_3$ 112, LB$_2$ 111, LB$_1$ 110, LB$_0$ 109, LC$_3$ 108, LC$_2$ 107, LC$_1$ 106, LC$_0$ 105, GND 104, GND 103

Left side pins (1 to 34):
V$_{DD}$ 1
CLPD 2
V$_7$ 3
V$_6$ 4
V$_5$ 5
V$_4$ 6
V$_3$ 7
V$_2$ 8
V$_1$ 9
V$_0$ 10
VH$_7$ 11
VH$_6$ 12
VH$_5$ 13
VH$_4$ 14
VH$_3$ 15
VH$_2$ 16
VH$_1$ 17
VH$_0$ 18
VHH$_7$ 19
VHH$_6$ 20
VHH$_5$ 21
VHH$_4$ 22
VHH$_3$ 23
VHH$_2$ 24
VHH$_1$ 25
VHH$_0$ 26
LRES 27
MOD$_2$ 28
MOD$_1$ 29
VF$_7$ 30
VF$_6$ 31
VF$_5$ 32
VF$_4$ 33
V$_{DD}$ 34

Right side pins (102 down to 69):
102 V$_{DD}$
101 Y$_7$
100 Y$_6$
99 Y$_5$
98 Y$_4$
97 Y$_3$
96 Y$_2$
95 Y$_1$
94 Y$_0$
93 CV$_A$
92 C$_A$
91 C$_9$
90 C$_8$
89 C$_7$
88 C$_6$
87 C$_5$
86 C$_4$
85 C$_3$
84 C$_2$
83 C$_1$
82 C$_0$
81 KIL
80 MI$_3$
79 MI$_2$
78 MI$_1$
77 MI$_0$
76 FIL$_2$
75 FIL$_1$
74 FIL$_3$
73 SID
72 SIK
71 SIB
70 SIBO
69 V$_{DD}$

Bottom side pins (35 to 68):
GND 35, GND 36, VF$_3$ 37, VF$_2$ 38, VF$_1$ 39, VF$_0$ 40, VFH$_7$ 41, VFH$_6$ 42, VFH$_5$ 43, VFH$_4$ 44, VFH$_3$ 45, VFH$_2$ 46, VFH$_1$ 47, VFH$_0$ 48, VFHH$_7$ 49, VFHH$_6$ 50, VFHH$_5$ 51, VFHH$_4$ 52, VFHH$_3$ 53, VFHH$_2$ 54, VFHH$_1$ 55, VFHH$_0$ 56, CK4$_A$ 57, CK4$_B$ 58, CLK 59, CLPI 60, VDI 61, BLK 62, LINE 63, MIL 64, V$_{DD}$ 65, N.C. 66, GND 67, GND 68

CONFIGURATION OF LSI SYSTEM FOR EDTV

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power-supply Voltage	V_{DD}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{DD} + 0.5	V
Output Current	I_{OUT}	20	mA
Power Dissipation	P_D	920 (T_a = 60 °C)	mW
Operating Temperature	T_{opt}	−20 to +60	°C
Storage Temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING RANGE (T_a = −20 °C to +60 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power-supply Voltage	V_{DD}	4.5	5.0	5.25	V	
Input Low Voltage	V_{IL}	0		0.3 V_{DD}	V	CMOS input pin
Input High Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Input Low Voltage	V_{IL}	0		0.8	V	TTL input pin
Input High Voltage	V_{IH}	2.4		V_{DD}	V	
Input Low Voltage	V_{IL}	0.6		3.1	V	
Input High Voltage	V_{IH}	1.8		4.0	V	Schmitt input pin
Hysteresis Voltage	V_H	0.3		1.5	V	
Clock Frequency	F_{CLK}		14.3		MHz	

ELECTRICAL SPECIFICATIONS (V_{DD} = 4.5 to 5.25 V, T_a = −20 °C to +60 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power-supply Current	I_{DD}		95		mA	No signal input
Output Low Current 1	I_{OL1}	6.0	13.0		V	Pins CK4$_A$, B, and C V_{OL} = 0.4 V
Output Low Current 2	I_{OL2}	3.0	6.5		V	Pins other than CK4$_A$, B, and C V_{OL} = 0.4 V
Output High Current 1	$-I_{OH1}$	3.2	7.0		V	Pins CK4$_A$, B, and C V_{OH} = V_{DD} − 0.4 V
Output High Current 2	$-I_{OH2}$	1.6	3.5		V	Pins other than CK4$_A$, B and C V_{OH} = V_{DD} − 0.4 V
Input Current 1	$\pm I_{I1}$		10^{-5}	10	μA	CMOS and TTL input pins V_{IN} = V_{DD} or GND
Input Current 2	$\pm I_{I2}$	40	100	270	μA	Pin with pull-down resistor V_{IN} = V_{DD}
Output Delay Time	T_d	5	19	40	ns	To CLK input *1
Input Pin Capacitance	C_{IN}		10	25	pF	f_{IN} = 1 MHz
Output Pin Capacitance	C_{OUT}		10	25	pF	f_{IN} = 1 MHz
Input/Output Pin Capacitance	C_{IO}		10	25	pF	f_{IN} = 1 MHz
Setup Time 1	t_{s1}	10			ns	To CLK input *2
Hold Time 1	t_{h1}	10			ns	To CLK input *2
Setup Time 2	t_{s2}	12			ns	To CLK input *3
Hold Time 2	t_{h2}	4			ns	To CLK input *3

*1 The data output is specified with falling-edge or rising-edge of input clock.

*2 The pins except CLPI, VDI, BLK, LINE

*3 The pins of CLPI, VDI, BLK, LINE

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Timing Chart

Clock
(CLK)

t_{h1}, t_{h2} t_{s1}, t_{s2}

Data Input

T_d

Data Output

T_d

Data Output
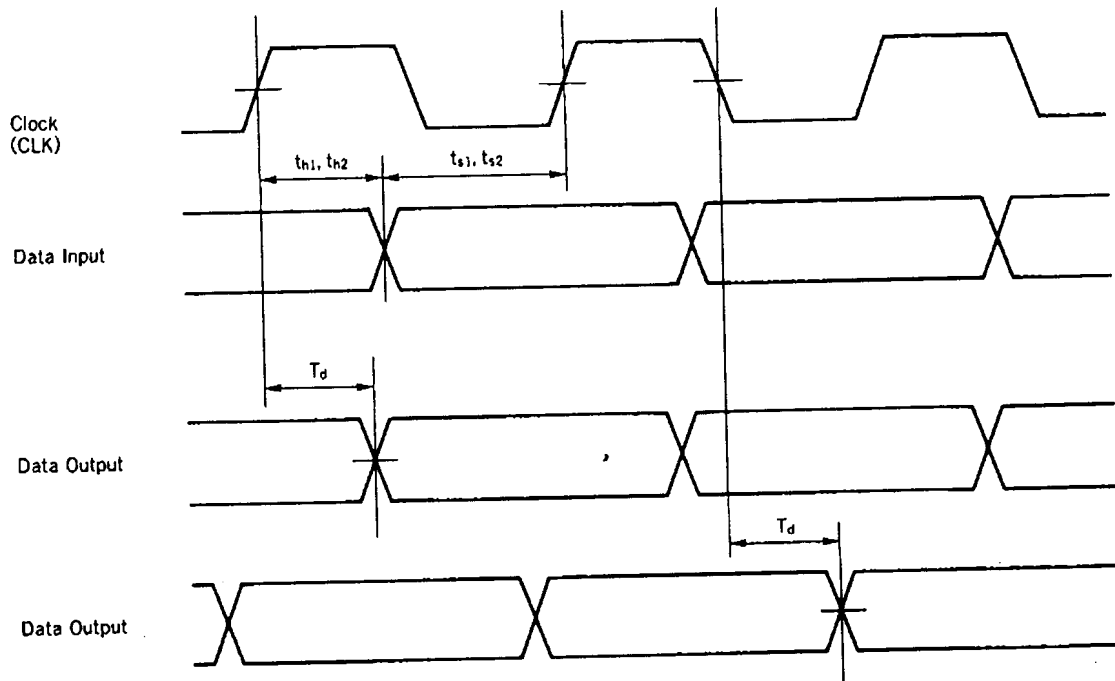
ATTENTION FOR APPLICATION

(1)   Please connect the body with the board, and radiate heat of chip.

(2)   Must be thick line wiring for the power supply, and reduce a potential difference of each V_{DD} pin.

(3)   Must be thick line wiring for Grounding, and reduce a potential difference of each GND Pin.

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PIN DESCRIPTION

PIN ABBREVIATION	PIN NAME	PIN NUMBER		FUNCTION
V_0 to V_7	Video Signal Input (0 H delay)	10 to 3	Input (TTL) ⌐_ *[SB]	This pin inputs 8-bit digital signals converted from their analog video signal. The pin inputs composite video signals in the composite video input mode or separate luminance signals in the S-terminal mode. Input signals at the pedestal level of 64. (V_0: LSB, V_7: MSB)
VH_0 to VH_7	Video Signal Input (1 H delay)	18 to 11	Input (TTL) _⌐ [SB]	This pin inputs video signals delayed by 1 H. This input serves as the center of Y/C separation. (VH_0: LSB, VH_7: MSB)
VHH_0 to VHH_7	Video Signal Input (2 H delay)	26 to 19	Input/Output (TTL), (Input) ⌐_ (Output) ⌐_ [SB]	This pin inputs video signals delay by 2 H. The pin serves as an input pin in the composite video signal input mode or an output pin in the S-terminal mode. In the S-terminal mode, the pin outputs input signals VH_0 to VH_7 added with only the burst signals among separate chroma input signals (CS_0 to CS_7). In the output mode, data is output in synchronization with the falling edge of a clock pulse. While the pin is serving for output, the line buffer connected to the pin must keep a high impedance using the MOD_2 pin. (VHH_0: LSB, VHH_7: MSB)
VF_0 to VF_7	Video Signal Input (1-frame delay)	40 to 37 33 to 30	Input (TTL) ⌐_ [SB]	This pin inputs video signals delayed by one frame (1 F = 525 H). In the S-terminal mode, the pin inputs signals delayed by 1 frame + 1 line (1 line = 1 F + 1 H = 526 H). In the S-terminal mode, the field buffer delay time must be controlled by the output from the MOD pin. (VF_0: LSB, VF_7: MSB)
VFH_0 to VFH_7	Video Signal Input (1-frame + 1 H delay)	48 to 41	Input/Output (TTL) ⌐_ [SB]	This pin inputs video signals delayed by 1 frame + 1 H (526 H). The pin serves as an input pin in the composite video signal input mode or an output pin in the S-terminal mode. In the S-terminal mode, the pin outputs separate chroma input signals (CS_0 to CS_7) without modification. In the output mode, data is output via the input buffer not in synchronization with the clock pulse. While the pin is serving for output, the line buffer connected to the pin must keep a high impedance using the MOD_2 pin. (VFH_0: LSB, VFH_7: MSB)
$VFHH_0$ to $VFHH_7$	Video Signal Input (1-frame + 2 H delay)	56 to 49	Input (TTL) ⌐_ [SB]	This pin inputs video signals delayed by 1 frame + 2 H (527 H). In the S-terminal mode, the pin inputs separate chroma signals delayed by 1 H. ($VFHH_0$: LSB, $VFHH_7$: MSB)
CS_0 to CS_7	Separate Chroma Input	134 to 127	Input (TTL) ⌐_ [SB]	This pin inputs 8-bit digital signals converted from their analog separated chroma signal such as S-terminal. Otherwise, the pin must be grounded. The gain from this input pin to the chroma output pin is 1 time (for the eight bits from MSB among 11 bits of the chroma output). (CS_0: LSB, CS_7: MSB)

*[SB] indicates that digital data is in straight binary code.

⌐ or ⌐ indicates the data input and output are specified with rising-edge or falling-edge of input clock.

PIN ABBREVIATION	PIN NAME	PIN NUMBER	FUNCTION	
Y_0 to Y_7	Luminance Output	94 to 101	Output (CMOS) [SB]	This pin outputs luminance signals that are Y/C-separated composite video signals. The composite video signals delayed by 1 H + 17 clock pulses are output from V_0 to V_7 inputs. The gain from V_0 to V_7 inputs is 1 time. The synchronizing signal is output protected by the BLK signal. (Y_0: LSB, Y_7: MSB)
C_0 to C_A	Chroma Output	82 to 92	Output (CMOS) *[2's complement]	This pin outputs luminance signals that are Y/C-separated composite video signals. The composite video signals delayed by 1 H + 17 clock pulses are output from V_0 to V_7 inputs. The gain from V_0 to V_7 inputs is 2 times, and the gain from CS_0 to CS_7 inputs is 1 time. (Each gain applies to the eight bits from MSB among 11 bits of the chroma output). (C_A: LSB, C_A: MSB)
CV_A	Chroma Inversion Output	93	Output (CMOS)	Since the output chroma signal is in 2's complement form, the MSB must be inverted to convert the signal into offset binary code. This output pin outputs the chroma signal with inverted MSB. For D/A conversion of the chroma output, the output pin CV_A is used instead of C_A.
CLPI	Clamp Pulse Input	60	Input (Schmitt with pull-down resistor)	This pin inputs a clamp pulse. The LSI contains a correction signal output circuit to automatically correct deviation in setting the pedestal level to 64. This input pin serves for clamp position sampling for input to the correction circuit. The clamp pulse to be input must be active high. Data is obtained at the fall of the clamp pulse. Ground or open the pin if it is not used.
CLPD	Clamp Error Data Output	2	Output (CMOS)	The LSI contains a correction signal output circuit to automatically correct deviation in setting the pedestal level to 64. This pin outputs error data to correct the deviation. The output data consists of four pulse-width-modulated (PWM) bits. The output pin connected with a CR filter allows error correction at initialization by feeding back the data to the analog clamping circuit placed in front of the A/D converter.
KIL	Y/C Separation Killer Input	81	Input (CMOS with pull-down resistor)	When this pin becomes high (H), the luminance output pin outputs luminance signals that are not restricted in color signal band. That is, the color signal is not eliminated from the composite video signal. Ground or open the pin when it is not being used.
MI_0 to MI_3	Y-Interpolation Motion Signal	77 to 80	Output (CMOS) [SB]	This pin outputs motion signals for Y-correction. Connect this output pin to the motion input pin of YCI II (μPD9382). (MI_0: LSB, MI_3: MSB)
MIL	Y-Interpolation Motion Signal Forcing Input	64	Input (CMOS with pull-down resistor)	This input pin forces every Y-Interpolation motion signal output (MI_0 to MI_3) to be high (H). H: MI_0 to MI_3 = all high L: MI_0 to MI_3 = standard output
LINE	Y/C Separation Motion Signal Forcing Input	63	Input (CMOS with pull-down resistor)	When this pin becomes high, it sets the Y/C separation motion signal processing mode forcedly for intra-field Y/C separation. H: Forced intra-field Y/C separation L: Adaptive operation

*[2's complement] indicates that digital data is in 2's complement code.

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PIN ABBREVIATION	PIN NAME	PIN NUMBER	FUNCTION	
MOD_1, MOD_2	Mode Selection Output	29, 28	Output (CMOS)	This output pin controls the number of lines and the degree of delay for the externally connected field or line buffer, and enables or disables the output of the buffer.
LRES	Line Buffer Reset Output	27	Output (CMOS)	This output pin resets the read/write address pointer of the externally connected line buffer. The pin detects the rising edge of the VDI input once (in frame unit) per 2 V, and it outputs the active low (L) pulses for one clock pulse in synchronization with the falling edge of the clock pulse. Use this output pin when the LSI is used independently (without the µPD9383/TIGII).
VDI	Vertical-Synchronizing Signal Input	61	Input (CMOS with pull-down resistor)	This timing input pin generates the LRES output to reset the read/write address pointer of the externally connected line buffer. Input the active low (L) vertical-synchronizing signal. When the LRES output pin is not used, ground or open this input pin.
BLK	Blank Signal Input	62	Input (CMOS with pull-down resistor)	This input pin protects the synchronizing luminance signal. When the pin becomes high (H), the internal signal processing is set for: − Frequency Y/C separation − Vertical contour compensation off − Synchronizing signal protection off
FIL_1	Filter Selection 1	75	Input (CMOS with pull-down resistor)	This input pin sets intra-field Y/C separation in the frequency separation filter mode forcedly. When the interleave detection output of the µPD9383 (TIGII) is connected to this pin, the frequency separation filter executes Y/C separation of non-interleaved signals. H: Frequency separation filter L: Line combing filter
FIL_2	Filter Selection 2	76	Input (CMOS with pull-down resistor)	This pin changes over band characteristics of the color signal pass-band for the intra-field Y/C separation filter (line combing or frequency separation type). The pin is usually used to input low signals. H: Narrow band L: Standard band
FIL_3	Filter Selection 3	74	Input (CMOS with pull-down resistor)	This pin changes over the field differential signal filter for luminance signals. In usual use, ground or open this pin.
LA_0 to LA_3	Output for Motion Extension	113 to 116	Output (CMOS) [SB]	The output pin extends motion signals. (LA_0: LSB, LA_3: MSB)
LB_0 to LB_3	Input for Motion Extension	109 to 112	Input (TTL) [SB]	This pin inputs signals from motion extension outputs (LA_0 to LA_3), that are delayed by 262 H − 2 clock pulses. (LB_0: LSB, LB_3: MSB)
LC_0 to LC_3	Input for Motion Extension	105 to 108	Input (TTL) [SB]	This pin inputs signals from motion extension outputs (LA_0 to LA_3), that are delayed by 263 H − 2 clock pulses. (LC_0: LSB, LC_3: MSB)
CLK	Clock Input	59	Input (CMOS)	This pin inputs the 4 f_{SC} clock pulse. Data in input and output at the rising edge of this clock unless specified.

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PIN ABBREVIATION	PIN NAME	PIN NUMBER		FUNCTION
CK4$_A$, CK4$_B$, CK4$_C$	Clock Output	57, 58, 117	Output (CMOS)	This pin outputs the clock input from the CLK input pin after delaying it by 10 ns (typ.). Use the clock for the A/D converter and line and field buffers connected to the LSI.
SID	Serial Bus Data Input	73	Input (CMOS) Schmitt	This pin inputs data via the serial bus.
SIK	Serial Bus Clock Input	72	Input (CMOS) Schmitt	This pin inputs the serial bus clock signal.
SIB	Serial Bus Busy Input	71	Input (CMOS) Schmitt	This pin inputs the serial bus busy signal.
SIBO	Serial Bus Busy Output	70	Output (N-CH open drain)	This pin outputs the serial bus acknowledge busy signal.
N.C	Non Connection	66		This pin is non connection.
V$_{DD}$	Power Supply	1, 34, 65, 69, 102, 123, 124		This pin supplies power to the LSI. Supply 4.5 to 5.25 V.
GND	Ground	35, 36, 67, 68, 103, 104, 126, 135, 136	,	This pin grounds the LSI.
TES$_1$, TES$_2$ TES$_3$	Test Input	118, 119 120	Input (CMOS with pull-down resistor)	This pin inputs data for test. Ground or open the pin.
TES$_4$, TES$_5$ TES$_6$	Test Output	121, 122, 125	Output (CMOS)	This pin outputs data for test.

IO

FUNCTIONS

1. Y/C SEPARATION

The μPD9388A incorporates three types of major Y/C-signal separation filters. It selects the optimum filter in accordance with an input signal.

(1) Inter-frame Y/C separation filter

This filter performs Y/C-signal separation according to the frame correlation of the NTSC (National Television System Committee) signal and the inter-frame characteristic of the signal color phase. (It is used for a static image.)

(2) Inter-line Y/C separation filter

This filter is one of the intra-field Y/C separation filters. It performs Y/C-signal separation according to the line correlation of the NTSC signal and the inter-line characteristic of the signal color phase.

(3) Frequency separation Y/C separation filter

This filter is another one of the intra-field Y/C separation filters. It separates color and luminance signals according to the frequency.

1.1 Changeover between Inter-frame and Intra-field Y/C Separation Filters

The changeover between the inter-frame and intra-field Y/C separation filters is controlled by the motion signal from the motion detection circuit in the LSI. It can also be controlled by serial bus data.

The motion detection signal to control the changeover consists of four bits. These can combine the two types of Y/C separation filters in the following 16 different ways.

Motion Signal	Intra-field Y/C Separation	Inter-frame Y/C Separation	Motion Signal	Intra-field Y/C Separation	Inter-frame Y/C Separation
0	0	1	8	0.5	0.5
1	0.0625	0.9375	9	0.5625	0.4375
2	0.125	0.875	10	0.625	0.375
3	0.1875	0.8125	11	0.6875	0.3125
4	0.25	0.75	12	0.75	0.25
5	0.3125	0.6875	13	0.8125	0.1875
6	0.375	0.625	14	0.875	0.125
7	0.4375	0.5625	15	1	0

The above table lists the ratios for adaptive composition of filter outputs. The output ratio is based on "1".

The serial bus data to control the changeover is a combination of MSC and MSD bits at subaddress SA$_6$. Unlike the motion detection signal to set the filters into 16 types of combinations, the serial bus data selects only one of inter-frame or intra-field Y/C separation filters. If the MSC and MSD bits are set respectively to 1 and 0, the intra-field Y/C separation filter is selected. If both are set to 1, the inter-frame Y/C separation filter is selected. While the MSC bit is 0, the motion detection signal selects the two types of filters as specified in the above table. (For details, see Section 7 explaining the functions of the serial bus.)

The external LINE pin (pin No. 63) is also available to select one of the two types of Y/C separation filters. If the LINE pin is high, the intra-field Y/C separation filter is selected forcibly. While the pin is low, the motion detection signal selects the type as specified as shown in the above table.

1.2 Selection between Intra-field Y/C Separation Filters

When the intra-field Y/C separation is specified, one of the inter-line Y/C separation and frequency separation filters is selected by the external FIL$_1$ pin or serial bus data.

The FIL$_1$ pin is controlled by the output from the interleave detection circuit in the μPD9383 (TIGII). The interleave detection signal is output when the chroma and horizontal-synchronizing signal are mis-coordinated in terms of interleave. The LSI performs Y/C separation correctly for even inappropriately interleaved signals using the detection output.

When the FIL_1 pin inputs a high signal, the Y/C separation filter of frequency separation type is selected. When it inputs a low signal, the Y/C separation filter of line combing type is selected.

The serial bus data to control the selection is the BPFS bit at subaddress SA_6. If the BPFS bit is set to 1, the frequency separation type is selected. If it is set to 0, the line combing type is selected.

When the inter-frame Y/C separation is specified, the pin and the serial bus data cannot control the selection. (For details, see Section 7 explaining the functions of the serial bus.)

1.3 Characteristics of Y/C Separation Filter

The Y/C separation unit consists of several blocks as shown in Fig. 1-1. The internal filters are all FIR filters. Figs. 1-2 and 1-3 show the characteristics of inter-frame Y/C separation, inter-line Y/C separation, and frequency separation filters. Note that Figs. 1-2 and 1-3 do not apply to the characteristic of the combing filter but to those of the built-in filters.
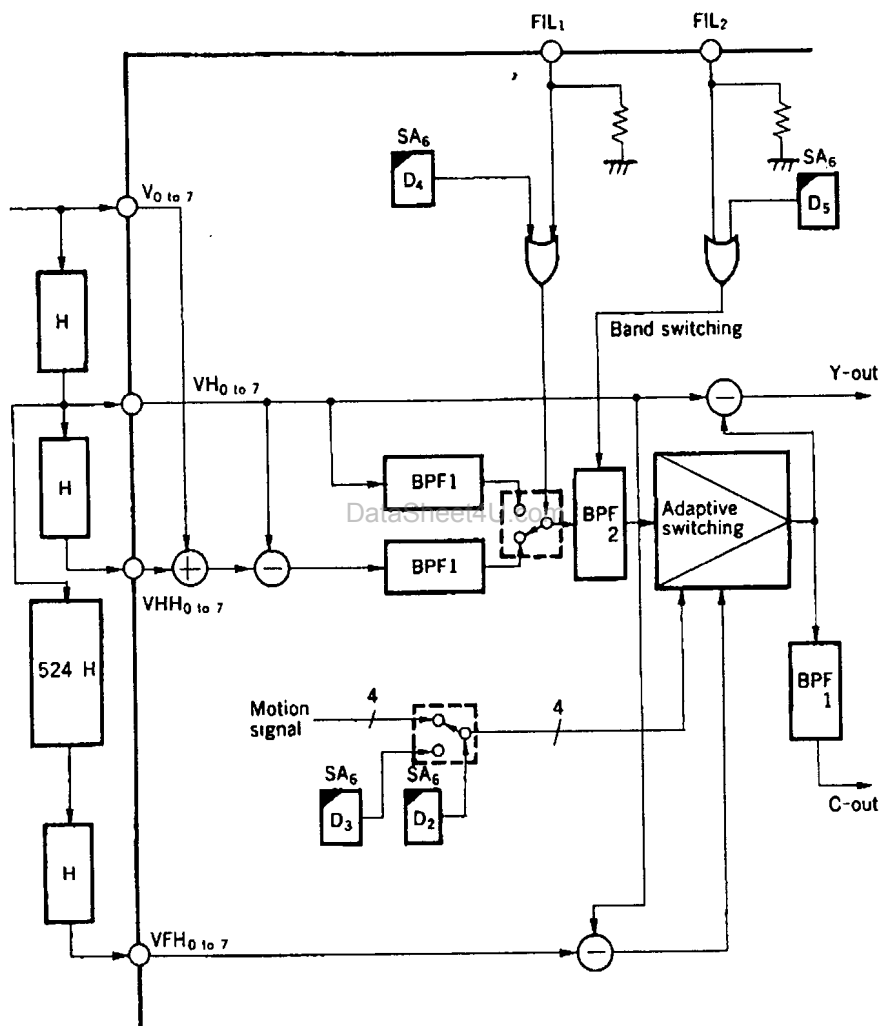
Fig. 1-1 Y/C Separation Filter Block Diagram

Fig. 1-2 Characteristics of Inter-line Y/C Separation and Frequency Separation Filters (Calculated Data)
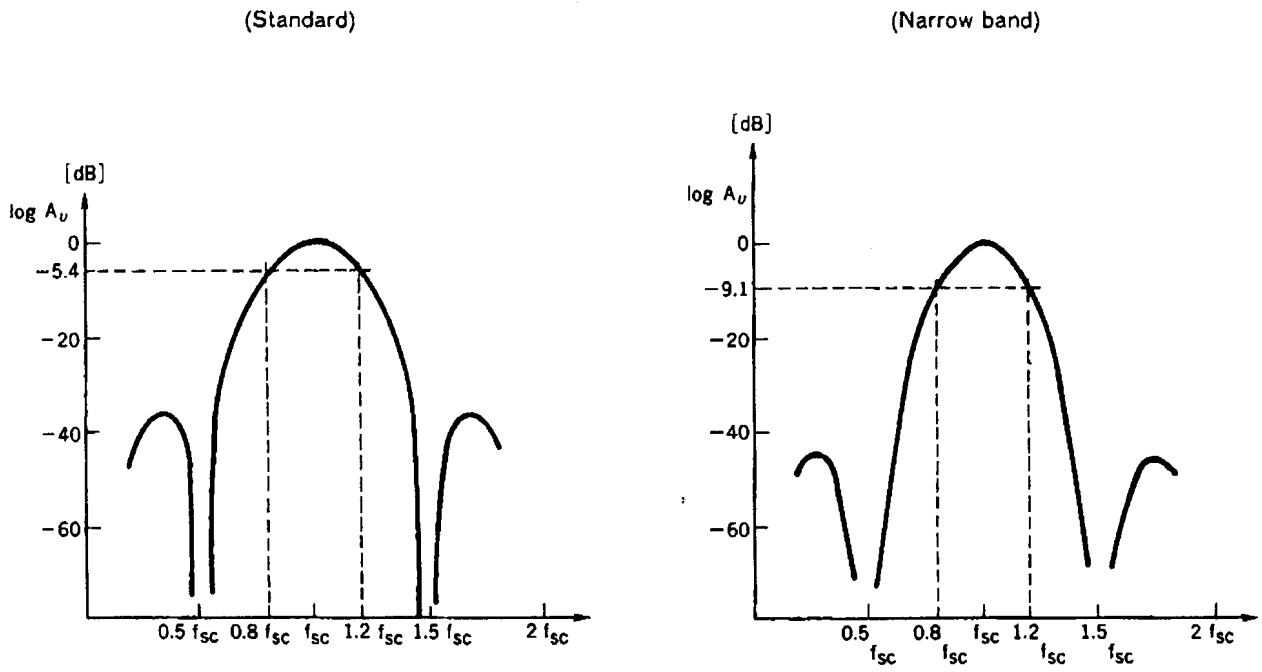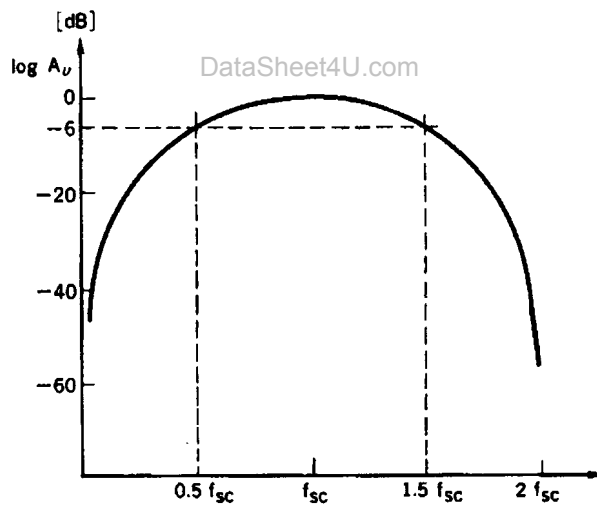
(Standard)

(Narrow band)

Fig. 1-3 Inter-frame Y/C Separation

2. A/D INPUT

The video signal input of the μPD9388A inputs signals having the pedestal level of 64 (256 on the full scale). Determine the dynamic range for the video input signals in consideration of input signal dispersion. Fig. 2-1 shows the input waveform having the synchronizing signal portion on the full scale.

The EDTV system protects the synchronizing signal to the end without modification and subjects it to synchronous separation after double-speed conversion, to be used as the signal for the deflecting system. Since the synchronizing signal carries important information, it must be correctly A/D converted and input.

The μPD9388A has a feedback loop as shown in Fig. 2-2 to help adjustment of the pedestal level. The feedback loop samples the pedestal level of an input video signal using an external clamp pulse input from the CLPI pin. It compares the sampled level to the internally fixed level of 64. The PWM D/A converter and an external filter convert the level difference to a DC voltage. The DC voltage is fed back to the pedestal level adjuster in front of the A/D converter.

Fig. 2-1 Video Signal Input Waveform
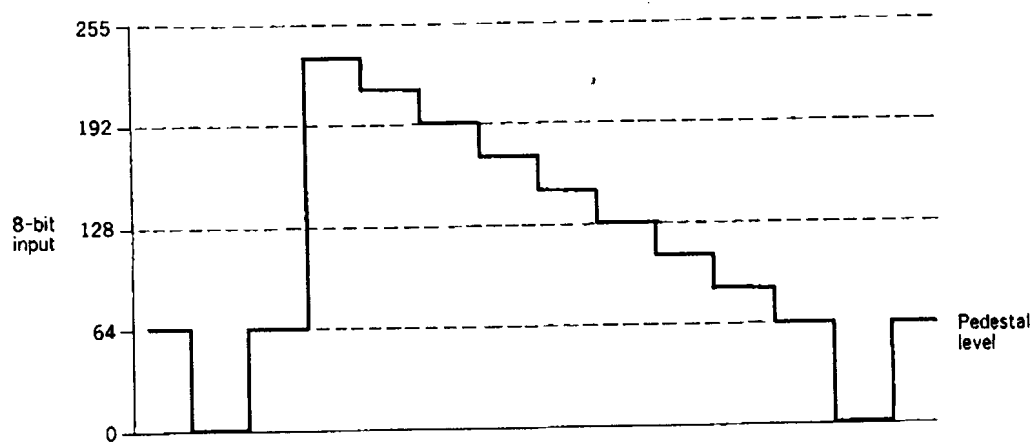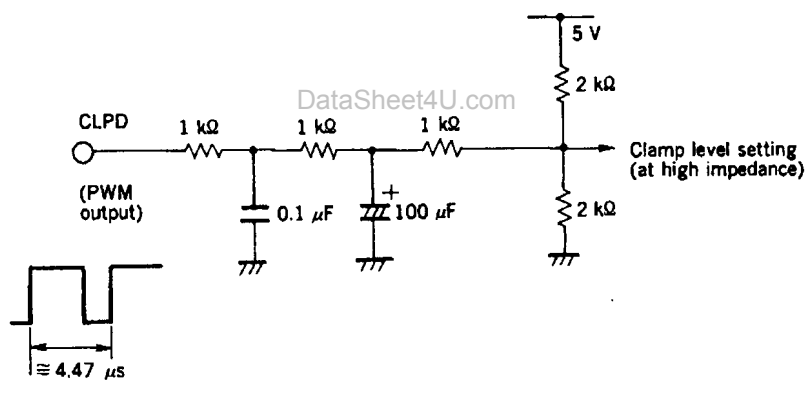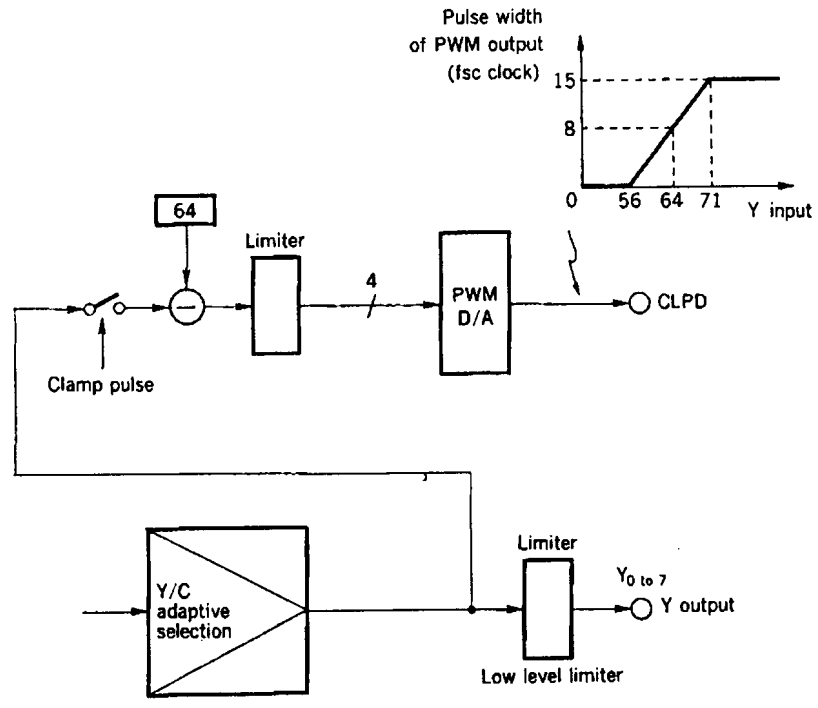

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Fig. 2-2 Clamp Level Feedback Block Diagram

3. S-TERMINAL MODE

If luminance and color signals are input separately, the LSI handles these signals using the video input pin (V pin) and the separate chroma input pin (CS pin). Accordingly, the LSI outputs the signals without performing Y/C-signal separation. In the S-terminal mode, the signals flow in an usual way as shown in Fig. 3-2. In the normal mode, the LSI uses all the externally connected line buffers. In the S-terminal mode, the line buffers connected between VH and VHH pins and between VF and VFH pins are not used. The outputs of those unused line buffers have high impedance in the S-terminal mode. When the mode is selected via the serial bus, the line buffers connected as in Fig. 3-1 are automatically treated in the above manner.

When S-terminal mode is selected, the vertical contour gain which set by serial-bus control must be "0" data and SA$_7$, D$_3$ to D$_0$ must be all "1" data.

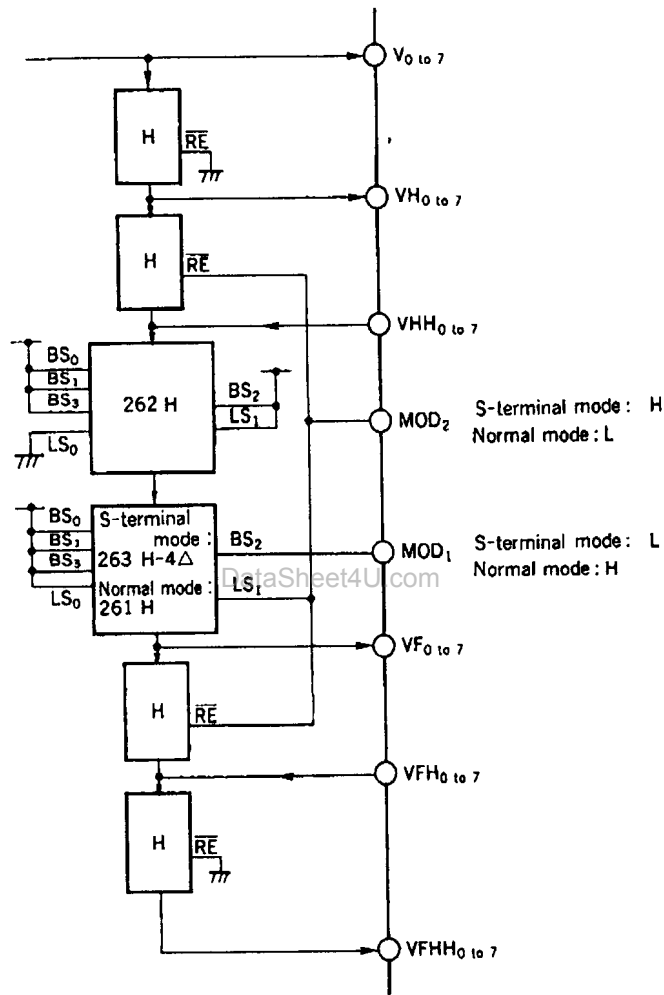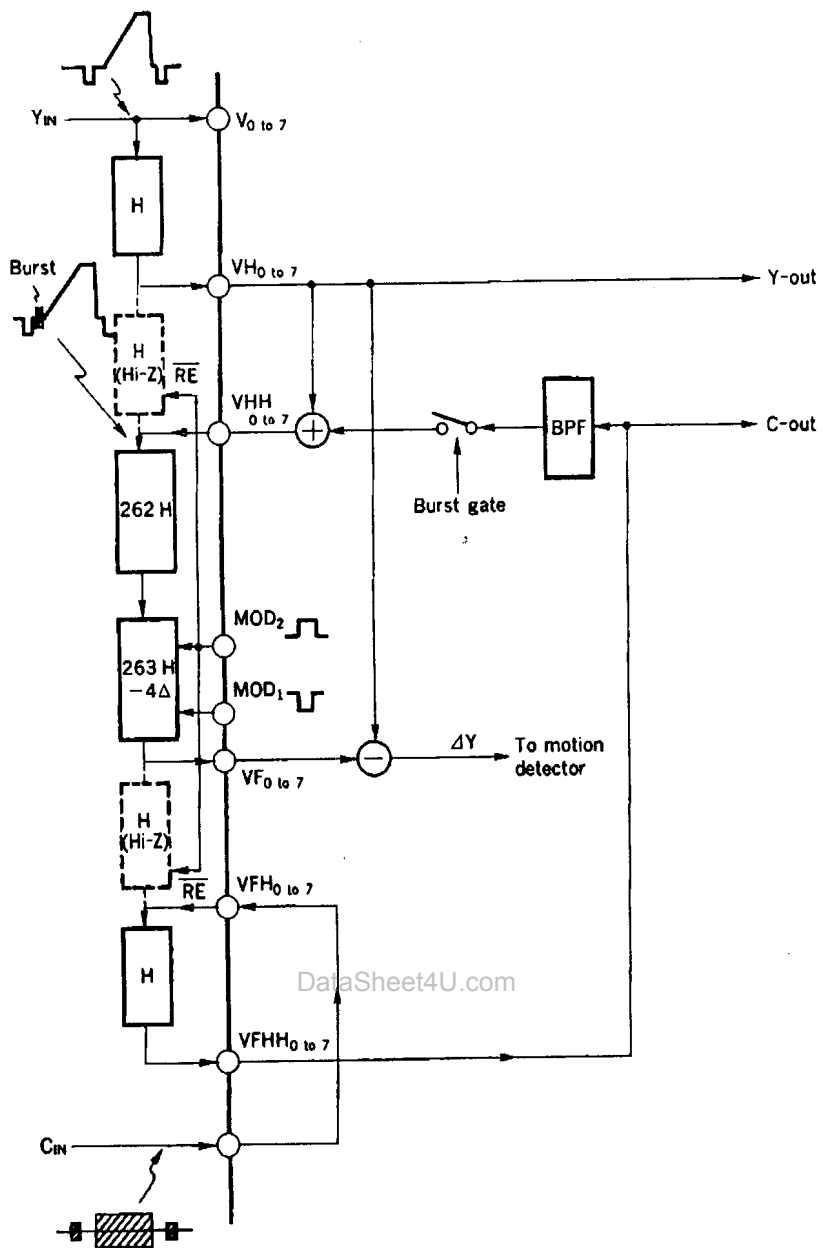<div align="center">Fig. 3-1 Connection of Line and Field Buffers</div>

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Fig. 3-2 Block Configuration in S-terminal Mode

4. VERTICAL CONTOUR COMPENSATION

The vertical contour compensation circuit reduces aperture distortion to intensify vertical contour. In this circuit, a secondary cascade filter detects a vertical edge component and a low-pass filter eliminates a color signal component and the oblique-line component of a luminance signal to select the vertical contour component. The selected signal passes through the nonlinear processing circuit consisting of coring and limiter circuits and is added to the luminance signal on the main line.

The nonlinear processing circuit contains a gain control circuit to control the intensity level as well as the coring and limiter circuits. The limiter circuit does not only clip input signals above a specific cutoff level into a certain value but also has an attenuation (−1 multiplication) characteristic. The operation point of the clipping circuit and the gain of the gain control circuit can be set via the serial bus. The coring circuit is fixed to one level.

Coring circuit : Decrements an input signal by one to establish a dead band for one level to prevent deterioration in the S/N ratio.

Limiter circuit : The signals to be processed for aperture compensation are relatively low-level signals. If the compensation is uniform, the aperture of a high-level signal is excessively intensified. Therefore the circuit attenuates signals over a certain cutoff level to change the intensity level for those higher-level signals. The level is variable with the serial bus within the range from 0 to 127.

Gain control circuit : Vary the vertical aperture intensity level. It is variable with the serial bus within the range from 0 to 7/8 multiplication in eight steps.

When SA_9, D_5 is set to "1", the vertical contour compensation can be acted in S-terminal mode.
The line and field buffers are connected as in Fig. 4-3, and the signals flow is as shown in Fig. 4-4.
However in this mode, the luminance signal of VHH_0 to 7 is not added the burst signal.

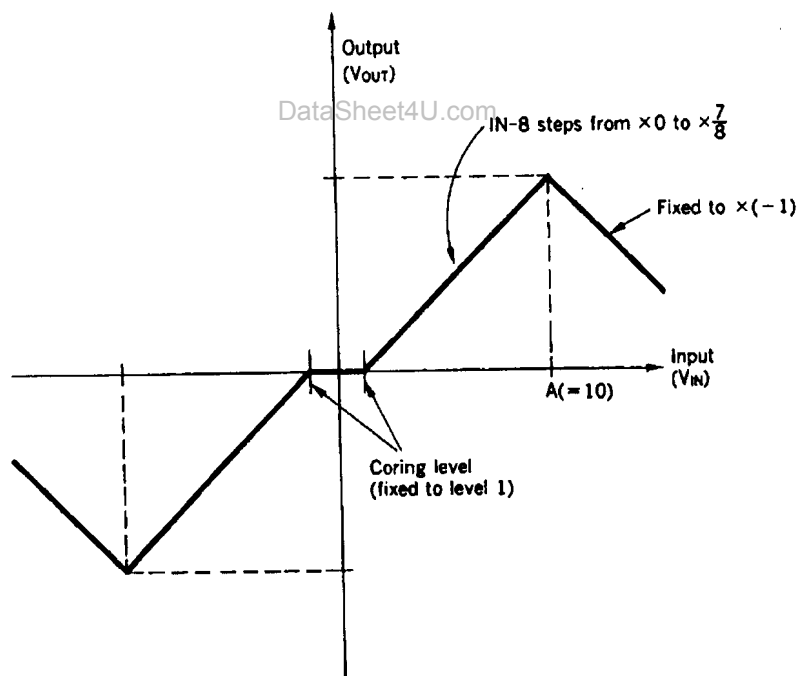### Fig. 4-1 Characteristics of Nonlinear Processing for Vertical Aperture Compensation

Fig. 4-2 Block Diagram of Vertical Aperture Compensation Circuit

Fig. 4-3 Connection of Line and Field Buffers (Vertical contour compensation is acted)