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SSI 78Q902
Ethernet Twisted-Pair Media Attachment Unit

December 1992

DESCRIPTION

The SSI 78Q902 twisted-pair Media Attachment Unit (TP-MAU) is designed to allow Ethernet connections to use the existing twisted-pair wiring plant through an Ethernet Attachment Unit Interface (AUI). The SSI 78Q902 provides the electrical interface between the AUI and the twisted-pair wire.

SSI 78Q902 functions include level-shifted data pass-through from one transmission media to another, collision detection, Signal Quality Error (SQE) testing and automatic correction of polarity reversal on the twisted pair input. It also includes LED drivers for transmit, receive, jabber, collision, reversed polarity detect and link functions.

The SSI 78Q902 is an advanced CMOS device and requires only a single 5-volt power supply.

APPLICATIONS

- Computer/workstation interface boards
- LAN repeater
- External 10Base-T converter

FEATURES

- **Meets or exceeds IEEE 802.3 standards for AUI and 10Base-T interface**
- **Direct interface to AUI and RJ45 connectors**
- **Automatic AUI/RJ45 selection**
- **Internal predistortion generation**
- **Internal common mode voltage generation**
- **Jabber function**
- **Selectable link test, SQE test disable**
- **Twisted-pair receive polarity reverse detection and selectable polarity correction**
- **LED driver for transmit, receive, jabber, collision, link and reversed polarity indicators or for flashing status indicator**
- **Single +5V supply, CMOS technology**
- **Available in 28-pin DIP or PLCC**

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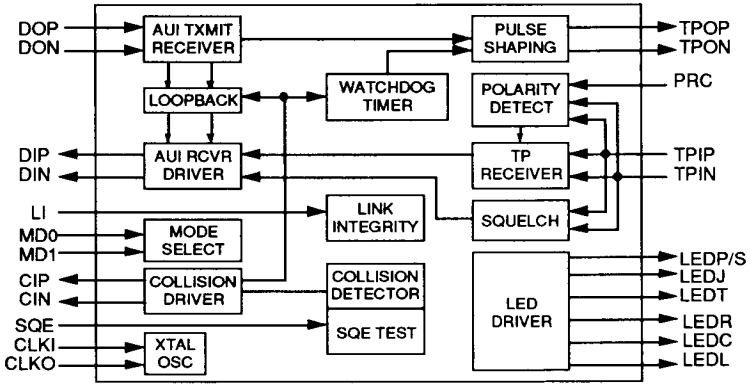
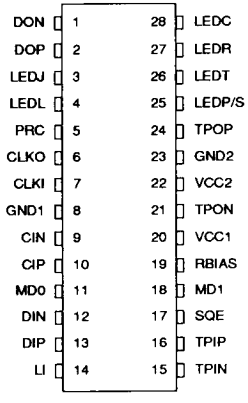
BLOCK DIAGRAM



PIN DIAGRAM



28-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78Q902 Media Attachment Unit (MAU) interfaces the Attachment Unit Interface (AUI) to the unshielded twisted pair cables, transferring data in both directions between the two. The AUI side of the interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision Interface (CI). The twisted pair network side of the interface comprises two circuits: Twisted Pair Input (TPI) and Twisted Pair Output (TPO). In addition to the five basic circuits, the SSI 78Q902 contains an internal crystal oscillator, separate power and ground pins for analog and digital circuits, various logic controls and six LED drivers for status indications.

Functions are defined from the AUI side of the interface. The SSI 78Q902 Transmit function refers to data transmitted by the Data Terminal Equipment (DTE) through the AUI and MAU to the twisted pair network. The SSI 78Q902 Receive function refers to data received by the DTE through the MAU and AUI from the twisted pair network. In addition to basic transmit and receive functions, the SSI 78Q902 performs all required MAU functions defined by the IEEE 802.3 10Base-T specification such as collision detection, link integrity testing, Signal Quality Error (SQE), jabber control and loopback.

TRANSMIT FUNCTION

The SSI 78Q902 transfers Manchester encoded data from the AUI port of the DTE (the DO circuit) to the twisted pair network (the TPO circuit). The output signal on TPON and TPOP is pre-distorted to meet the 10 Base-T jitter template, and filtered to meet FCC requirements. The output waveform (after the transmit filter) is shown in Figure 1. If the differential inputs at the DO circuit fall below 75% of the threshold level for 8 bit times (typical), the SSI 78Q902 transmit function will enter the idle state. During idle periods, the SSI 78Q902 transmits link integrity test pulses on the TPO circuit.

RECEIVE FUNCTION

The SSI 78Q902 receive function transfers serial data from the twisted pair network (the TPI circuit) to the DTE (over the DI circuit of the AUI). An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the receive function. If the differential inputs at the TPI circuit fall below 75% of the threshold level (unsquelched) for 8 bit times (typical), the SSI 78Q902 receive function will enter the idle state. The TPI threshold can be reduced by approximately 3 dB to allow for longer loops in low-noise environments. The reduced threshold is selected when MD1 = 0 and MD0 = 1.

DIFFERENTIAL INPUT MODE

In the differential input mode, the transmit interface consists of TXP and TXN, PE, PDC, and the Transmit Enable input ($\overline{TEN}$). Transmission starts when PE is high and $\overline{TEN}$ is low, and ends when either PE or $\overline{TEN}$ goes inactive. Predistortion control is provided by the PDC input.

POLARITY REVERSE FUNCTION

The SSI 78Q902 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse with the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the SSI 78Q902 enters the link fail state and no data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity is disabled, polarity detection is based only on received data pulses.)

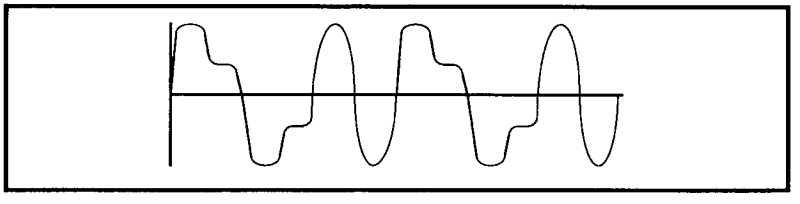


FIGURE 1: 78Q902 TPO Output Waveform

COLLISION DETECTION FUNCTION

The collision detection function operates on the twisted pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The SSI 78Q902 reports collisions to the AUI by sending a 10 MHz signal over the CI circuit. The collision report signal is output no more than 9 bit times (BT) after the chip detects a collision. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the DTE over the DI circuit, disabling the loopback. Figure 2 is a state diagram of the SSI 78Q902 collision detection function (refer to IEEE 802.3 10Base-T specification).

LOOPBACK FUNCTION

The SSI 78Q902 loopback function operates in conjunction with the transmit function. Data transmitted by the DTE is internally looped back within the SSI 78Q902 from the DO pins to the DI pins and returned to the DTE. The loopback function is disabled when a data collision occurs, clearing the DI circuit for the TPI data. Loopback is also disabled during link fail and jabber states.

SQE TEST FUNCTION

Figure 3 is a state diagram of the SQE Test function. The SQE test function is enabled when the SQE pin is tied high. When enabled, the SQE test sequence is transmitted to the controller after every successful transmission on the 10Base-T network. When a successful transmission is completed, the SSI 78Q902 transmits the SQE signal to the AUI over the CI circuit for 10 BT ± 5 BT. The SQE function can be disabled for hub applications by tying the SQE pin to ground.

JABBER CONTROL FUNCTION

Figure 4 is a state diagram of the SSI 78Q902 Jabber control function. The SSI 78Q902 on-chip watchdog timer prevents the DTE from locking into a continous transmit mode. When a transmission exceeds the time limit, the Watchdog timer disables the transmit and loopback functions, and sends the SQE signal to the DTE over the CI circuit. Once the SSI 78Q902 is in the jabber state, the DO circuit must remain idle for a period of 491 to 525 ms before it will exit the jabber state.

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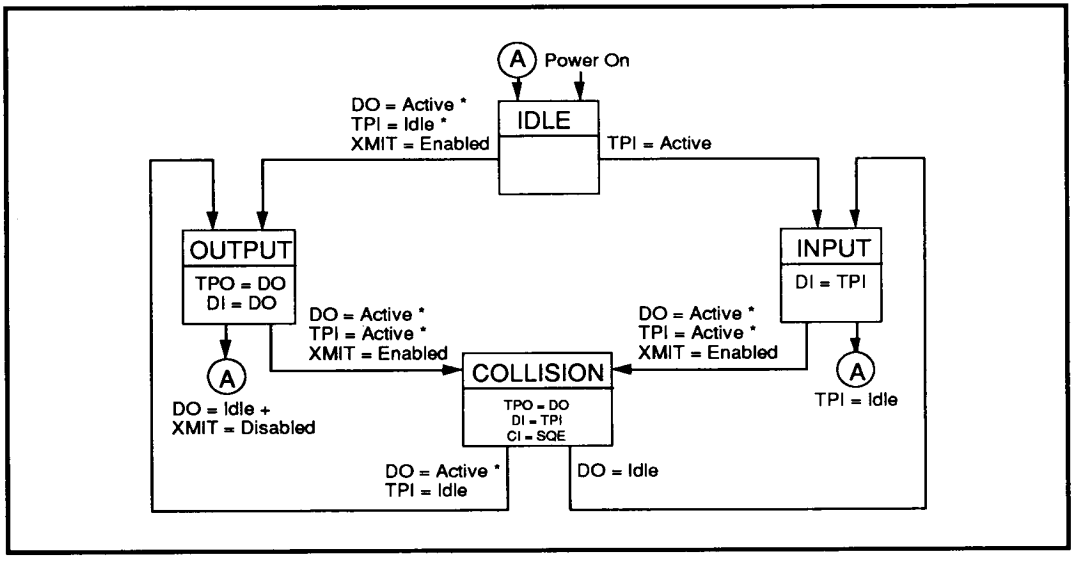

FIGURE 2: Collision Detection Function

LINK INTEGRITY TEST FUNCTION

Figure 5 is a state diagram of the SSI 78Q902 Link Integrity Test Function. The Link Integrity Test is used to determine the status of the receive side twisted pair cable. The link integrity test is enabled when the LI pin is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and loopback functions. The SSI 78Q902 ignores any link integrity pulse with intervals less than 2 - 7 ms. The SSI 78Q902 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

TEST MODE

The SSI 78Q902 Test mode is selected when a 2 to 2.5 MHz clock is input on the MD0 mode select pin. Test mode sets the internal counter chains to run at 1024 times their normal speed. The maximum transmit time, unjab time, Link Integrity timing and LED timing are reduced by a factor of 1024. During test operation, 10 MHz and 20 MHz signals are output on the PRC and SQE pins, respectively. When Test mode is selected, the SQE function cannot be disabled. In Test mode the PRC function can be disabled by the LI pin. Jabber can be disabled by setting MD1 = 0.

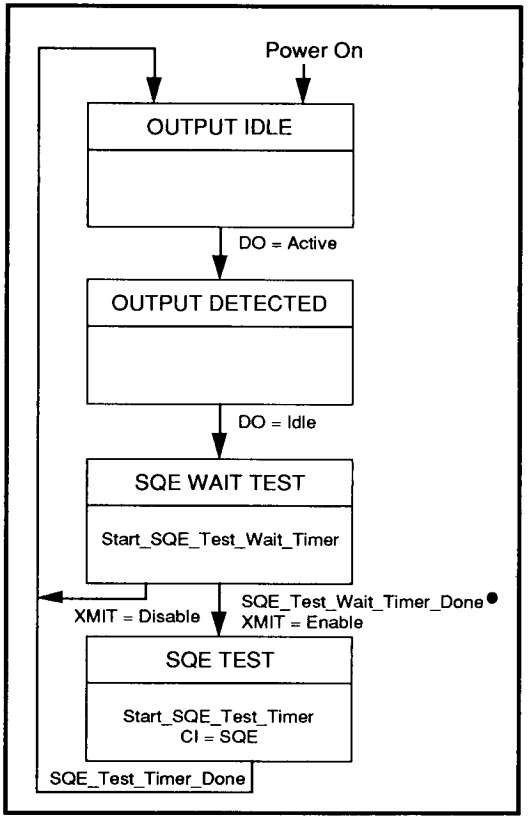

FIGURE 3: SQE Test Function

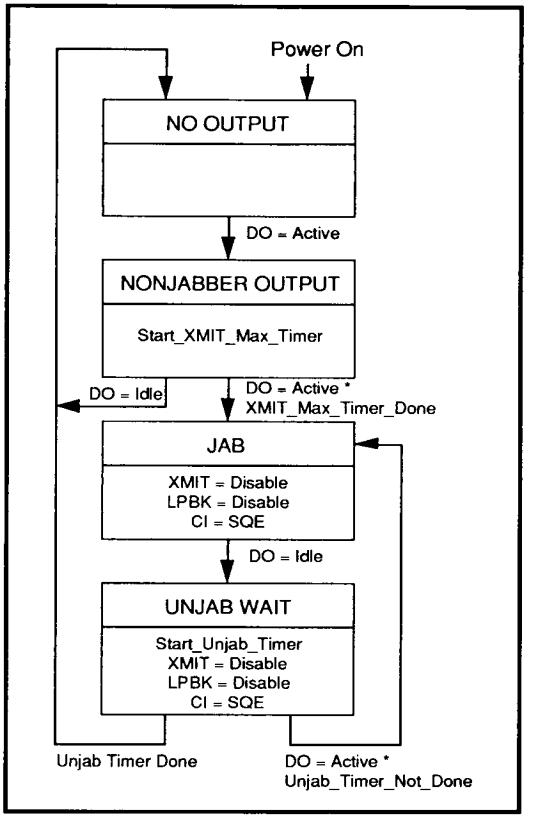

FIGURE 4: Jabber Control Function

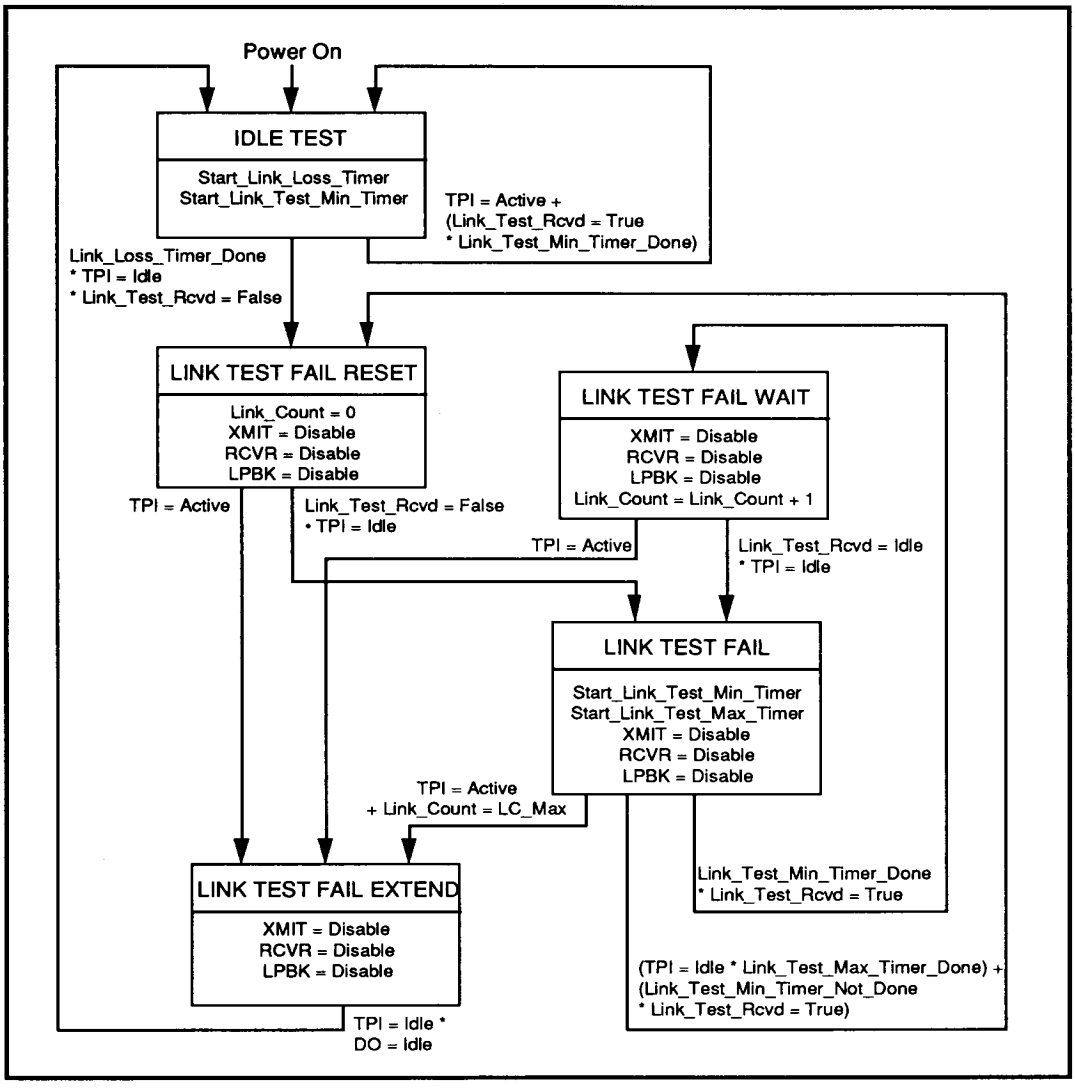

FIGURE 5: Link Integrity Test Function

TABLE 1: Mode Select Options

MD1	MD0	MODE
0	0	Base-T compliant MAU
0	1	Reduced squelch level
1	0	Half current AUI driver
1	1	DO, DI & CI ports disabled
1	Clock	Test mode, jabber on
0	Clock	Test mode, jabber disabled

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
DON/DOP	I	Data Out Negative/Data Out Positive: Differential input pair connected to the AUI transceiver DO circuit
LEDJ	I/O	Jabber LED Driver: Open drain driver for the Jabber indicator LED. Output goes active[1] when watchdog timer begins jab, and stays active until end of the unjab wait period (491 - 525 ms). When tied to ground, causes LEDP/S to act as a multi-function blinking status indicator.
LEDL	O	Link LED Driver: Open drain driver for the Link indicator LED. Output is active except during Link Fail or when Link Integrity Test is disabled.
PRC	I/O	Polarity Reverse Correction: The SSI 78Q902 automatically corrects reversed polarity at TPI when PRC is tied high. In Test mode, this pin is a 10 MHz output.
CLKO/CLKI	-	Crystal Oscillator: The SSI 78Q902 requires either a 20 MHz crystal (or ceramic resonator) connected across these pins, or a 20 MHz clock applied at CLKI.
GND1	-	Ground #1.
CIN/CIP	O	Collision Negative/Collision Positive: Differential driver output pair tied to the collision presence pair of the Ethernet transceiver AUI cable. The collision presence signal is a 10 MHz square wave. This output is activated when a collision is detected on the network, during self-test by the SQE sequence, or after the watchdog timer has expired to indicate the transmit wire pair has been disabled.
MD0	I	Mode Select 0: Selects operating modes in conjunction with MD1. See Table 1 above for mode select options.
DIN/DIP	O	Data In Negative/Data In Positive: Differential driver pair connected to the AUI transceiver DI circuit.

[1] LED drivers pull low when active.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
LI	I	Link Integrity Test Enable: Link integrity testing is enabled when this pin is tied high. With link test enabled, the SSI 78Q902 sends the link integrity signal in the absence of transmit traffic. It also recognizes received link test pulses, indicating the receive wire pair is present in the absence of transmit traffic.
TPIN/TPIP	I	Twisted Pair Receive Inputs: Differential receive inputs from the twisted pair input filter.
SQE	I/O	Signal Quality Error Test Enable: SQE is enabled when this pin is tie high. When enabled, the SSI 78Q902 sends the signal quality error test sequence to the CI of the AUI cable after every successful transmission to the media. In Test mode, SQE becomes a 20 MHz output.
MD1	I	Mode Select 1: Selects operating modes in conjunction with MD0, (see Table 1). MD1 clock input between 2.0 and 2.5 MHz enables Test mode.
RBIAS	-	Resistor Bias Control: Bias control pin for the operating circuit. Bias set from external resistor to ground. External resistor value = 12.4 kΩ (±1%).
VCC1	I	Power Supply 1: +5V power supply.
TPON/TPOP	O	Twisted Pair Transmit Outputs: Transmit drivers to the twisted-pair output filter. The output is Manchester encoded and pre-distorted to meet the 10Base-T template.
VCC2	I	Power Supply 2: +5V power supply.
GND2	-	Ground #2.
LEDP/S	O	Polarity/Status LED Driver: Open drain LED driver. In normal mode, LEDP/S is active when reversed polarity is detected. If LEDJ is tied to ground, the output LEDP/S indicates multiple status conditions as shown in Figure 6. On solid = Normal, 1 Blink = Link Down, 2 Blinks = Jabber, 5 Blinks = Polarity Reversed
LEDT	O	Transmit LED Driver: Open drain driver for the Transmit indicator LED. Output is active during transmit.
LEDR	O	Receive LED Driver: Open drain driver for the Receive indicator LED. Output is active during receive.
LEDC	O	Collision LED Driver: Open drain driver for the Collision indicator LED. Output is active when a collision occurs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNIT
Supply Voltage, Vcc	-0.3 to 6	V
Operating Temperature, TOP	0 to +70	°C
Storage Temperature, TST	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage[1], Vcc		4.75	5.0	5.25	V
Operating Temperature, TOP		0	-	70	°C

[1]Maximum voltage differential between VCC1 and VCC2 must not exceed 0.3V.

SWITCHING CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

PARAMETER	CONDITIONS	MIN	NOM [1]	MAX	UNIT
Jabber Timing					
Maximum transmit time [2]		98.5	-	131	ms
Unjab time [2]		491	-	525	ms
Time from Jabber to CS0 on CIP/CIN [3]		0	-	900	ns
Link Integrity Timing					
Time link loss [2]		65	-	66	ms
Time between Link Integrity Pulses [2]		9	-	11	ms
Interval for valid receive Link Integrity Pulses [2]		4.1	-	65	ms
Collision Timing					
Simultaneous TPI/TPO to CSO state on CIN/CIP		0	-	900	ns
DO loopback to TPI on DI [3]		300	-	900	ns
CS0 state delay after TPI/DO idle [3]		-	-	900	ns
CS0 high pulse width		40	-	60	ns
CS0 low pulse width		40	-	60	ns
CS0 frequency		-	10	-	MHz

1 Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2 Switching times reduced by a factor of 1024 during Test mode.
3 Parameter is guaranteed by design; not subject to production testing.

SWITCHING CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%) (continued)

PARAMETER	CONDITIONS	MIN	NOM[1]	MAX	UNIT
SQE Timing					
SQE signal duration		500	-	1500	ns
Delay after last positive transition of DO		0.6	-	1.6	µs
LED Timing					
LEDC, LEDT, LEDR on time[2]		100	-	-	ms
LEDP/S on time[2] (See Figure 6)		-	164	-	ms
LEDP/S period [2] (See Figure 6)		-	328	-	ms
General					
Receive start-up delay		0	-	500	ns
Transmit start-up delay		0	-	200	ns
Loopback start-up delay		0	-	500	ns

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Switching times reduced by a factor of 1024 during Test mode.

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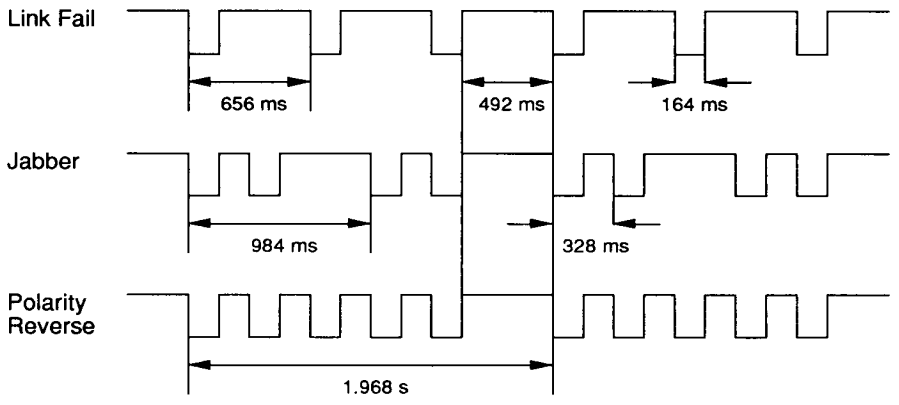
I/O ELECTRICAL CHARACTERISTICS (Ta = 0 to 70 °C, Vcc = 5V ±5%)

PARAMETER		CONDITIONS	MIN	NOM[1]	MAX	UNIT
Input low voltage[2]	V_{IL}		-	-	0.8	V
Input high voltage[2]	V_{IH}		2.0	-	-	V
Output low voltage (Open drain LED Driver[3])	V_{OL}	R_{LOAD} = 2 kΩ	-	-	0.13	V
Supply current	I_{CC}	Line Idle	-	60	69.3	mA
(Vcc1 = Vcc2 = 5.25V)		Line Active, transmitting all ones	-	125	140	mA
Input leakage current[4]	I_{LL}	Input between VCC and GND	-	±1	±10	µA
Tristate leakage current	I_{TS}	Output between VCC and GND	-	±1	±10	µA

[1] Typical figures are at 25°C and are for desing aid only; not guaranteed and not subject to production testing.
[2] MD0, MD1, SQE, PRC and LI pins. MD1 clock (test mode) must be CMOS level input.
[3] LED Drivers can sink up to 10 mA of drive current.
[4] Not including TPIN, TPIP, DOP or DON.



NOTE: LEDP/S status indications are shown in order of priority, i.e., Link Fail indication supersedes Jabber indication which supersedes Polarity Reverse (when PRC = 1). Reversed polarity conditions supersede Link Fail conditions when PRC = 0 (Polarity Correction Disabled). At the LEDL indicator, reversed polarity condition reported as Link Fail when PRC = 0. This allows the user to distinguish between actual link failure and apparent link failure due to polarity reversal.

FIGURE 6: LEDP/S Status Indication Timing

AUI ELECTRICAL CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

PARAMETER		CONDITIONS	MIN	NOM[1]	MAX	UNIT
Input low current	I_{IL}		-	-	-700	µA
Input high current	I_{IH}		-	-	500	µA
Differential output voltage	V_{OD}		±550	-	±1200	mA
Differential squelch threshold	V_{DS}		-	220	-	mV
Receive input impedance	Rz	Between DOP and DON	-	20	-	kΩ

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

TRANSMIT CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

PARAMETER		CONDITIONS	MIN	NOM[1]	MAX	UNIT
Transmit output impedance	ZOUT		-	5	-	Ω
Peak differential output voltage	VOD	Load = 200Ω at TPOP and TPON	±4.5	-	±5.2	V
Transmit timing jitter addition[2]		After Tx filter, 0 line length	-	-	±8	ns
Transmit timing jitter addition[2]		After Tx filter, line model as shown in IEEE 802.3 standard for 10Base-T	-	-	±3.5	ns

RECEIVE CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

Receive input impedance	ZIN	Between TPIP/TPIN	-	20	-	kΩ
Differential squelch threshold	VDS		-	420	-	mV
Reduced squelch threshold	VDSR		-	300	-	mV
Receive timing jitter[2]			-	-	1.5	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
[2] Parameter is guaranteed by design; not subject to production testing.

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APPLICATION INFORMATION

EXTERNAL MAU

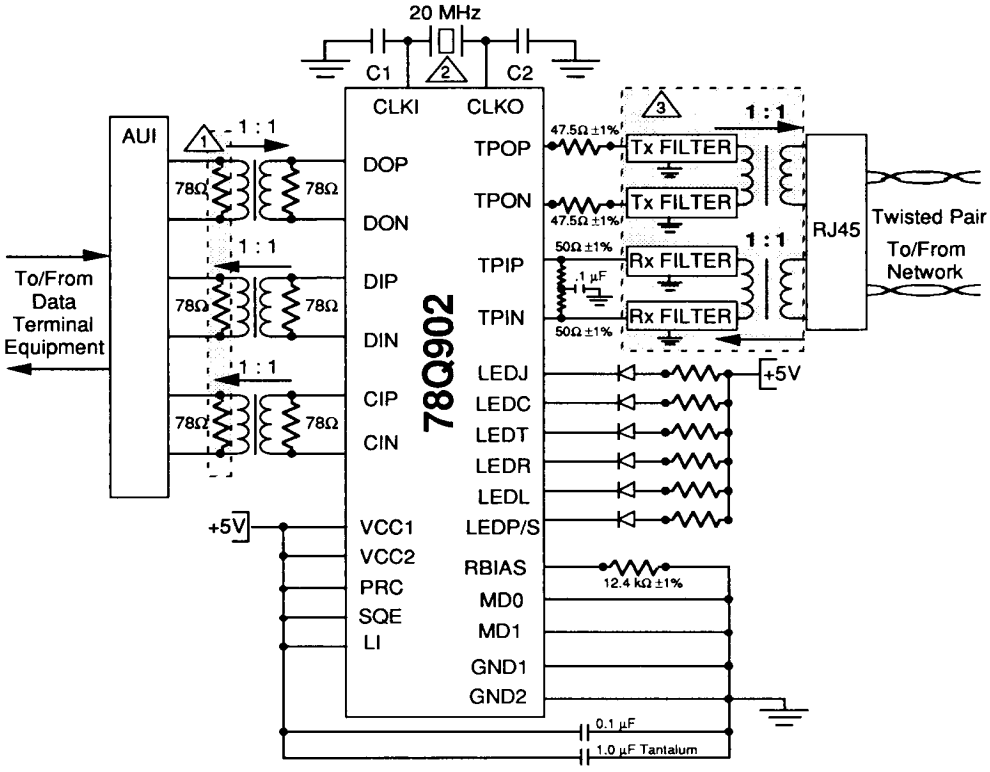
Figure 7 shows the SSI 78Q902 in a typical external MAU application, interfacing between an AUI and the RJ45 connectors of the twisted pair network. A 20 MHz crystal (or ceramic resonator) connected across CLKI and CLKO provides the required clock signal. Transmit and receive filters are required in the TPO and TPI circuits. Details of the transmit and receive filters are shown in Figures 8 and 9, respectively. (Differential filters are also recommended.)

INTERNAL MAU

Figure 10 shows an internal MAU application which takes advantage of the SSI 78Q902's unique AUI/10Base-T switching feature to select either the D-connector (AUI) or the RJ45 connector (10Base-T). No termination resistors are used on the SSI 78Q902 side of the AUI interface to prevent impedance mismatch with the drop cable. The half current drive mode is used to maintain the same voltage levels in the absence of termination resistors. This application uses capacitive coupling instead of transformer coupling. MD1 is tied high so MD0 functions as the mode control switch.

When MD0 is low, the half current drive mode is selected. When MD0 is high, the SSI 78Q902 is effectively removed from the circuit. The 902 AUI ports (DO, DI and CI) are disabled isolating the SSI 78Q902 from the AUI. The SSI 78Q902 DI and CI ports go to a high impedance state and the DO port is ignored.

To implement an auto-select function, LEDL can be tied to MD0. This activates the 902/AUI interface when the TP link is active (data or link integrity pulses) and disables it when the link is inactive.



1. Typically, resistors on the AUI side of the transformer are already present in the terminal. If termination resistors are present in the terminal, the shaded resistors are not required.
2. A 20 MHz (±1%) crystal or ceramic resonator may be used at CLKI/CLKO.
3. Suitable integrated filter/transformers include TDK Corporation HIM 3000, Pulse Engineering PE65421, FilMag 78Z1120B and Valor PT3877.

FIGURE 7: SSI 78Q902 External MAU Application Diagram

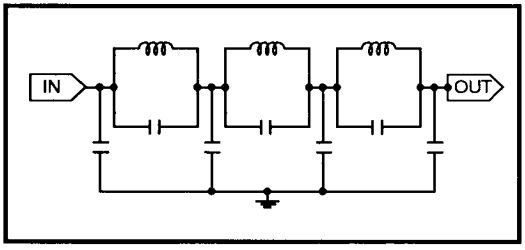


FIGURE 8: Transmit Filter Diagram

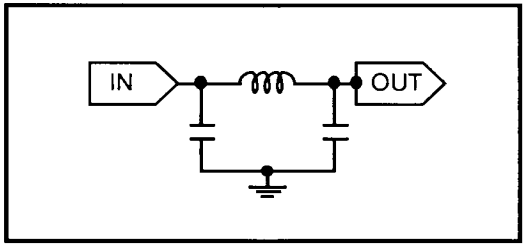


FIGURE 9: Receive Filter Diagram

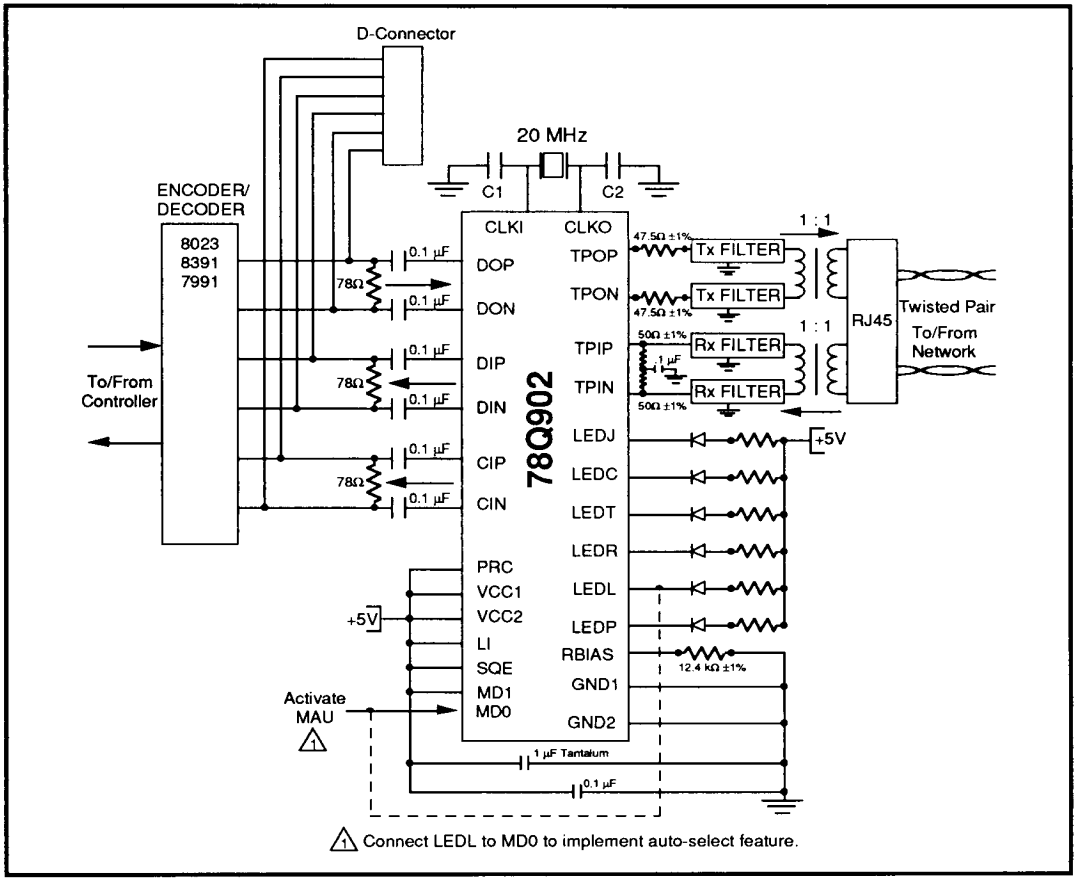
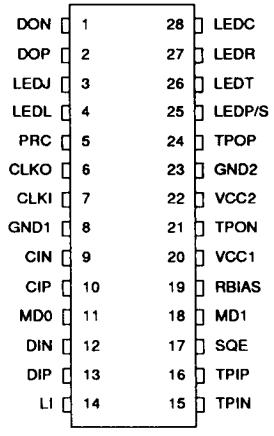


FIGURE 10: SSI 78Q902 Internal MAU Application Diagram

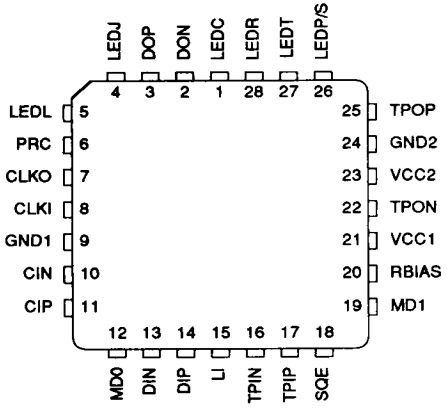
SSI 78Q902
Ethernet Twisted-Pair Media Attachment Unit

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78Q902 28-Pin DIP	78Q902-CP	78Q902-CP
SSI 78Q902 28-Pin PLCC	78Q902-CH	78Q902-CH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914