DATA SHEET

PCF5077T
Power amplifier controller for GSM and PCN systems

Preliminary specification
File under Integrated Circuits, IC17

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Semiconductors

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Power amplifier controller for GSM and PCN systems

PCF5077T

FEATURES

- CMOS low-voltage, low-power
- Can be used in burst mode with power-down
- 3-wire serial bus interface with the bus available in Power-down mode
- On-chip ramp generator for 256 different power levels with two dynamic ranges
- Two programmable regulator start conditions (V_{KICK} and V_{HOME})
- Programmable analog output voltage limitation
- Ramping speed depending on the 13 MHz system frequency clock for Global System for Mobile communications (GSM) and Personal Communications Network (PCN)
- Low swing input buffer for the 13 MHz master clock
- Compatible to a large number of different RF power modules
- Programmable temperature matching
- Dual supply concept for analog and digital part
- No external filter for suppression of clock pulse feed through
- Direct power control with ramping function (control loop can be switched off)
- On-chip Power-on reset for all registers
- Serial bus is compatible to bus systems independent of additional clock pulse after rising edge of strobe signal
- Low operating current consumption
- TTL compatible interface
- Programmable gain factor for sensor signal at OP1
- Two different voltages for 1 LSB of the burst power Digital-to-Analog Converter (DAC) are programmable.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	2.7	3.0	6.0	V
V_{DDA1}	analog supply voltage 1	note 1	2.7	3.0	6.0	V
V_{DDA2}	analog supply voltage 2 (for OP4)		2.7	5.0	6.0	V
$I_{DD(oper)(tot)}$	total operating current on the V_{DD} pins	note 2	–	9	18	mA
T_{amb}	operating ambient temperature		–40	–	+85	°C

Notes

1. The voltages V_{DDA1} and V_{DDD} must be equal and V_{DDA2} must be either equal or greater than $V_{DDA1} = V_{DDD}$.
2. $V_{DDA1} = V_{DDD} = 3$ V and $V_{DDA2} = 5$ V. The V_{DD} pins are: V_{DDA1}, V_{DDA2} and V_{DDD}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5077T	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

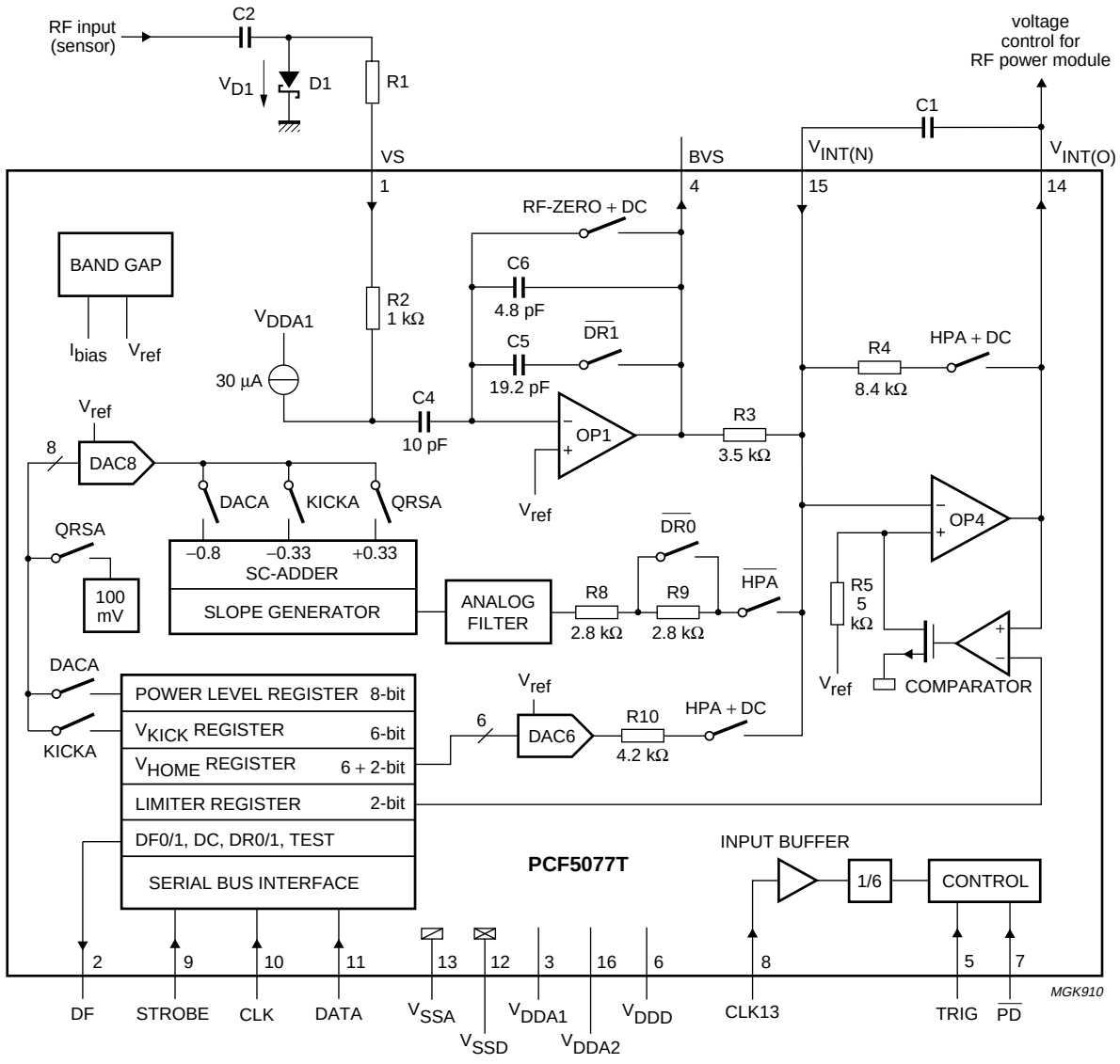


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VS	1	sensor signal input
DF	2	programmable 3-state output
V_{DDA1}	3	analog supply voltage 1
BVS	4	buffered sensor signal output
TRIG	5	trigger signal input
V_{DDD}	6	digital supply voltage
$\overline{PD}$	7	power-down input (active LOW)
CLK13	8	13 MHz master clock input (low-swing)
STROBE	9	serial bus strobe signal input
CLK	10	serial bus clock signal input
DATA	11	serial bus data signal input
V_{SSD}	12	digital ground
V_{SSA}	13	analog ground
$V_{INT(O)}$	14	integrator output
$V_{INT(N)}$	15	integrator inverting input
V_{DDA2}	16	analog supply voltage 2 (for OP4)

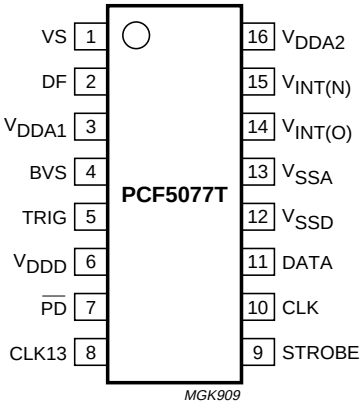


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

This CMOS device integrates operational amplifiers, two digital-to-analog converters and a serial bus interface to implement an 'Integrating-Controller' (see Fig.1). It is designed to control both the power level and the up- and down-ramping of GSM/PCN transmit bursts.

The GSM/PCN power-up and power-down ramping curves are generated on-chip, using an internal clock frequency of 2.166 MHz $\left(T_{cy} = \frac{1}{f_{clk}}\right)$, that is generated internally by dividing the external 13 MHz clock signal by six.

Generally, the power amplifier is ramped-up after a rising edge on pin TRIG and ramped-down after a falling edge.

The content of the power level register (bits PL7 to PL0) determines which of the 2×256 possible values the top of the burst will have.

To match the controller to different power modules and sensors several parameters must be adapted.
The following parameters influence the performance of the transmission system:

- The external capacitor C1 in Fig.1 determines the maximum bandwidth of the power control loop, depending on the highest steepness of the control curve of the power module and on the sensor attenuation.
- The maximum output voltage at pin $V_{INT(O)}$ to protect the power module: the limiting value of $V_{INT(O)}$ can be set to 4, 3.3 or 2.55 V, depending on the contents of the limiter register (bits Lim1 and Lim0). This limiting results in a ringing at $V_{INT(O)}$ (typ. 200 mV peak-to-peak value) but it will not be transferred to the antenna because the power module is in saturation. The limiter register bits Lim1 and Lim0 can be used to switch off the limiter option (see Table 5).
- The home position at $V_{INT(O)}$: the integrator output voltage at home position ($\overline{PD}$ = HIGH and TRIG = LOW) is programmed by means of the V_{HOME} register. Bits Vh5 to Vh0 are fed into a 6-bit DAC that generates a part of V_{HOME}.
- The temperature behaviour of the home position: bits DVh1 and DVh0 can be used to compensate temperature dependencies (–2 or –4 mV/K) of the control curves of the power module. This completes the setting of V_{HOME}.
- The KICK voltage: the 6 bits of the V_{KICK} register (Vk5 to Vk0) determine the differential integrator input voltage just after a ramp-up starting signal is detected.

The register information is written via a 3-wire serial bus (see Sections “Serial bus programming” and “Data format”).

The output of pin DF is for general purpose which can have three different states (LOW, HIGH and 3-state), depending on the values of bits DF0 and DF1 in the serial register.

Dual supply pins are provided for the analog and digital blocks.

Reset function

After switching on the power supply, the on-chip reset is active for maximal 50 µs when the rising slope of V_{DDD} has reached 1.5 ±0.4 V. During this reset, all controllers are set to the home position and the registers are set to their default values. If the supply voltage drops below the reset threshold a constant reset will appear.

Operating conditions

$\overline{PD}$ = LOW

The serial bus interface is operating, e.g. all registers can be programmed but no effect will be seen on any pin. The contents of the registers are passed to the rest of the circuit only during power-up and with the 13 MHz master clock applied.

If the low-swing input buffer at pin CLK13 is switched off, neither the SC-adder nor the slope generator will function. This means that after the chip is powered-up, the outputs have to settle again to the programmed register values. The settling time is dominated by the slow power-up of the band gap of typically 50 µs.

When the chip is used in the burst mode, it is important to switch on the PCF5077T before the power module or the RF power. Otherwise it is possible that a positive spike at $V_{INT(O)}$ will open the power module.

A safe value is t_{ON} = 200 µs between the switching on of the PCF5077T and the switching on of the power module respectively the next TRIG (see Fig.3).

$\overline{PD}$ = HIGH

The whole chip is active. CLK13 clocks the internal state machine as well as the SC-adder and slope generator. Every change at TRIG is recognized if the master clock is running. The contents of the serial bus registers are processed. If the master clock is switched off during power-up, the state machine is stopped and the output of the SC-adder and slope generator becomes undefined. Nevertheless, by reactivating the master clock, the output of the SC-adder and slope generator will settle to the old values again.

The analog integrating controller

The analog integrating controller consists of two operational amplifiers (OP1 and OP4) and a comparator. OP1 amplifies the sensor signal and OP4 is used to form a differential integrator. The comparator is used to limit the integrator output voltage to the value selected by bits Lim1 and Lim0 in the limiter register.

A (Schottky) diode D1 as external rectifier is connected to pin VS. The SC-adder block generates the voltage for the ramping of the power module.The differential integrator integrates the difference of this voltage and the voltage detected at the diode. The integrator output voltage $V_{INT(O)}$ is used to control the power amplifier module.

Table 1 Definition of some voltages used in Figs 1 and 3

SYMBOL	DESCRIPTION
V_{ref}	reference voltage, typically 1.25 V
V_{D1}	voltage over the sensor diode D1
V_{PL}	voltage determining the power level; it is generated in the Switched Capacitor (SC)-adder block if switch DACA is closed (i.e. if the signal DACA is HIGH)
V_{VS}	voltage at pin VS when RF is rectified by the sensor diode D1
V_{BVS}	amplified voltage from pin VS
V_{KICK}	voltage determining the kick level; it is generated in the SC-adder block if switch KICKA is closed (i.e. if the signal KICKA is HIGH)
V_{HOME}	voltage determining the home position voltage; if HPA signal is active, the output of DAC6 plus temperature compensation is amplified and appears at the output of OP4 (pin $V_{INT(O)}$)
V_{QRS}	low voltage at the output of the SC-adder block which causes a ramp-down with a shortened tail if switch QRSA is closed (i.e. if the signal QRSA is HIGH)
V_{RFIN}	input signal to the power amplifier

Ramp generation (see Fig.3)

The circuit is activated with the $\overline{PD}$ signal going HIGH before time mask AS and deactivated after ramping down, e.g. at time GS to HS. For this usual 'power-down burst mode' application in GSM/PCN mobile stations, the RF input power at the power module must be activated between time AS and BS (when the home position at $V_{INT(O)}$ has already reached its stable value) and deactivated between time GS and HS. This is necessary for many types of power modules to meet the –70 dB margin.

A ramp-up is started by a rising edge of the TRIG signal. The TRIG signal and all other internal signals are delayed by two clock periods ($2T_{cy}$) with respect to the signal at pin TRIG.

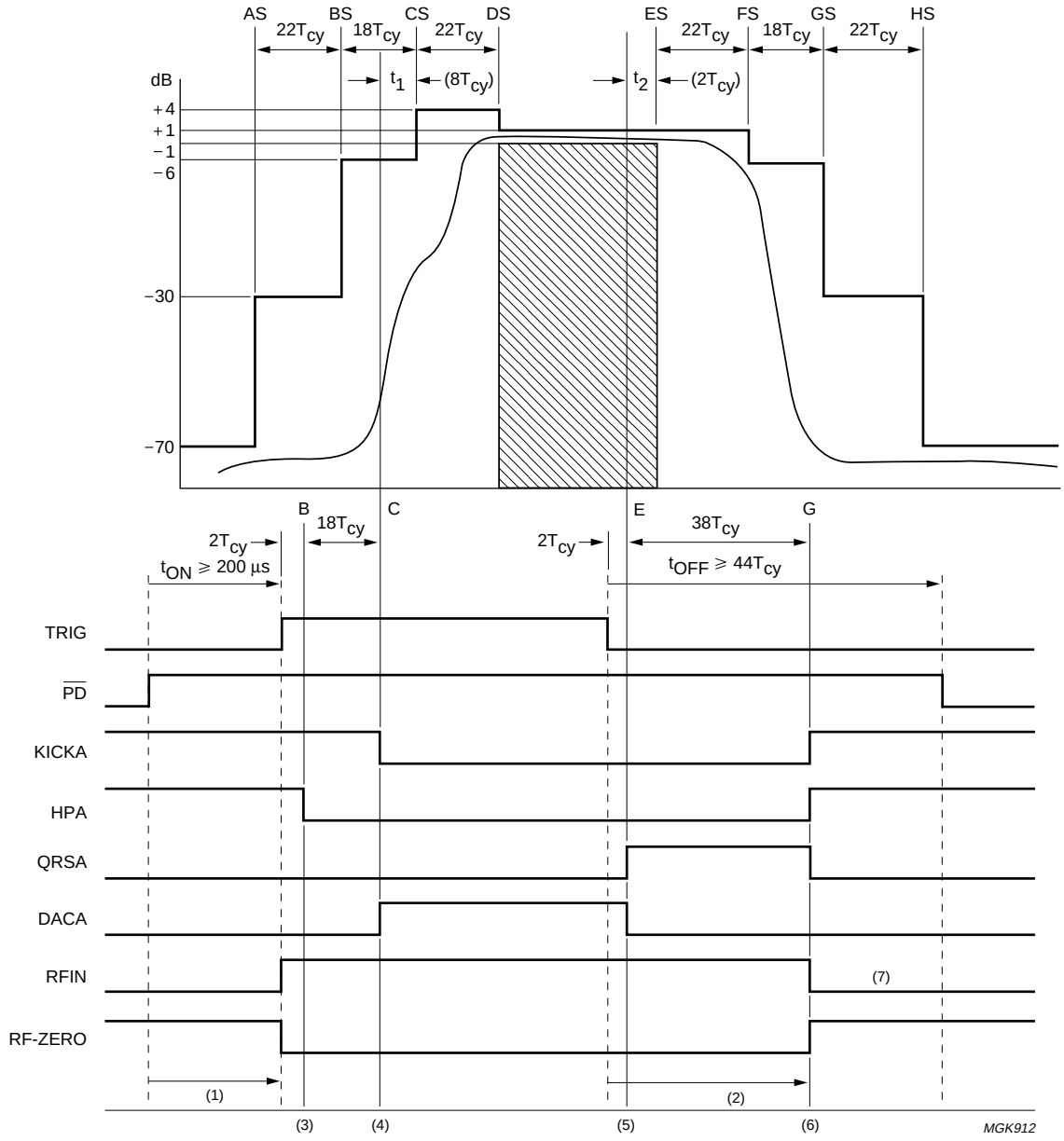
The timing diagram shows a possible relationship between the chip timing (time B to G) relative to the GSM-mask (AS to HS). However, the user is free to choose the rising and falling edge of TRIG independently so that the mask is not violated.

DESCRIPTION OF THE SIGNALS STARTING AT A STABLE HOME POSITION OF $V_{INT(O)}$ AT TIME B – $2T_{cy}$

The integrator output voltage is regulated to the value defined in the V_{HOME} register. The output of the slope generator is connected to the negative input $V_{INT(N)}$ of operational amplifier OP4 (V_{KICK} is defined by bits Vk5 to Vk0 in the V_{KICK} register). Two clock periods after a rising edge on pin TRIG, the integrator start condition circuitry is turned off and OP4 is switched into an integrator configuration (time B). The HPA switches will open (HPA + DC is either HPA switch or DC bit). Switch $\overline{HPA}$ is closed when there is no home position. Due to the negative differential input voltage V_{KICK}, the integrator output will start to rise. After $18T_{cy}$ (time C) the output of DAC8 is connected to the SC-adder and slope generator block. The input of the 8-bit DAC comes from bits PL7 to PL0 in the power level register. The slope generator will generate a smooth curve between the former and the new output value of the SC-adder block. The power amplifier is ramped-up via the integrator in approximately $22T_{cy}$.

This condition is stable as long as TRIG remains HIGH. Two clock periods after a falling edge at TRIG the ramp-down is started (time E). The SC-adder output voltage will change to V_{QRS} (–100 mV), because DACA becomes inactive and QRSA active. This causes a ramp-down with a shortened tail. The slope generator again generates a smooth curve between the new SC-adder output voltage and the old SC-adder output voltage.

The slope generator must have reached its final value at $38T_{cy}$ after the recognized falling edge of TRIG because the HPA signal is activated again and by that turning the integrator into its 'home position' (time G). The integrator output voltage will be regulated once more to the value defined in the V_{HOME} register.



(1) $t_{RFON} = t_{ON} - 12T_{cy}$ to $t_{ON} + 2T_{cy}$.
(2) $t_{RFOFF} = 44T_{cy}$ to $66T_{cy}$.
(3) V_{KICK} (start integrator) applied to integrator.
(4) V_{PL} applied to integrator.
(5) V_{QRS} applied to integrator.
(6) V_{HOME} at output of OP4.
(7) This timing of the RF input power (from the power module) ensures that the −70 dB margin is met, even if the isolation of the power module is bad.

Fig.3 Timing diagram of a typical ramp-up/ramp-down curve.

Serial bus programming

A simple 3-wire unidirectional serial bus is used to program the circuit. The 3 wires are DATA, CLK and STROBE. The data sent to the device is loaded in bursts framed by STROBE. Programming clock edges and their appropriate data bits are ignored until STROBE goes active LOW.

The last four address bits are decoded on the active STROBE edge. This produces an internal load pulse to store the data in one of the addressed registers. To avoid erroneous circuit operation, the STROBE pulse is not allowed during internal data reads by the rest of the circuit. This condition is guaranteed by respecting a minimum STROBE pulse width after data transfer.

Only the last 16 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. The bus is also programmable during power-down.

Data format

Data is entered with the most significant bit (MSB) first. The leading 10 bits p15 to p6 are the data field, the following bits p5 and p4 form the subaddress, while the last 4 bits p3 to p0 are the device address field.
The PCF5077T uses only one of the available addresses. The format is given in Table 2.

The correspondence between data and address fields is given in Table 3 and the description in Table 4.

All three registers in Table 3 are set to 00H during reset.

Table 2 Programming register format

DATA BITS				SUBADDRESS		DEVICE ADDRESS			
MSB			LSB						
p15	p14 to p8	p7	p6	p5	p4	p3	p2	p1	p0
data9	data8 to data2	data1	data0	Sadd1	Sadd0	add3	add2	add1	add0

Table 3 Register bit allocation

DATA FIELD (D9 TO D0)										SUBADDRESS		DEVICE ADDRESS			
MSB									LSB						
p15	p14	p13	p12	p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
Vk5	Vk4	Vk3	Vk2	Vk1	Vk0	Lim1	Lim0	DC	Test	0	0	1	0	1	0
Vh5	Vh4	Vh3	Vh2	Vh1	Vh0	DVh1	DVh0	DR1	DR0	0	1	1	0	1	0
PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	DF1	DF0	1	1	1	0	1	0

Table 4 Description of bits used in Table 3

BITS	DESCRIPTION
Vk5 to Vk0	6 bits to control the kick voltage in 64 steps
Vh5 to Vh0	6 bits to control the home position voltage in 64 steps
PL7 to PL0	8 bits to control the power level in 256 steps
Lim1 and Lim0	2 bits to control the limiter voltage (see Table 5)
DC	direct control with ramping function (control loop is switched off when DC = 1)
Test	test mode (Test = 1); **must always be set to logic 0 in application**
DVh1 and DVh0	2 bits to set the temperature coefficient of V_{HOME} (see Table 6)
DR1	gain factor of OP1
DR0	gain factor for slope generator output
DF1	enable of the 3-state output on pin DF (for DF1 = 0, pin DF is in 3-state mode)
DF0	data output on pin DF

Table 5 Limiter voltage

Lim1	Lim0	LIMITER VOLTAGE (V)	TOLERANCE AT T_{amb} = 27 °C (mV)	TOLERANCE AT T_{amb} = 85 °C (mV)
0	0	limiter off	–	–
0	1	4.00	±250	±350
1	0	3.30	±250	±350
1	1	2.55	±250	±350

Table 6 Programmable temperature coefficient of V_{HOME}

DVh1	DVh0	V_{HOME}(1)
0	0	Vh ±0.4 mV/K
0	1	Vh – 2 mV/K ±20%
1	0	Vh – 4 mV/K ±20%
1	1	V_{SS}

Note

1. Vh = voltage programmed in V_{HOME} register bits Vh5 to Vh0 and generated by DAC6.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1	–0.5	+6.0(1)	V
V_{DDA2}	analog supply voltage 2	–0.5	+6.0(1)	V
V_{DDD}	digital supply voltage	–0.5	+6.0(1)	V
V_I	DC input voltage on all pins (except pin VS)	–0.5	V_{DD} + 0.5	V
$V_{I(VS)}$	DC input voltage on pin VS	–3.0	V_{DD} + 0.5	V
$I_{I(n)}$	DC input current on any signal pin	–10	+10	mA
P_{tot}	total power dissipation	–	83	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C

Note

1. Pulses of 7 V are allowed for less than 100 ms.

OPERATING CHARACTERISTICS

V_{DDA1}, V_{DDA2} and V_{DDD} = V_{DD} = 2.7 to 6.0 V; V_{DDD} = V_{DDA1} ≤ V_{DDA2}; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operational amplifier (OP1)						
V_{DDA1}	analog supply voltage 1		2.7	3.0	6.0	V
GB	gain bandwidth product	V_{DDA1} = 3.0 V	2.0	–	–	MHz
G_{min}	minimum gain	DR1 = 0	−8.1	−7.6	−7.1	dB
G_{max}	maximum gain	DR1 = 1	5.9	6.4	6.9	dB
V_{offset}	offset voltage	no load at output	−20	0	+20	mV
Operational amplifier (OP4)						
V_{DDA2}	analog supply voltage 2		2.7	5.0	6(1)	V
GB	gain bandwidth product	C_L = 120 pF; V_{DDA2} = 5 V; note 2	4	–	–	MHz
PSRR	power supply rejection ratio	V_{DDA2} = 5 V, at 217 Hz	50(3)	55	–	dB
SR_{pos}	positive slew rate	V_{DDA2} = 5 V; note 4	3.5	15	–	V/µs
SR_{neg}	negative slew rate	V_{DDA2} = 5 V; note 4	3.5	6	–	V/µs
V_{offset}	voltage offset	no load at output	−20	0	+20	mV
$V_{o(min)}$	minimum output voltage		–	–	0.3	V
$V_{o(max)}$	maximum output voltage		0.85V_{DDA2}	–	–	V
I_o	output current	note 5	4.5	–	–	mA
Programmability and accuracy of V_{PL} (DAC8) at $V_{INT(O)}$						
INL	integral non-linearity		–	±1.5	±10	LSB
DNL	differential non-linearity		–	±0.2	±1	LSB
$V_{o(min)}$	minimum output voltage	DC = 1; DR0 = 1; note 6	−30	–	+60	mV
$V_{o(max)}$	maximum output voltage	DC = 1; DR0 = 0; note 6	2.72	–	3.15	V
STS	step size	DC = 1; DR0 = 1	–	6	–	mV
		DC = 1; DR0 = 0	–	11.7	–	mV
Programmability and accuracy of V_{KICK} (DAC8) at $V_{INT(O)}$						
$V_{o(min)}$	minimum output voltage	DC = 1; DR0 = 1; note 6	−50	–	+50	mV
$V_{o(max)}$	maximum output voltage	DC = 1; DR0 = 0; note 6	270	–	400	mV
STS	step size	DC = 1; DR0 = 1	–	2.6	–	mV
		DC = 1; DR0 = 0	–	5.0	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programmability and accuracy of V_{HOME} (DAC6) at $V_{INT(O)}$						
INL	integral non-linearity	note 7	–	±1.0	±3	LSB
DNL	differential non-linearity	note 7	–	±0.2	±1	LSB
$V_{o(min)}$	minimum output voltage	DVh1 = 0; DVh0 = 0	50	–	170	mV
$V_{o(max)}$	maximum output voltage	DVh1 = 0; DVh0 = 0	1.95	–	2.25	V
STS	step size		–	33	–	mV

Notes

1. Pulses of 7 V are allowed for less than 100 ms.
2. Minimum specified frequency at T_{amb} = 27 °C. For T_{amb} = 85 °C a typical value of 4 MHz is specified.
3. Not tested. Guaranteed by design.
4. Slew rates are measured between 10% and 90% of output voltage with a load of approximately 40 pF to ground.
5. Measured with R_L = 1.2 kΩ, C_L = 80 pF and V_{DDA2} = 5 V. The voltage drop at the output is less than 20 mV.
6. Referred to V_{HOME}; nominal operating condition, direct control (DC = 1), V_{HOME} programmed to 40.
7. The parameter is measured starting from code 4, due to a saturation effect for the first four codes.

DC CHARACTERISTICS

V_{DDA1}, V_{DDA2} and V_{DDD} = V_{DD} = 2.7 to 6.0 V; V_{DDD} = V_{DDA1} ≤ V_{DDA2}; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		2.7	3.0	6.0	V
V_{DDA1}	analog supply voltage 1		2.7	3.0	6.0	V
V_{DDA2}	analog supply voltage 2		2.7	5.0	6.0	V
$I_{DD(oper)(tot)}$	total operating current on the V_{DD} pins	f_{CLK13} = 13 MHz; see Fig.5	–	9	18	mA
$I_{DD(idle)(tot)}$	total idle current on the V_{DD} pins	$\overline{PD}$ = LOW	–	4	20	µA
Logic inputs (pins TRIG, STROBE, CLK and DATA)						
I_{LIL}	LOW-level input leakage current	V_{IL} = 0 V	–5	–	+5	µA
I_{LIH}	HIGH-level input leakage current	V_{IH} = 6 V	–5	–	+5	µA
C_i	input capacitance		–	10	–	pF
V_{IL}	LOW-level input voltage		0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.5V_{DD}$	–	V_{DD}	V
3-state output (pin DF)						
V_{OL}	LOW-state output voltage	I_{OL} = I_{OH} = 3 mA	–	–	0.4	V
V_{OH}	HIGH-state output voltage	I_{OL} = I_{OH} = 3 mA	$0.7V_{DD}$	–	–	V
I_{LO}	3-state output leakage current	V_{DF} = 0 to V_{DD}	–5	–	+5	µA
Low-swing master clock input (pin CLK13)						
I_{LI}	input leakage current		–5	–	+5	µA
C_i	input capacitance		–	10	–	pF
$\lvert Z_i \rvert$	input impedance	f_{CLK13} = 13 MHz; note 1	–	5	–	kΩ
$V_{i(p-p)}$	input voltage (peak-to-peak value)	note 2	0.35	–	V_{DD}	V
Sensor input voltage (pin VS)						
$V_{i(VS)}$	input voltage at pin VS		–3.0	–	V_{DD}	V
Band gap						
I_{bias}	bias current (source for D1)	V_{VS} = 0 V; T_{amb} = 25 °C; TC = –0.08 µA/K	21	28	35	µA
V_{ref}	reference voltage	T_{amb} = 25 °C	1.18	1.25	1.32	V
TC	temperature coefficient for V_{ref}		–	±170	–	ppm/K
t_{pu}	power-up time for V_{ref}	note 3	–	5	50	µs
Power-on reset, threshold voltage V_{th}; see Fig.4						
V_{th}	threshold voltage	T_{amb} = 25 °C; TC = –4 mV/K	1.2	1.5	1.8	V
t_{rst}	reset time		–	–	50	µs

Notes

1. An AC coupling with 33 pF is recommended.
2. Tested at nominal working condition (V_{DDD} = V_{DDA1} = 3 V; V_{DDA2} = 5 V). AC coupling = 33 pF.
3. The necessary start-up time t_{ON} = 200 µs (see Fig.3) between $\overline{PD}$ and TRIG is more than t_{pu}.

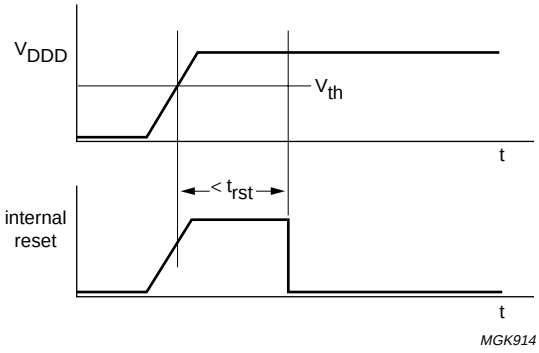
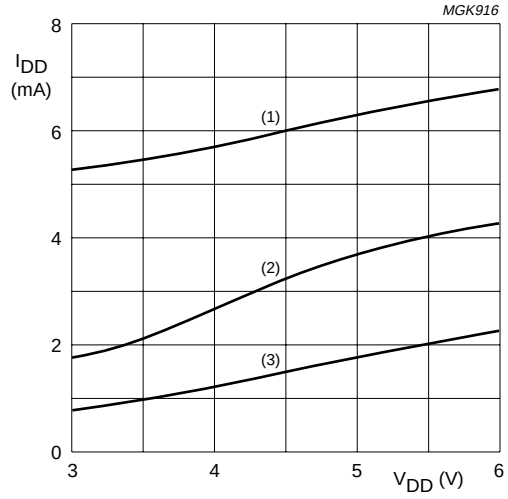


Fig.4 Timing diagram for on-chip reset function.



(1) I_{DDA1}. (2) I_{DDA2}. (3) I_{DDD}.

Fig.5 Operating current I_{DD} as a function of V_{DD}.

TIMING CHARACTERISTICS

V_{DDA1}, V_{DDA2} and V_{DDD} = 2.7 to 6.0 V; $V_{DDD} = V_{DDA1} \leq V_{DDA2}$; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	UNIT
Controller timing; see Fig.3				
$t_{d(TRIG-B)}$	delay from positive TRIG edge to time B = $^{13}/_{6}T_{cy}$	–	1.0	µs
$t_{d(B-C)}$	delay from time B to time C = $18T_{cy}$	–	8.31	µs
$t_{d(TRIG-E)}$	delay from negative TRIG edge to time E = $^{13}/_{6}T_{cy}$	–	1.0	µs
$t_{d(E-G)}$	delay from time E to time G = $38T_{cy}$	–	17.54	µs
Serial bus timing; see Fig.6				
SERIAL PROGRAMMING CLOCK (PIN CLK)				
t_r	rise time	–	10	ns
t_f	fall time	–	10	ns
T_{cy}	clock period	100	–	ns
ENABLE PROGRAMMING (PIN STROBE)				
t_{start}	strobe start time to first clock edge	0	–	ns
t_{end}	strobe end time after last clock edge	40	–	ns
REGISTER SERIAL INPUT DATA (PIN DATA)				
t_{su}	input data to CLK set-up time	20	–	ns
t_h	input data to CLK hold time	20	–	ns

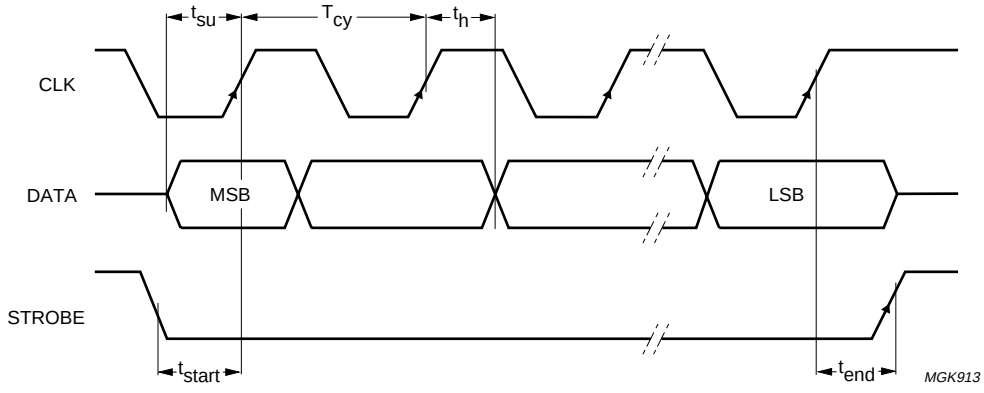


Fig.6 Serial bus timing diagram.

APPLICATION INFORMATION

Direct power control with ramping function (DC = 1)

The circuit offers a useful feature to control power levels close to the saturation region of the external power module.

This flexibility consists in the direct control on the power level by setting bit DC to logic 1.

In this condition, the external control loop is switched off by disabling the gain path from OP1. The ramping shape of the signal to be transmitted as well as its final level are driven only by the internally generated control signal from the slope generator. In this way transient effects to recover active components from deep saturation are avoided. The relative error on the absolute value of output power is quite limited, as a power amplifier is less sensitive to temperature variation in its saturated region. However, this way of operating may increase the phase error.

Increased dynamic range

The PCF5077T is able to control a dynamic range of 30 dBm by switching the gain factor of the sensor amplifier and the resolution of DAC8. This range corresponds to a maximum peak-to-peak voltage of 3 V measured at the sensor diode. Figure 7 shows the voltage at the sensor diode (V_S) versus the output power (P) of the Power Amplifier (PA) with a directional coupler of 20 dB attenuation. The maximum voltage of 3 V is reached when the output power is 35 dBm.

The sensor voltage for power level lower than 13 dBm, as necessary for GSM Phase 2 and DCS1800, is lower than 200 mV. An 8-bit DAC would not be sufficient to cover the complete dynamic range. Therefore bits DR0 and DR1 are used to switch the power range that can be controlled with the controller (see Table 7).

Reduced voltage steps of power level DAC8 (DR0 = 1)

The DR0 bit is used to switch resistor R9 (switch $\overline{DR0}$ is closed) at the integrator input (OP4). The ratio of the DAC8 range to the sensor signal voltage is therefore halved and the power corresponding to one LSB of DAC8 is reduced by 3 dB. With this setting the power module can be controlled more accurately for low output power levels.

Gain factor of OP1 (DR1)

Bit DR1 switches (switch $\overline{DR1}$ is closed) the ratio of the capacitances at OP1. The gain factor for the sensor amplifier is five times higher when DR1 is in high state.

When DR1 = 1, the control loop regulates the output power of the PA to a lower power level. A dynamic range of about 10 dBm can be switched by this manner.

$V_S : V_{peak}$ is the ratio of sensor signal to slope generator output voltage effective at the integrator output (OP4).

Table 7 Gain factors

DR1	DR0	$V_S : V_{peak}$
0	0	1 : 1
0	1	2 : 1
1	0	5 : 1
1	1	10 : 1

Additional application information

Evaluation kits with software and demonstration board are available for the PCF5077T together with Philips power modules BGY206, CGY2010, CGY2020 and CGY2021 for GSM and PCN, which will provide help for applications.

Very little bus traffic is required for the PCF5077T because the ramping curves are generated on-chip. V_{KICK} and V_{HOME} define the start conditions for up-ramping. V_{PL} determines the power levels. TRIG is the trigger for up and down-ramping.

The non-linear behaviour of the control curves of the power modules have a big influence on the loop. Start conditions in the flat area of the control curve are critical and need some attention. Initially $V_{INT(O)}$ will be at the home position. The HPA switches release the regulator. The integrator is moved into the active part of the control curve. This is achieved by integrating V_{KICK}. When $V_{INT(O)}$ has reached the active region of the control curve the loop is closed and the circuit is able to follow the ramping function generated by a voltage step to the slope generator. The step height V_{PL} determines the power of the transmit burst. Down-ramping is started at the slope generator input by a voltage step from V_{PL} back to V_{QRS}. The loop follows the leading function for down-ramping until the RF sensor measures zero. The reason for V_{QRS} is to shorten the tail of the slope.

Figures 8 and 9 show the results of measurements on the up and down-ramping where REF is the reference level of the power in the time slot, ATTEN is the attenuation of the input instrument for not to destroy the instrument itself, RES BW is the resolution bandwidth, VBW is the video bandwidth, CENTER is the carrier frequency for the burst that has been measured and SWP is the sweep time used for the measurement.

ADJUSTMENT OF THE HOME POSITION

The 6-bit DAC for V_{HOME} determines the start point of the burst in the time template. Curve 2 in Fig.8 shows what happens when V_{HOME} is too low. The burst starts too late and the up-ramping of the power is too steep. The steep up-ramping results in a wide transient spectra. The RF input power shall be switched off when the TRIG signal is LOW to keep the −70 dB margin before the burst.

The home position has to be adjusted for each mobile phone because of DAC tolerances and individual PA characteristics.

The temperature coefficients for V_{HOME} (−2 and −4 mV/K) are used to compensate the temperature shift of the PA control curve. Therefore the PA and the controller shall be placed nearby on the printed-circuit board. Additionally it has to be considered that the temperature of the PA and PCF5077T are different because the PA heats up itself. Software may help to adapt V_{HOME} to different temperatures.

ADJUSTMENT OF V_{KICK}

After the falling edge of HPA the integrator starts to increase the control voltage up to the position of V_{KICK} where the PA should have reached its active region. Increasing V_{KICK} at high power level makes the up ramping of the burst smoother and improves the transient spectra.

V_{KICK} must be reduced for low level of V_{PL} to avoid that both voltages become equal. Setting V_{KICK} to minimum value for the lowest power level can be sufficient.

At low power level the burst will start later because of the bend sensor curve (see Fig.7). The trigger pulse has to be started up to 3 bits earlier for the lowest power level to avoid that the power is ramped up too late for the first data bits of the burst.

LIMIT FOR CORRECT DOWN-RAMPING

The maximum RF power that the power module in saturation is able to deliver depends on RF input power, transmit frequency, supply voltage, temperature and load impedance. The maximum V_{PL} must be matched to the worst case output power and then reduced by 1 dB when the PCF5077T is used in closed loop mode.

Curve 2 in Fig.9 shows what happens when the PA is driven into saturation. The down-ramping of the power is getting too steep and therefore the transient spectra will be too wide. The 1 dB margin is necessary because of the flat PA control curve at high power level. The loop needs more time to reduce the power during the down-ramping and the control voltage increases. The high control voltage forces the power quickly down when the steep region of the control curve is achieved. The steep down-ramping results in a wide transient spectra.

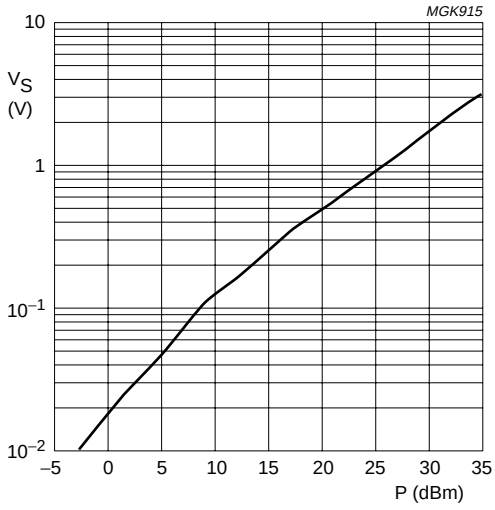
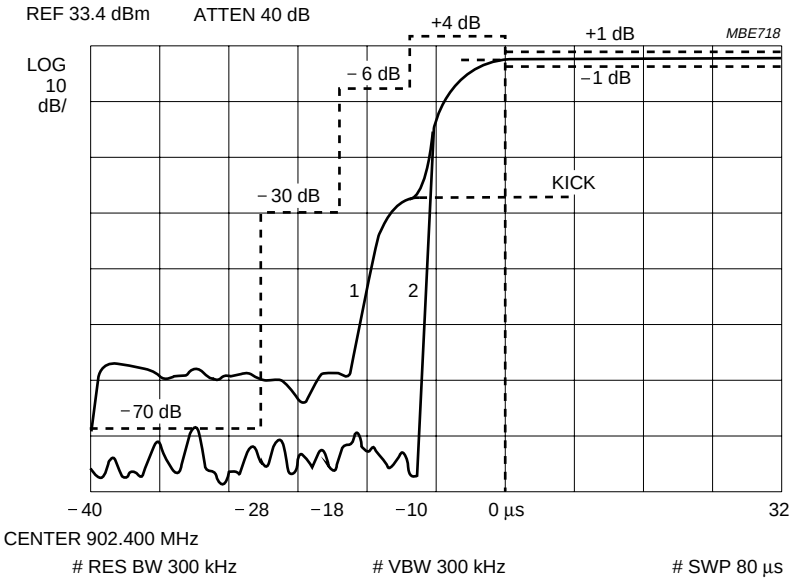
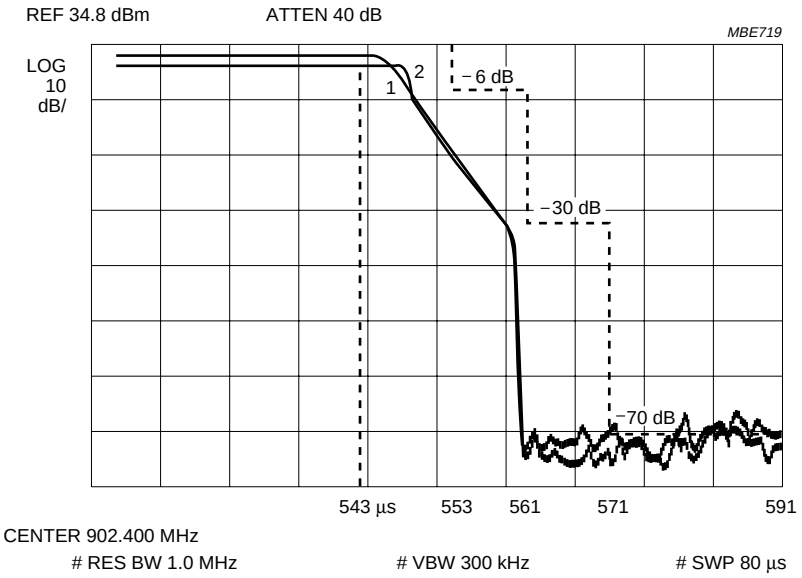


Fig.7 Sensor voltage as a function of output power (diode BAT62).



(1) Highest usable value.
(2) Lowest usable value.

Fig.8 Power as a function of time; rising edge (behaviour at different worst case home positions of $V_{INT(O)}$).



(1) Correct behaviour.
(2) Unusable behaviour with wrong V_{PL} value.

Fig.9 Power as a function of time; falling edge.

Application in mobile stations

Using a directional coupler with 16.5 dB attenuation produces a sensor signal between 100 mV and 3 V below the diode forward voltage at pin VS for the PA output power range of 8 to 36 dBm.

The sensor voltage of 3 V at pin VS corresponds to the maximum DAC output voltage. The power range that can be controlled is therefore not limited by the sensor voltage input VS and higher power levels can be controlled with the control loop switched on.

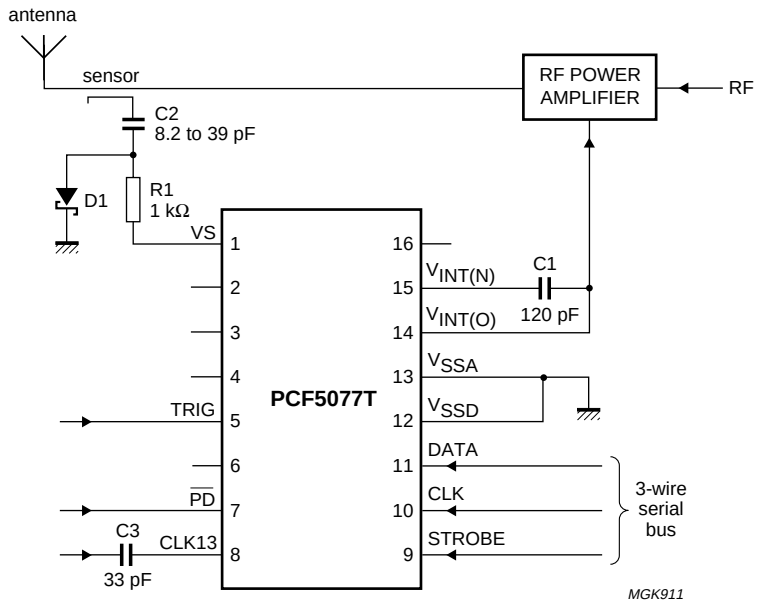
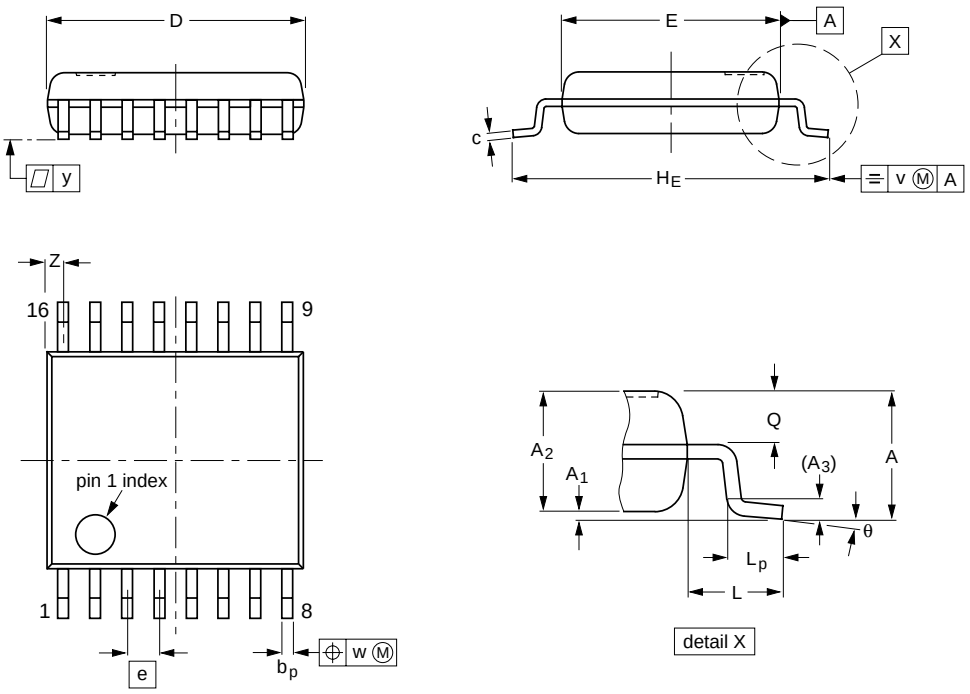
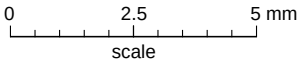


Fig.10 Application diagram for mobile stations.

PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						~~94-04-20~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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