iT6145
Duobinary Encoder and Driver Amplifier
(Preliminary Information)

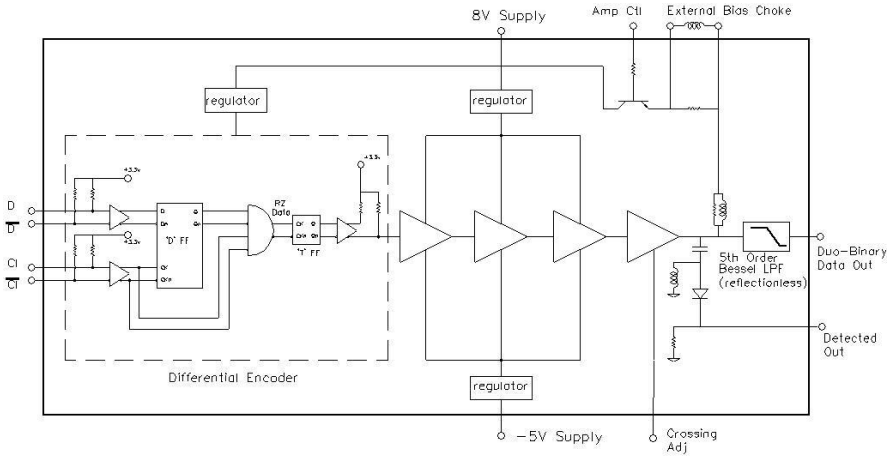
Description

The iT6145 combines a duobinary encoder, driver amplifier, and fifth-order Bessel low-pass filter in a compact module. It is designed for use in the transmitters (transponders) of long-haul duobinary optical communication links. The microchip module is suitable for use in standard 300-pin MSA modules and is housed in a rugged enclosure. The output of the iT6145 is a duobinary encoded signal with the correct bandwidth and amplitude to directly drive a M-Z optical modulator. The output level is adjustable from 5 to 9 Vpp to allow for variations in modulator Vpi. An internal detector provides a temperature-stable DC voltage that is proportional to the output data amplitude, facilitating the use of AGC loops to set the output level. The clock and data inputs can be driven either differentially for maximum sensitivity, or single ended with the unused inputs terminated in 50 ohms.

Features

- ❖Complete, compact duo-binary transmitter solution
- ❖Adjustable output voltage from 5.0 to 9.0 Vpp
- ❖Power dissipation: 5 W
- ❖16-mm SMT ceramic package with bottom pad grounding and heat sinking
- ❖Differential data and clock inputs
- ❖Integral output level detector for AGC loop control

Device Diagram



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
Vsig_max	Clock/data input	Vcc-2	Vcc+0.6	V
V8_max	+8 VDC supply input		10	V
V-5_max	-5 VDC supply input	-10		V
Tc_max_op	Case temperature (operating)		75	ºC
Tc_max_st	Storage temperature		125	ºC

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Electrical Characteristics

At ambient temperature

#	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
1	Input data rate	DIN_dr		9.9		11.1	Gb/s
2	Input clock frequency	CLK_f		9.9		11.1	GHz
3	Input amplitude (clock and data)	Vin_pp	Differential	0.3		1.0	Vpp
4	Data-clock phase margin	PH_d-c	Jitter degradation from optimum setting of TBD ps	TBD			ps
5	Long pulse droop (from low-frequency-cutoff)	DROOP	Vout at end of pulse Vout at start of 1 µs pulse		0.46		
6	Maximum output voltage amplitude	Vout_max	Level adjust control set for max.	9.0			Vpp
7	Minimum output voltage amplitude	Vout_min	Level adjust control set to min.			5.0	Vpp
8	Power detector output	Vdet	7 Vpp output		-170		mV
9	Level adjust input	V_amp			5 to 12		V
10	8 V supply current	+8 V	Output set to 9 Vpp			600	mA
11	-5.0 V supply	-5 V	Output set to 9.0 Vpp			40	mA

Eye Specifications

1. See Jitter Definition (p. 3).
2. See Eye Skew Definition (p. 3).
3. See Eye Opening Definition (p. 3)
+1EO = Va/Vb*100.
4. See Eye Opening Definition (p. 3)
-1EO = Vc/Vd*100.
5. See Half Clock Amplitude Ratio Definition (p. 3)
F/2_rat = Va/Vb.

#	Parameter	Symbol	Min.	Typ.	Max.	Unit
1	+1 jitter (note 1)	J+1			20	ps p-p
2	-1 jitter (note 1)	J-1			20	ps p-p
3	0 jitter (note 1)	J0		25		ps p-p
	Skew (note 2)	Skew			5	ps
	+1 level eye opening (note 3)	+1EO		65		%
	-1 level eye opening (note 4)	-1EO		65		%
	Half clock ratio (note 5)	f/2_rat		0.3	0.4	%

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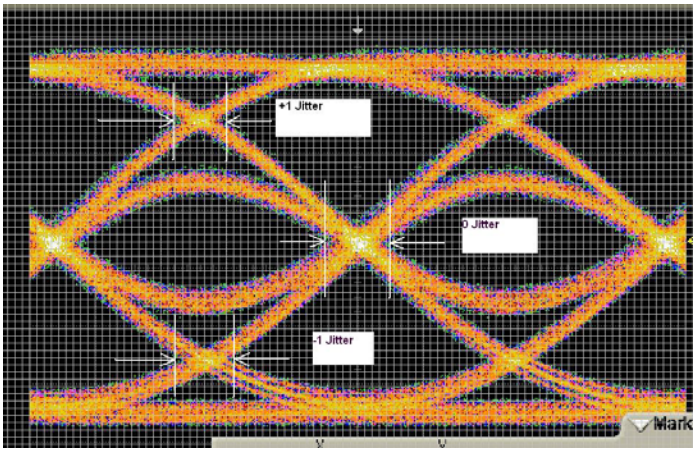
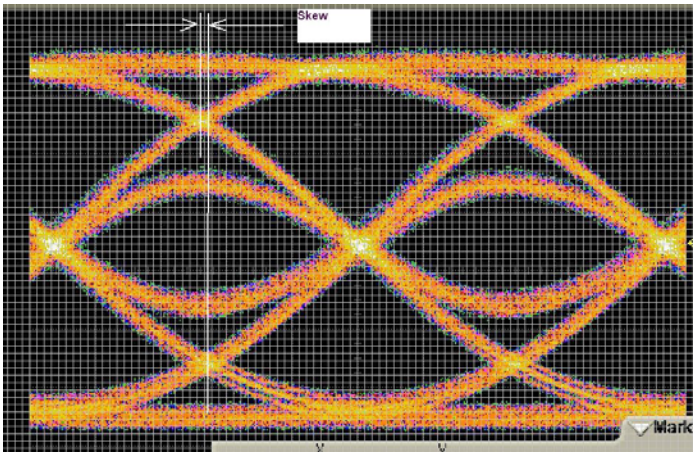
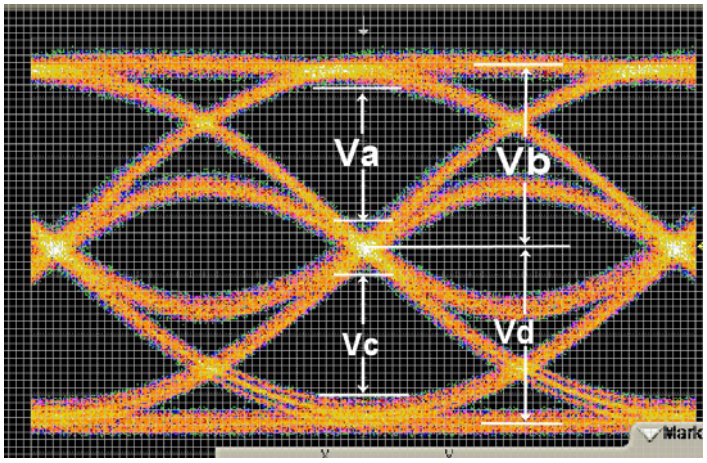
Jitter Definitions



Eye Skew Definitions



Eye Opening Definitions



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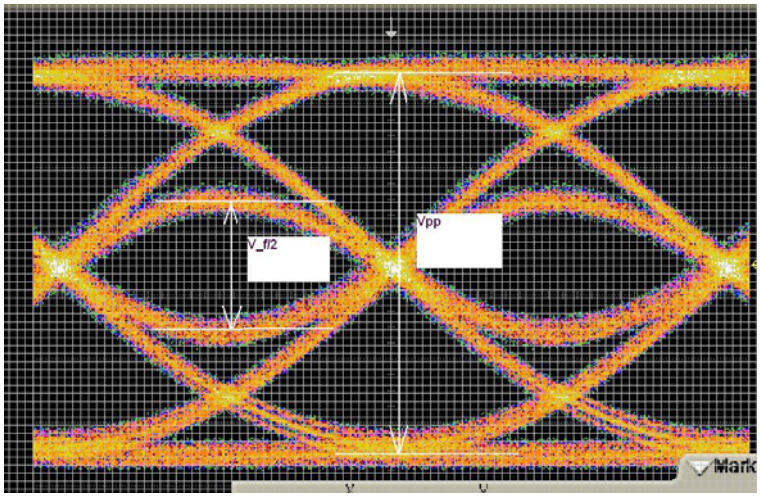
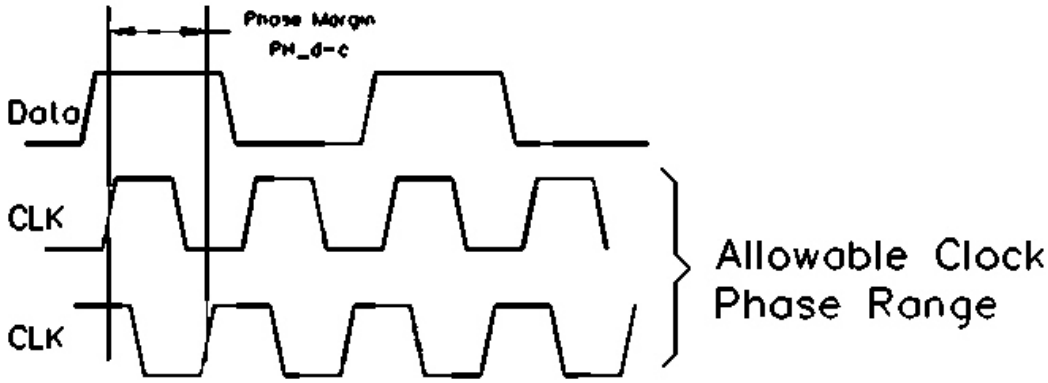
Half-Clock Amplitude Ratio Definition



Timing Diagram



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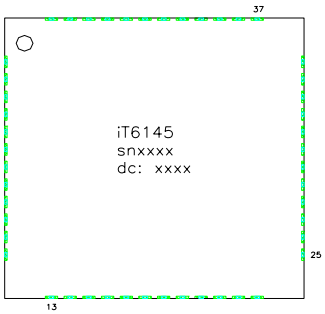
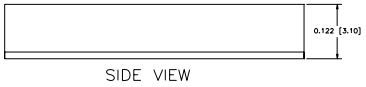
Chip Dimensions And Pinouts



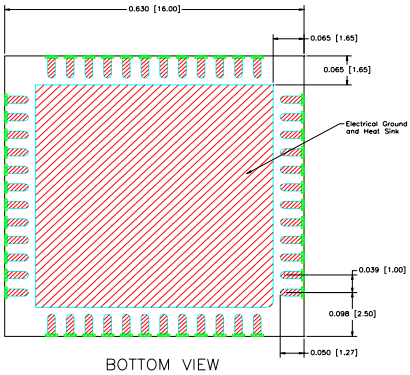
Top VIEW

Pin Assignment:

1, 2, 3, 5, 7, 9, 11, 12 13, 14, 15, 16, 17, 18 19, 20, 21, 22, 23, 25 26, 27, 28, 29, 31, 33 34, 35, 36, 37, 38, 39 41, 43, 45, 47, 48	gnd
4	data in
6	data/ in
8	cl in
10	cl/ in
24	−5V
30	data out
32	det out
40	BI (to external choke)
42	BO(to external choke)
44	VC
46	+8V



SIDE VIEW



BOTTOM VIEW

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