

### General Description

The AAT7103 25V N-Channel Power MOSFET is a member of AnalogicTech™'s TrenchDMOS™ product family. Using the ultra-high density proprietary TrenchDMOS technology, the product demonstrates high power handling and small size.

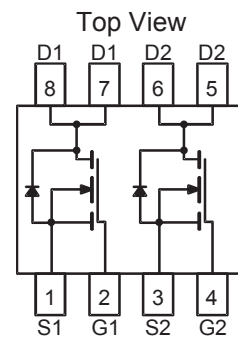
### Features

- $V_{DS(MAX)} = 25V$
- $I_{D(MAX)}^{(1)} = 6.8 A @ 25^{\circ}C$
- Low  $R_{DS(ON)}$ :
  - $26 m\Omega @ V_{GS} = 4.5V$
  - $41 m\Omega @ V_{GS} = 2.5V$

### Applications

- Battery Packs
- Cellular & Cordless Telephones
- PDAs, Camcorders, and Cell Phones

### Dual SOP-8 Package



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### Absolute Maximum Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

Symbol	Description	Value	Units
$V_{DS}$	Drain-Source Voltage	25	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	
$I_D$	Continuous Drain Current @ $T_J=150^{\circ}C$ <sup>1</sup>	$T_A = 25^{\circ}C$	$\pm 6.8$
		$T_A = 70^{\circ}C$	$\pm 5.4$
$I_{DM}$	Pulsed Drain Current <sup>3</sup>	$\pm 24$	A
$I_S$	Continuous Source Current (Source-Drain Diode) <sup>1</sup>	1.8	
$P_D$	Maximum Power Dissipation <sup>1</sup>	$T_A = 25^{\circ}C$	2.0
		$T_A = 70^{\circ}C$	1.25
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^{\circ}C$

### Thermal Characteristics

Symbol	Description	Value	Units
$R_{\theta JA}$	Typical Junction-to-Ambient steady state, one FET on <sup>2</sup>	100	$^{\circ}C/W$
$R_{\theta JA2}$	Maximum Junction-to-Ambient Figure, $t < 10$ sec. <sup>1</sup>	62.5	$^{\circ}C/W$
$R_{\theta JF}$	Typical Junction-to-Foot, one FET on <sup>1</sup>	35	$^{\circ}C/W$

### Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Description	Conditions	Min	Typ	Max	Units
<b>DC Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	25			V
R <sub>DS(ON)</sub>	Drain-Source ON-Resistance <sup>3</sup>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =6.8A		19	26	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =5.4A		28	41	
I <sub>D(ON)</sub>	On-State Drain Current <sup>3</sup>	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =5V (Pulsed)	24			A
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	0.6			V
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±12V, V <sub>DS</sub> =0V			±100	nA
I <sub>DSS</sub>	Drain Source Leakage Current	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V			1	μA
		V <sub>GS</sub> =0V, V <sub>DS</sub> =20V, T <sub>J</sub> =70°C			5	
g <sub>fs</sub>	Forward Transconductance <sup>3</sup>	V <sub>DS</sub> =5V, I <sub>D</sub> =6.8A		20		S
<b>Dynamic Characteristics <sup>4</sup></b>						
Q <sub>G</sub>	Total Gate Charge	V <sub>DS</sub> =15V, R <sub>D</sub> =2.2Ω, V <sub>GS</sub> =4.5V		13	19	nC
Q <sub>GS</sub>	Gate-Source Charge	V <sub>DS</sub> =15V, R <sub>D</sub> =2.2Ω, V <sub>GS</sub> =4.5V		1.9		
Q <sub>GD</sub>	Gate-Drain Charge	V <sub>DS</sub> =15V, R <sub>D</sub> =2.2Ω, V <sub>GS</sub> =4.5V		2.9		
t <sub>D(ON)</sub>	Turn-ON Delay	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>D</sub> =2.2Ω, RG=6Ω		15		ns
t <sub>R</sub>	Turn-ON Rise Time	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>D</sub> =2.2Ω, RG=6Ω		18		
t <sub>D(OFF)</sub>	Turn-OFF Delay	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>D</sub> =2.2Ω, RG=6Ω		36		
t <sub>F</sub>	Turn-OFF Fall Time	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>D</sub> =2.2Ω, RG=6Ω		27		
<b>Source-Drain Diode Characteristics</b>						
V <sub>SD</sub>	Source-Drain Forward Voltage <sup>3</sup>	V <sub>GS</sub> =0, I <sub>S</sub> =6.8A			1.5	V
I <sub>S</sub>	Continuous Diode Current <sup>1</sup>				1.8	A

Note 1: Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 10 second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in many applications. R<sub>θJF</sub> + R<sub>θFA</sub> = R<sub>θJA</sub> where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. R<sub>θJF</sub> is guaranteed by design; however, R<sub>θFA</sub> is determined by PCB design. Actual maximum continuous current is limited by the application's design.

Note 2: Steady state thermal response while mounted on a 1" x 1" PCB with maximum copper area is provided for comparison with other devices. This test condition approximates many battery pack applications.

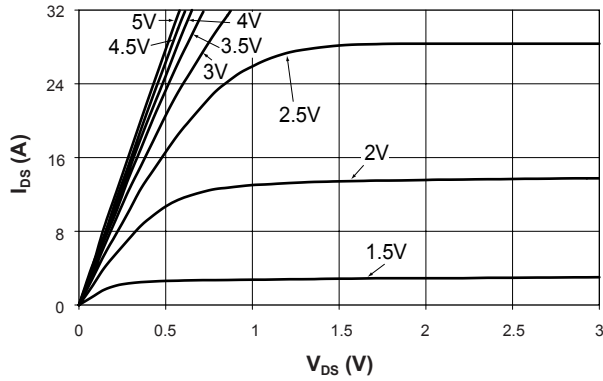
Note 3: Pulsed measurement 300 μs, single pulse.

Note 4: Guaranteed by design. Not subject to production testing.

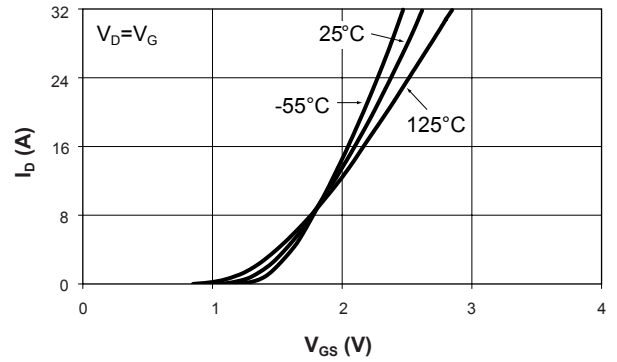
### Typical Characteristics

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

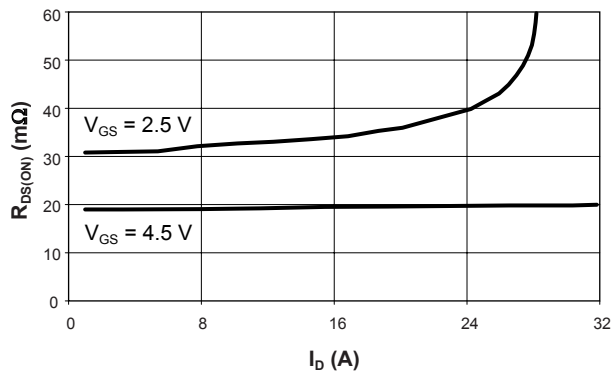
#### Output Characteristics



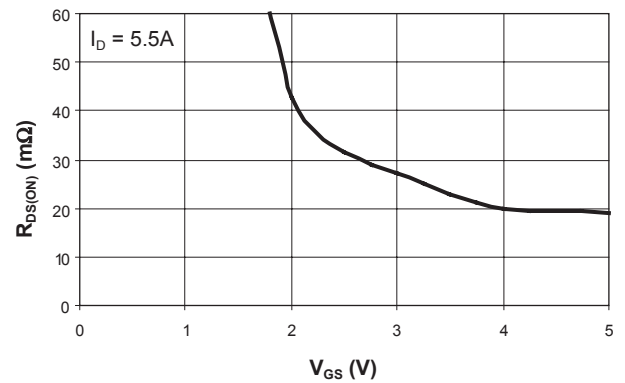
#### Transfer Characteristics



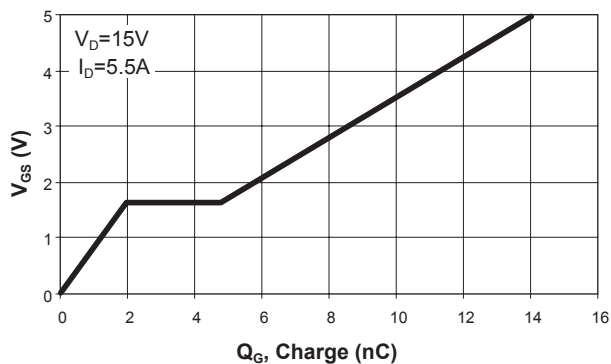
#### On-Resistance vs. Drain Current



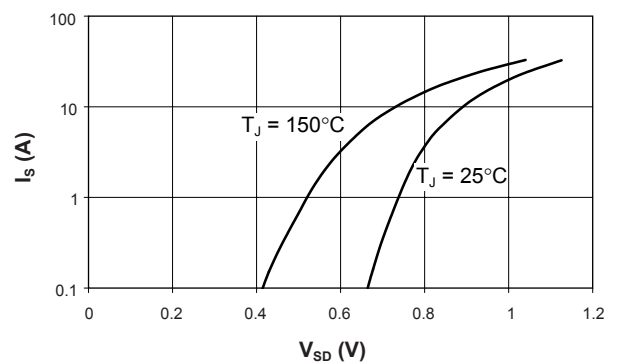
#### On-Resistance vs. Gate to Source Voltage



#### Gate Charge



#### Source-Drain Diode Forward Voltage

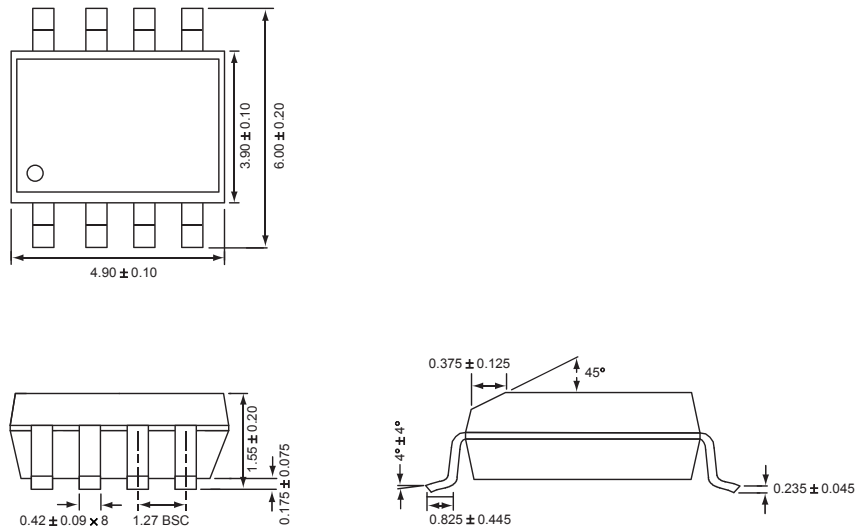


## Ordering Information

Package	Marking	Part Number (Tape and Reel)
SOP-8	7103	<b>AAT7103IAS-T1</b>

Note: Sample stock is generally held on all part numbers listed in **BOLD**.

## Package Information



All dimensions in millimeters.

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