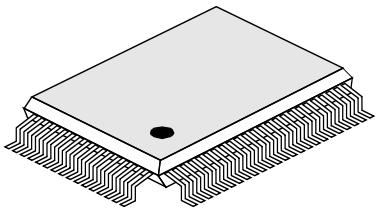
INTRODUCTION

The KS0125 is a multistandard video encoder with line interpolation, crisping circuits, and on-screen-display (OSD) functions. These special functions make this encoder well suited for MPEG playback applications, such as video compact disk (VCD), and digital video disk (DVD).

80–PQFP



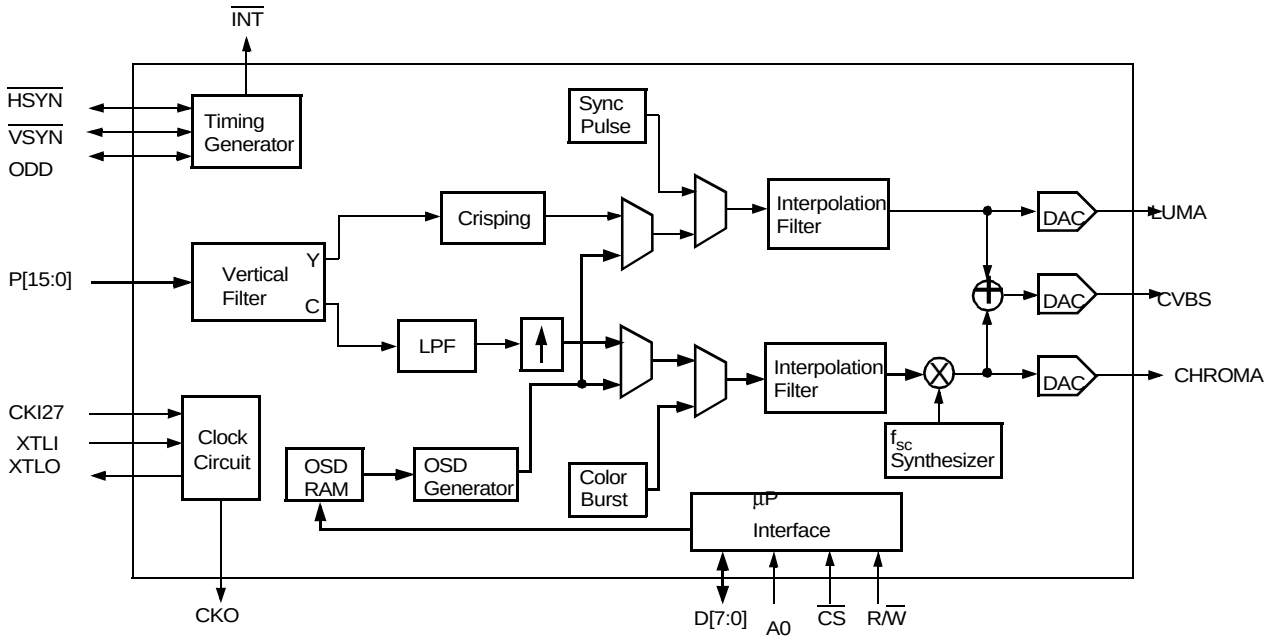
FEATURES

- Line interpolation
- Crisping circuit to enhance horizontal resolution and to reduce MPEG mosquito effect
- 250 character ROM containing the English and Japanese alphabets, Korean characters, numbers, and symbols.
- 4 user selectable OSD character colors and 2 background colors
- CCIR 601 or CCIR 656 input
- NTSC-M or PAL-B,G,H output
- Master or slave timing operation with EAV support for CCIR 656 input
- Adjustable hue
- 3 10-bit DACs for simultaneous CVBS and S-video output
- DACs support power-down mode

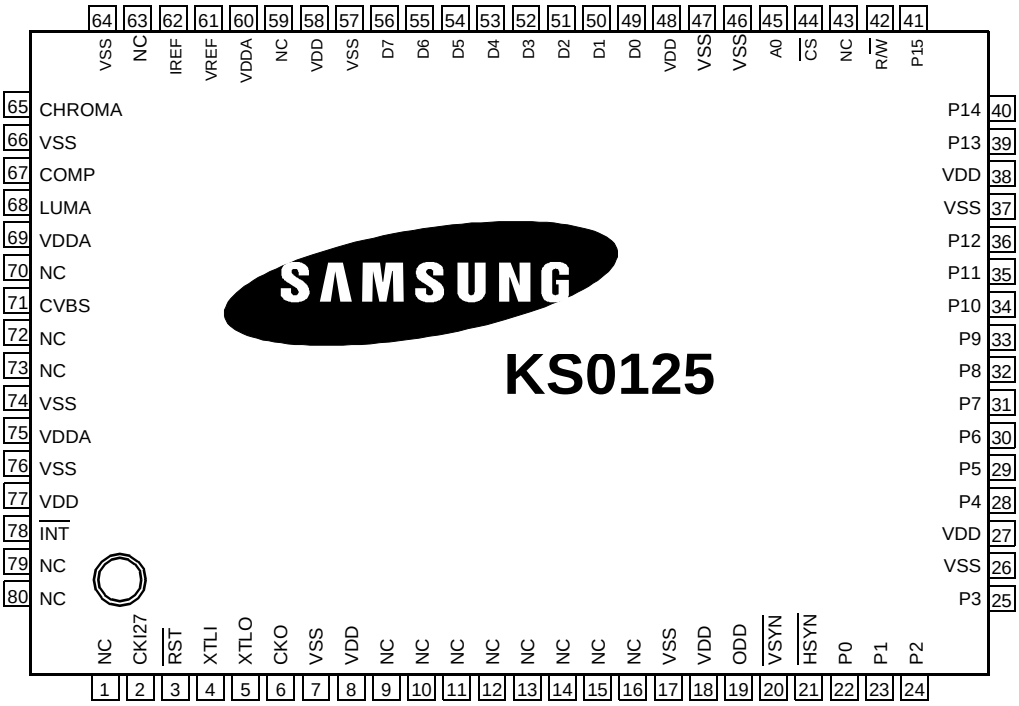
ORDERING INFORMATION

Device	Package	Operating Temperature
KS0125	80–PQFP	0 to +70°C

BLOCK DIAGRAM



PIN ASSIGNMENT- 80 PQFP



TYPICAL APPLICATION

The KS0125 is shown in a typical VCD or DVD application

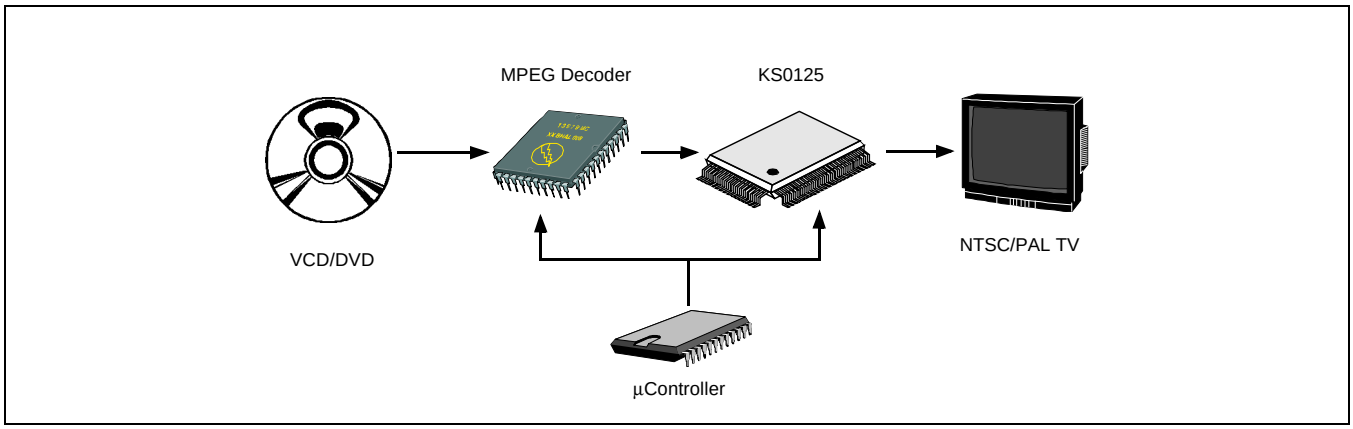


Figure 1. Typical Application

PIN CROSS REFERENCE: ORDER BY PIN NUMBER

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NC	21	HSYN	41	P15	61	VREF
2	CKI27	22	P0	42	R/$\overline{W}$	62	IREF
3	RST	23	P1	43	NC	63	NC
4	XTLI	24	P2	44	CS	64	VSS
5	XTLO	25	P3	45	A0	65	CHROMA
6	CKO	26	VSS	46	VSS	66	VSS
7	VSS	27	VDD	47	VSS	67	COMP
8	VDD	28	P4	48	VDD	68	LUMA
9	NC	29	P5	49	D0	69	VDDA
10	NC	30	P6	50	D1	70	NC
11	NC	31	P7	51	D2	71	CVBS
12	NC	32	P8	52	D3	72	NC
13	NC	33	P9	53	D4	73	NC
14	NC	34	P10	54	D5	74	VSS
15	NC	35	P11	55	D6	75	VDDA
16	NC	36	P12	56	D7	76	VSS
17	VSS	37	VSS	57	VSS	77	VDD
18	VDD	38	VDD	58	VDD	78	INT
19	ODD	39	P13	59	NC	79	NC
20	VSYN	40	P14	60	VDDA	80	NC

PIN DESCRIPTION

Pin Name	Pin Name	I/O	Description
DIGITAL VIDEO PORT			
P0 – P7	22 – 25, 28 – 31	I	For CCIR 601 data, these pins are the inputs for C0 – C7. For CCIR 656 data, these pins are the inputs for YC0 – YC7.
P8 – P15	32 – 36, 39 – 41	I	These pins are for CCIR 601 Y0 - Y7 inputs only.
CLOCK AND TIMING			
XTLI	4	I	13.5MHz crystal input, or 13.5 MHz CMOS clock input.
XTLO	5	O	13.5MHz crystal output.
CKI27	2	I	27MHz TTL clock input.
CKO	6	O	27MHz or 13.5MHz clock output(controlled by REGC bit4).
HSYN	21	I/O	Active low horizontal sync. It is an output in master mode; an input in slave mode(default).
VSYN	20	I/O	Active low vertical sync. It is an output in master mode; an input in slave mode(default).
ODD	19	I/O	Field flag. High for field 1; low for field 2. It is an output in master mode; an input in slave mode.
INT	78	O	Open drain, active low interrupt. It is triggered by the start of the vertical sync. Reset by software (VFLG bit0).
ANALOG VIDEO OUTPUT			
CVBS	71	O	Composite base band output(controlled by REGD bit5).
CHROMA	65	O	Chroma output(controlled by REGD bit6).
LUMA	68	O	Luma output(controlled by REGD bit6).
DAC REFERENCE AND COMPENSATION			
VREF	61	–	Voltage reference. The chip contains a 1.235 V internal band gap reference. Connect a 0.1 μF capacitor to VSSA.
IREF	62	–	Current reference. A resistor with a nominal value of 787 Ω should be connected to this pin and ground.
COMP	67	–	Compensation capacitor for the DAC internal reference amplifier. A 0.1 μF ceramic capacitor is required between this pin and ground.
HOST INTERFACE			
A0	45	I	Address line.
D0 - D7	49 - 56	I/O	Bidirectional data lines.
CS	44	I	Chip select strobe for data read and write.

PIN DESCRIPTION (Continued)

Pin Name	Pin Name	I/O	Description
R/$\overline{W}$	42	I	This pin controls the data flow direction when $\overline{CS}$ is low. A high indicates that the data is read from the chip. A low indicates the data is written to the chip.
RST	3	I	Active low chip reset.
POWER AND GROUND			
VDD	8, 18, 27, 38, 48, 58, 77	+5V	Digital power supply.
VDDA	60, 69, 75	+5V	Analog power supply.
VSS	7, 17, 26, 37, 46, 47, 57, 66, 74, 76	GND	Common ground.
NO CONNECT			
NC	1, 9 – 16, 43, 59, 62, 63, 70, 72, 73, 79, 80	–	These pins are reserved and should not be connected.

FUNCTIONAL DESCRIPTION

CLOCK INPUT AND OUTPUT

The KS0125 requires an external clock for its operation. It also outputs a clock (CKO) which can be used as a pixel clock for an external memory controller.

CLOCK INPUT

The KS0125 internally operates at 27 MHz. A 27 MHz TTL clock, a 13.5 MHz CMOS clock or a 13.5 MHz crystal can be used to supply the internal clock. Figure 4 shows the three possible external clock configurations. It is important that the unused clock input be grounded. The clock source should have no more than a 50 ppm frequency variation.

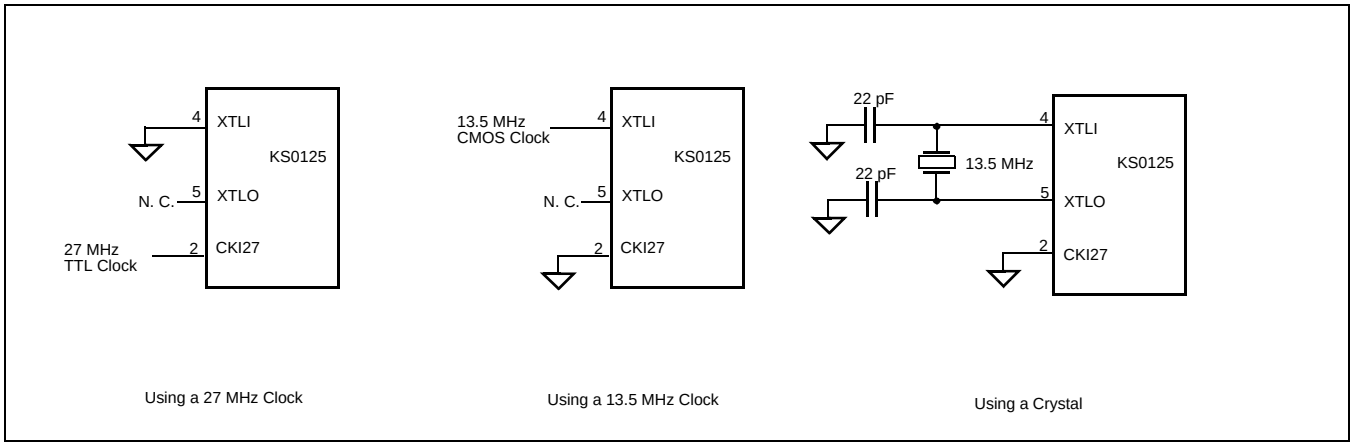


Figure 1. External Clock Configurations

CLOCK OUTPUT

The KS0125 provides an output clock (CKO) which can be used as a pixel clock. The frequency of the output clock can be either 27 MHz or 13.5 MHz, which is selected via the **CKOSL** bit in the **REGC** control register. Figure 2 shows the internal logic for this output clock

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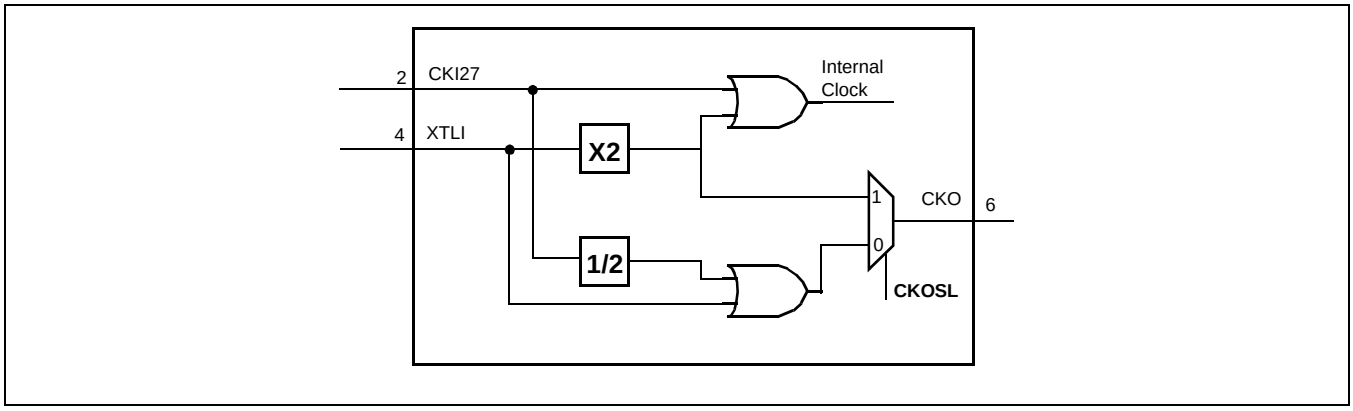

Figure 2. Output Clock Generation Logic

RESET

The KS0125 has a master reset pin $\overline{RST}$. This input is used to set the internal operation to a predefined state. During power up, the input on this pin must remain low until the power supply is stable. When the $\overline{RST}$ is low, all the control registers are set to their default values.

VIDEO TIMING

The KS0125 can operate in either master or slave timing mode. There are three bidirectional synchronization signals: HSYN, VSYN, and ODD. In master mode, these three signals are outputs. In slave mode, the KS0125 synchronizes to externally generated HSYN, and VSYN or ODD. For CCIR 656 format, the KS0125 will synchronize to the embedded EAV.

MASTER MODE TIMING

In master mode, the KS0125 generates three synchronization signals: $\overline{HSYN}$, $\overline{VSYN}$, and ODD. Depending on the field rate, the KS0125 generates different synchronization timings for 50 Hz and 60 Hz video. For 50 Hz video, Figure 1 shows the three synchronization signals during the vertical interval. For 60 Hz video similar timing is shown in Figure 7. Depending on which field is active, the $\overline{VSYN}$ transitions are either aligned to the falling edge of HSYN, or in the middle of a video line. ODD is always aligned to the falling edge of HSYN.

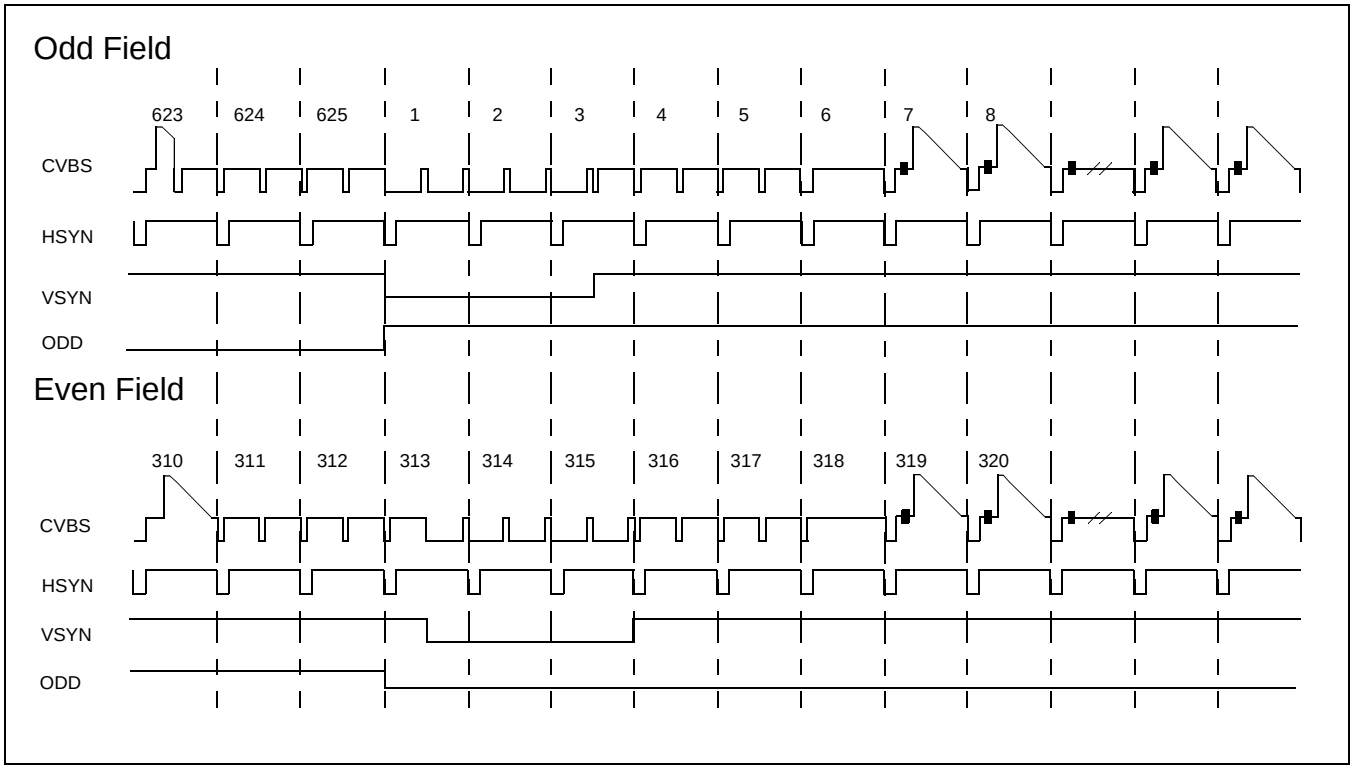

Figure 1. Synchronization Timings during Vertical Interval for 50 Hz Video

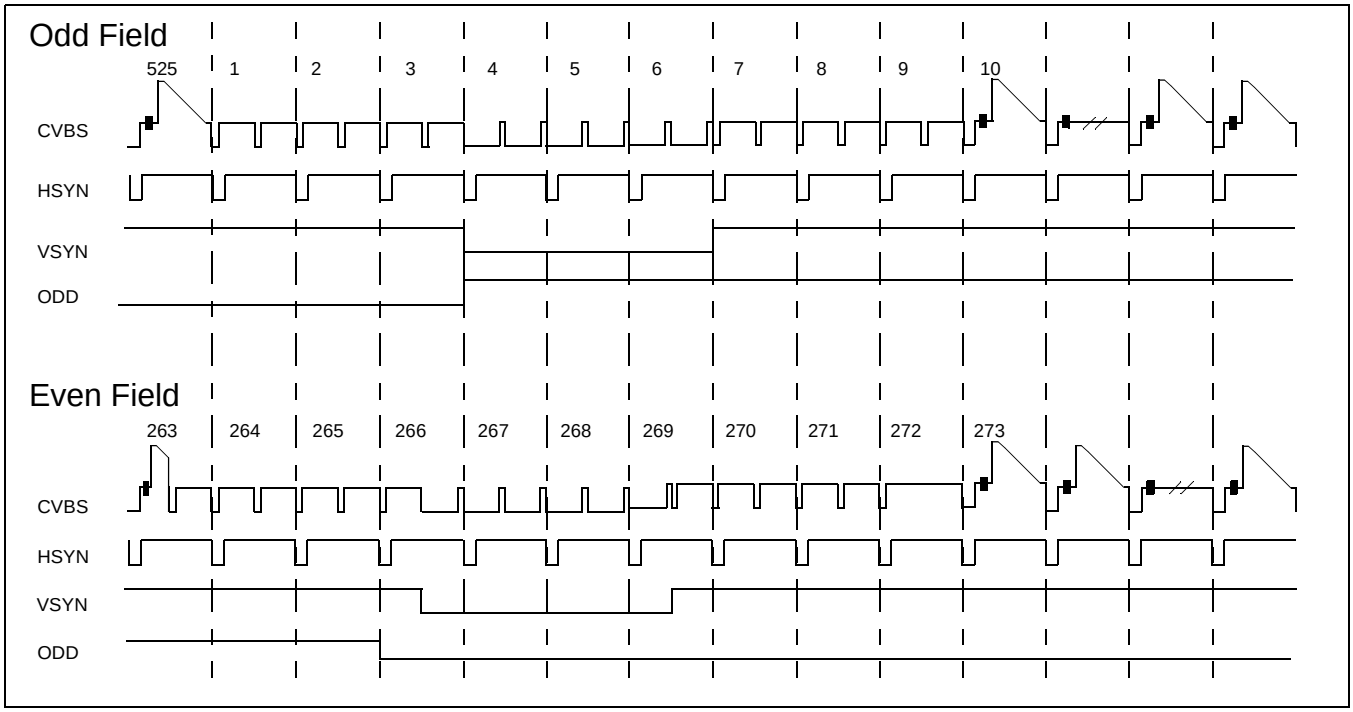

Figure 1. Synchronization Signals during Vertical Interval for 60 Hz Video.

Figure 2 shows the line timing. Note that the pulse width for $\overline{\text{HSYN}}$ is the same as the CVBS horizontal sync
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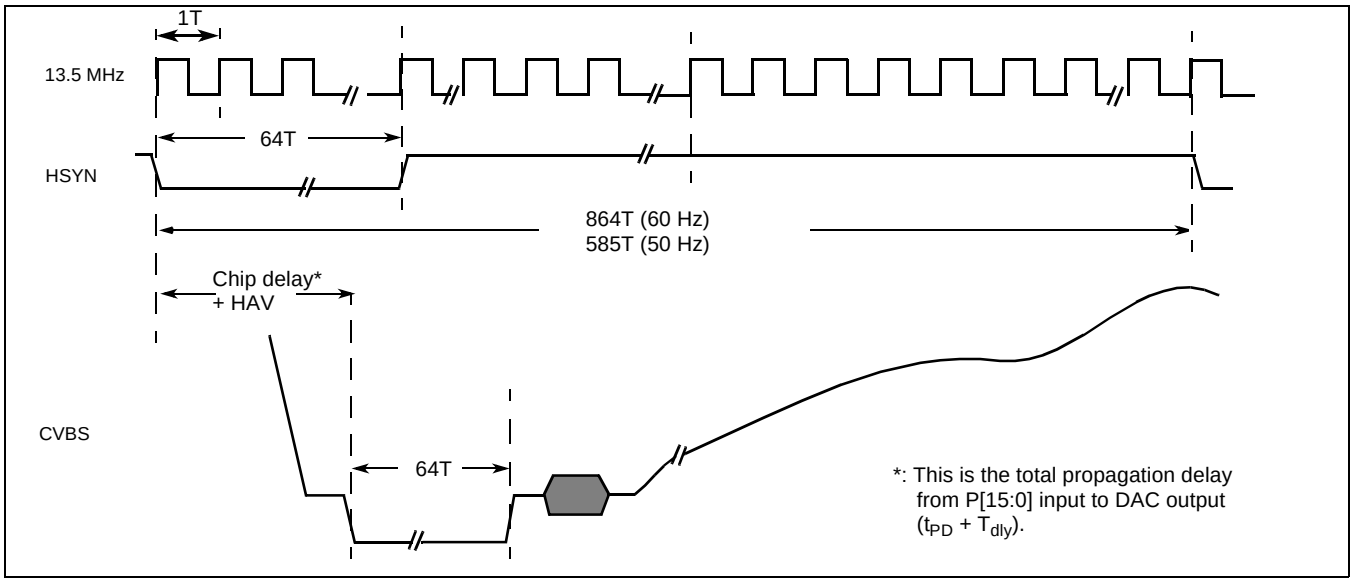

Figure 2. Video Line Timing

The active video input is synchronized to $\overline{\text{HSYN}}$. To accommodate external data latency, the phase between the start of the active video input and the leading edge of $\overline{\text{HSYN}}$ can be adjusted via **HAV[2:0]** in control register **REGD**, and **SHFHAV** in control register **REGE**. Pixel data alignment for 16 bit and 8 bit inputs are shown in Figure 3 and Figure 10, respectively.

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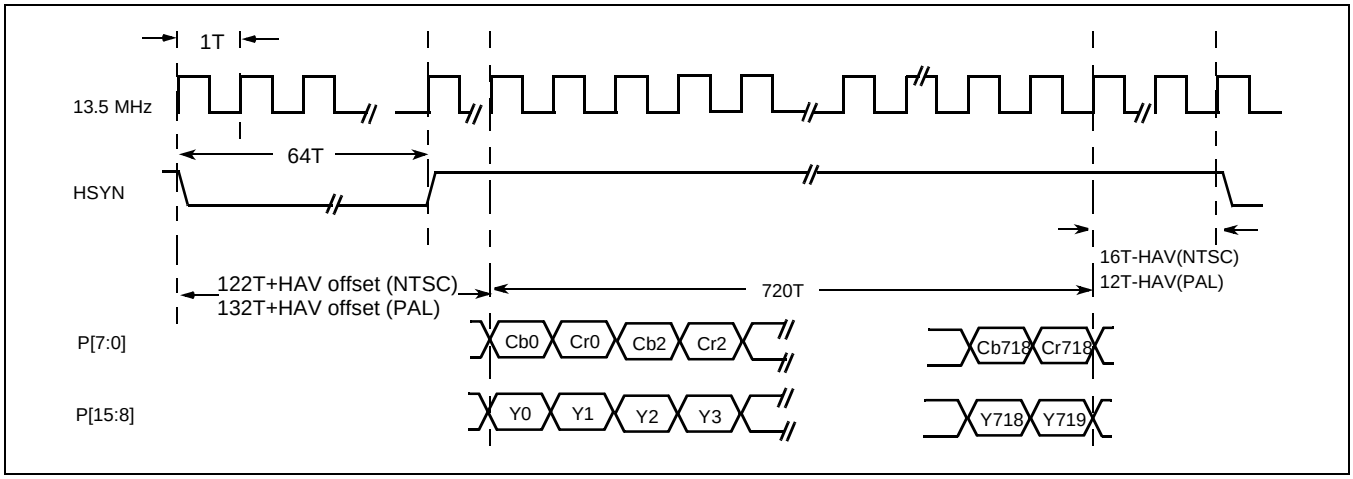

Figure 3. Pixel Data Alignment for 16 Bit Input

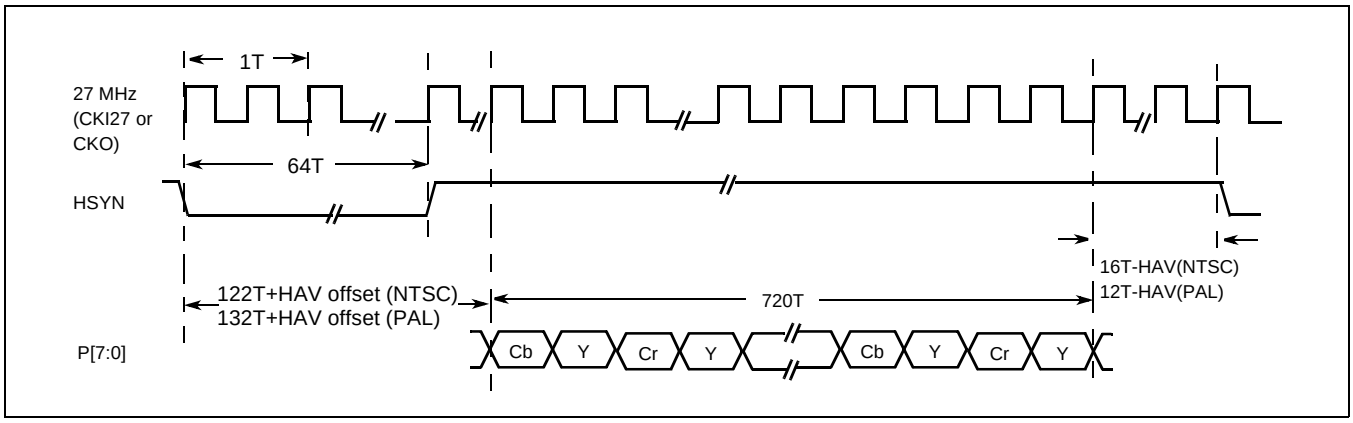

Figure 4. Pixel Data Alignment for 8 Bit Input

The reference point for pixel data setup and hold time is different for 27 MHz and 13.5 MHz clock inputs for 8 bit input data. If the 27 MHz clock input is used, the reference point is the rising edge of the CKI27 input. If the 13.5 MHz clock input is used, the reference point is the rising edge of the CKO output.

For CCIR 601 input, the setup and hold time is always referenced to the rising edge of the clock input.

SLAVE MODE TIMING

In slave mode operation, the KS0125 synchronizes to externally generated timing signals, or EAV timing reference codes embedded in the CCIR 656 data stream.

For CCIR 601 input, the internal horizontal timing counter is synchronized to the leading edge of the $\overline{\text{HSYN}}$ input. The KS0125 assumes the first active pixel input starts 122 pixel clocks (13.5 MHz) after the leading edge of $\overline{\text{HSYN}}$ for NTSC, or 132 pixel clocks for PAL. The line counter gets reset by the leading edge of VSYN. The internal field counter is synchronized to the leading edge of either VSYN or ODD input. The programmable **FLD** bit in the control

register **REGE** is used to select one of the two inputs for field synchronization.

For CCIR 656 input, synchronization is done through the EAV timing codes embedded in the digital video stream. The **EAV** bit in **REGE** must be set to a 1.

For 8-bit CbYCr input without EAV timing codes, The KS0125 synchronizes to the external timing signals. The **EAV** bit in **REGE** must be set to a 0.

If the KS0125 is programmed to use $\overline{\text{VSYN}}$ and $\overline{\text{HSYN}}$ for identifying the odd field (the **FLD** bit in **REGE** is set to a 0), the timing shown in Figure 11 must be met. If the falling edge of the $\overline{\text{VSYN}}$ falls outside of the window, the field is identified as an even field

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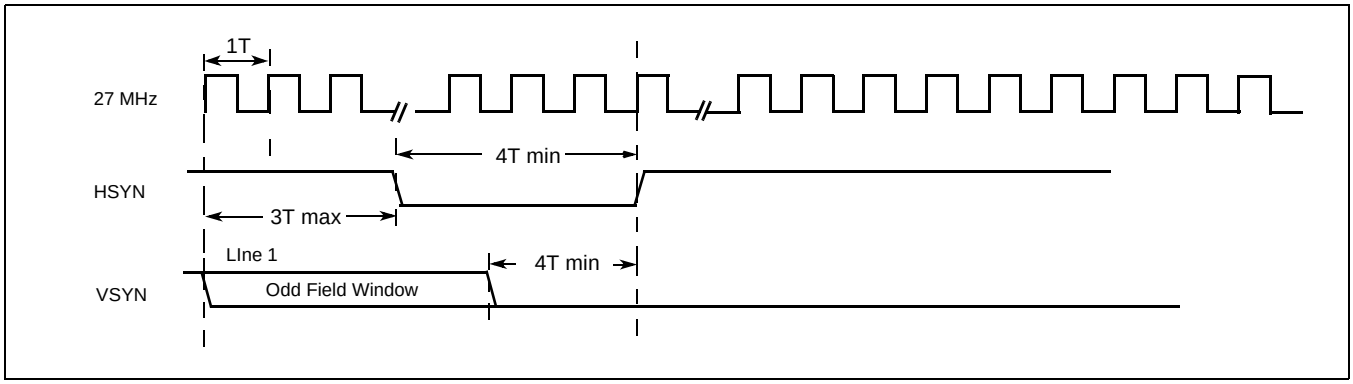

Figure 5. Identifying Field Using $\overline{\text{HSYN}}$ and $\overline{\text{VSYN}}$ in Slave Mode

DIGITAL DATA PATH AND SIGNAL PROCESSING

LUMINANCE DATA PATH

Figure 6 shows the functional block diagram for the luminance path

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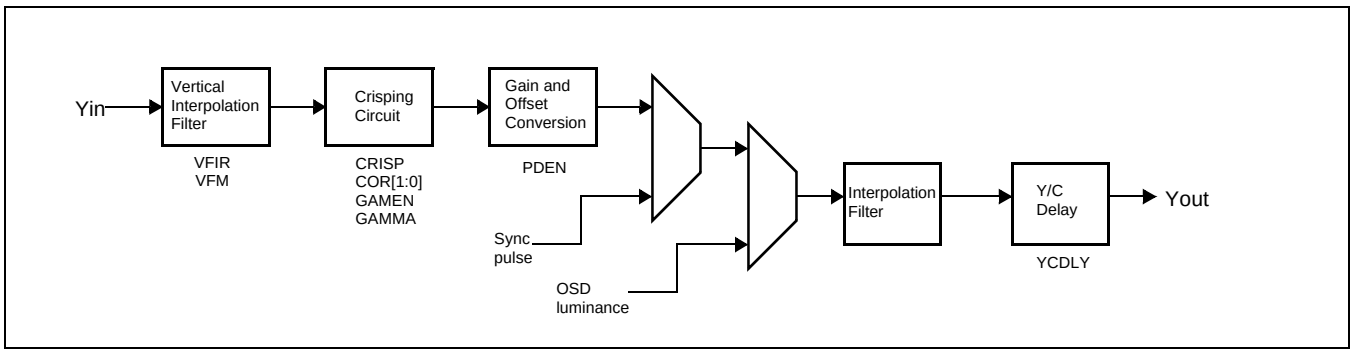

Figure 6. Luminance Processing Unit

The KS0125 has a field interpolation filter which is very useful for single field input sources, such as MPEG 1. For single field video sources, the KS0125 uses the input for the odd field without change. The even field is interpolated from the input. The interpolation filter employs a proprietary algorithm to create the even field which results in a smooth edge along diagonal and vertical directions. The vertical interpolation filter generates the current line output using the current and previous line inputs. Figure 13 shows how interlaced video is displayed on a CRT. The vertical interpolation filter generates a line using the lines above and below it in the other field. This requires that pixel data for the line below the interpolated line be the input when the interpolated line is generated. For example, if line 274 in Figure 13 is the line being interpolated, pixel data used for video line 12 (line n in the field buffer) must be the current input (Refer to Figure 1 and Figure 7 for video line definition)

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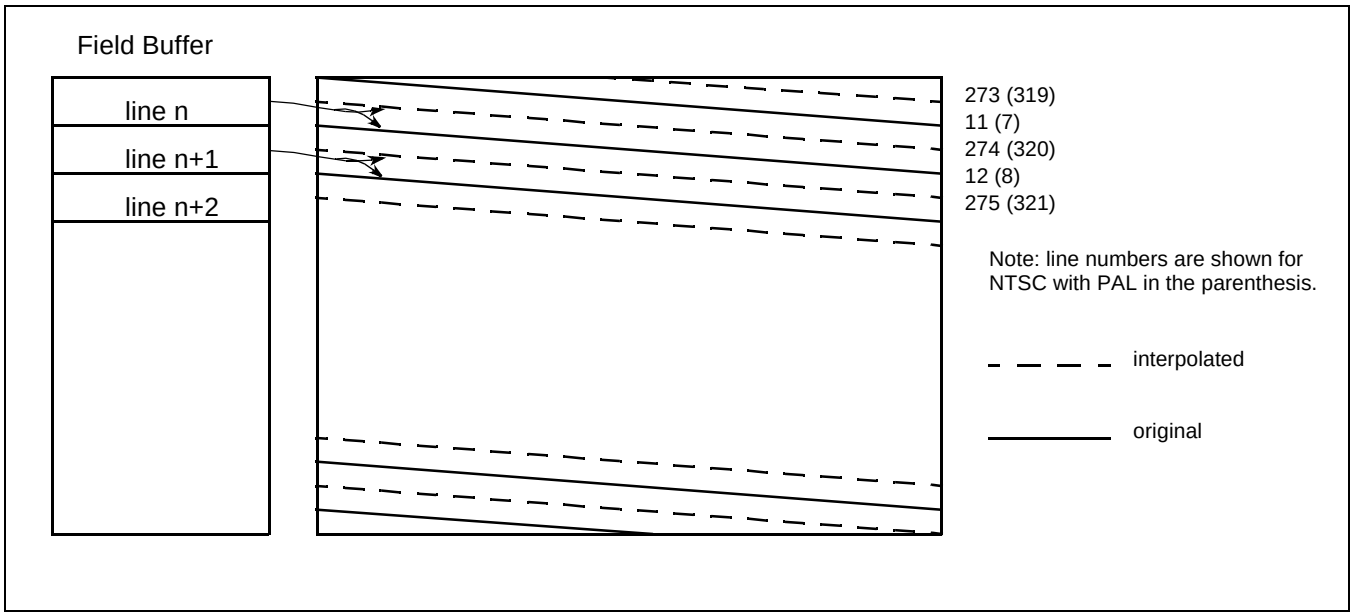

Figure 7. Field Interpolation Input Requirement

The crisping circuit further improves video quality. The crisping circuit is designed to reduce mosquito effect in MPEG 1 video. The functional block diagram is shown in Figure 8. It consists of a band separation circuit, a coring circuit, and a gamma correction ROM. The Y data is first separated into high and low frequency components. The high frequency component's low amplitude signals can optionally be suppressed by the coring circuit. The amplitude can be binary codes 1, 3, or 6, which is selected by programming the **COR[1:0]** bits in **REGA**. An additional gamma ROM can apply gamma correction to the high frequency component after the coring function. Two selections are provided for gamma correction. One has large peaking (**GAMMA** in **REGA** is set to a 1); the other has small peaking (**GAMMA** is set to a 0). The gamma correction can be disabled by programming the **GAMEN** bit in **REGA** to a 0. Finally, the high and low frequency components are recombined
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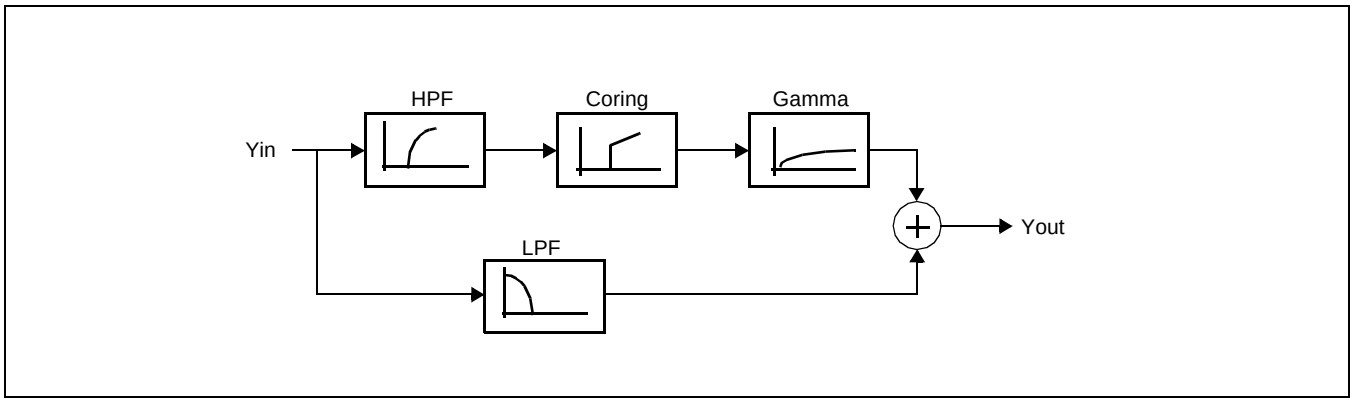

Figure 8. Crisping Circuit Block Diagram

The luminance data is gain and offset adjusted so its output will be at the correct NTSC or PAL level. The sync and OSD are inserted after the gain and offset conversion stage.

Before going to the DAC, the luminance data is interpolated to 27 MHz. This up sampling will simplify the external analog reconstruction filter. Figure 9 shows the characteristic of the interpolation filter. An optional one pipe line delay is also included to compensate for any YC delay in the reconstruction filter

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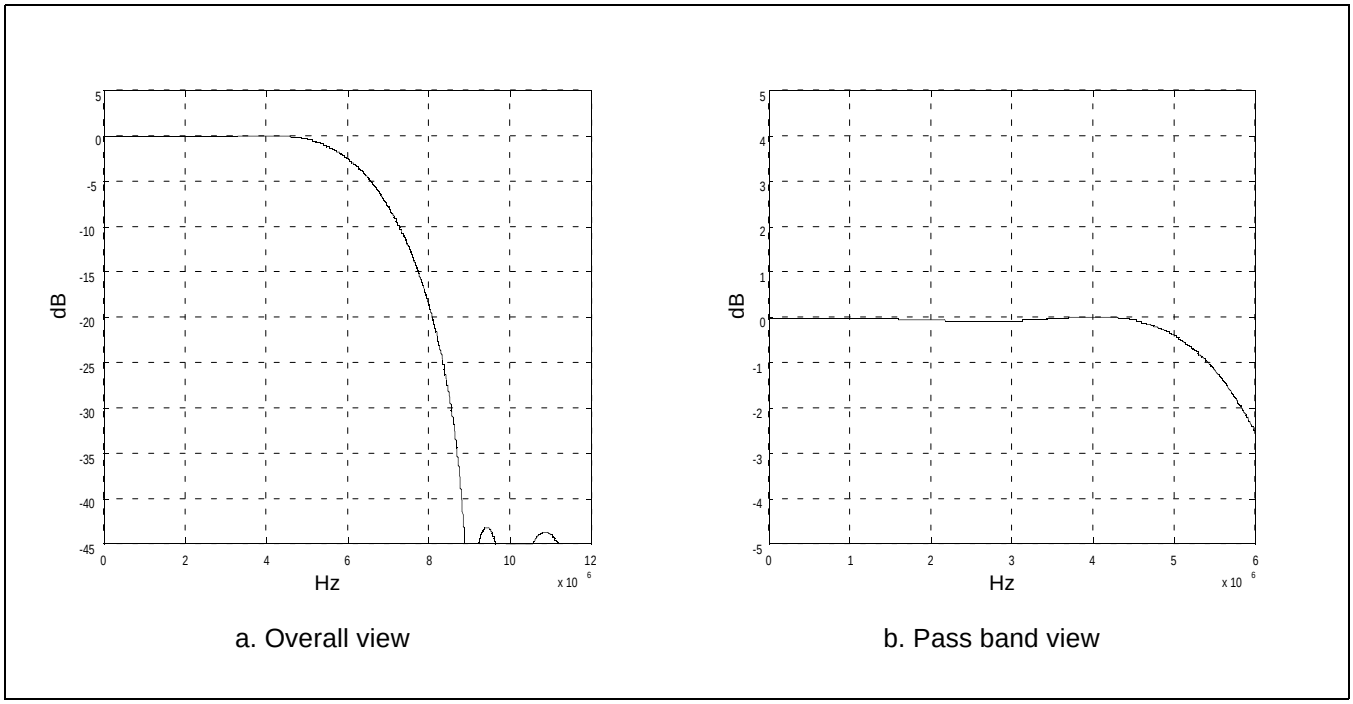

Figure 9. Luminance Pixel Interpolation Filter Characteristic

Chrominance Data Path

Figure 10 is the functional block diagram for the chrominance data path

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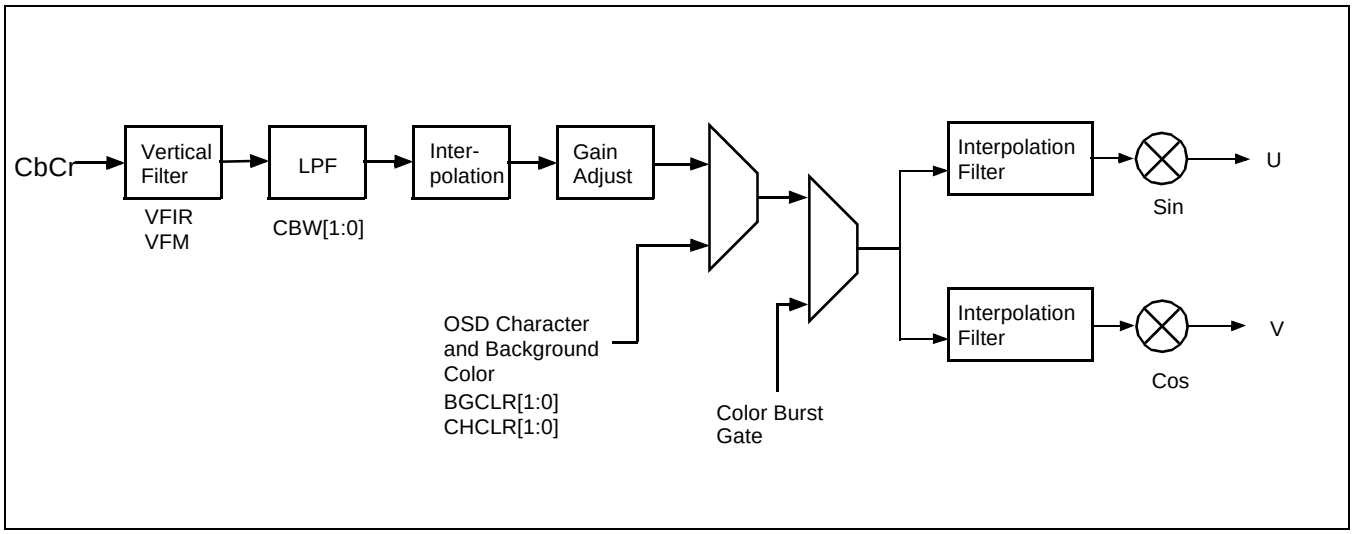

Figure 10. Chrominance Data Path

The chrominance path also contains a field interpolation filter which serves the same purpose as the field interpolation filter in the luminance path. Both luma and chroma field interpolation filters are controlled by the two register bits **VFIR** and **VFM**.

The chrominance data passes through a low pass filter whose bandwidth can be controlled via **CBW[1:0]** in **REGA**. The bandwidth can be 1.1 MHz, 1.45 MHz, or 1.75 MHz.

The Cb/Cr data is interpolated from 6.75 MHz to 13.5 MHz, and then gain adjusted. The Cb/Cr data is then demultiplexed to Cb and Cr paths.

OSD character and background colors are inserted into the Cb and Cr data paths. Two background colors (blue and black) or transparent background can be selected through **BGCLR[1:0]**, and four character colors (white, cyan, green, and magenta) can be selected via **CHCLR[1:0]**, both in **REGB**.

The color burst gate is inserted and the 13.5 MHz Cb and Cr data are up sampled to 27 MHz through an interpolation filter. Finally, the two color difference components are quadrature modulated by an internally generated subcarrier.

The overall frequency response of the chrominance path is shown in Figure 11
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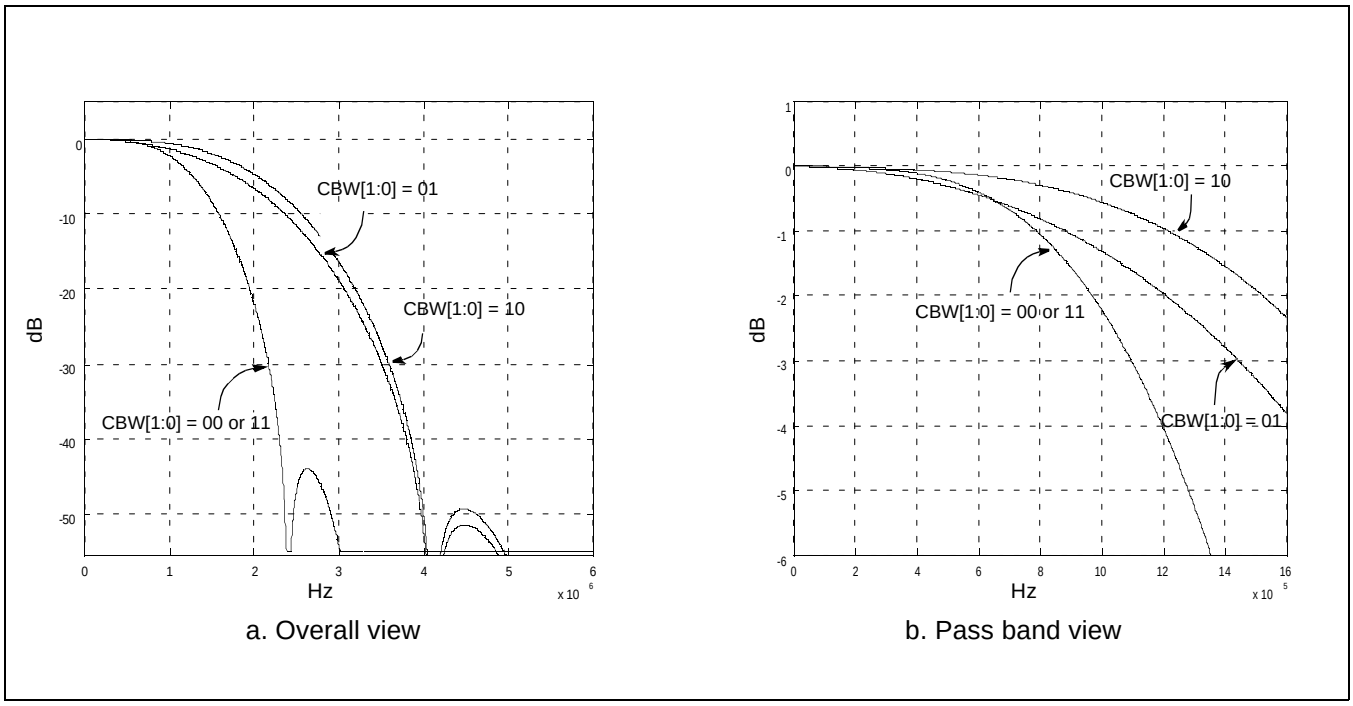

Figure 11. Chrominance Path Overall Frequency Response

ON-SCREEN-DISPLAY (OSD)

The On Screen Display (OSD) allows the user to Overlay characters over the video. The desired characters and their positions are programmed on the display screen via the 8-bit micorprocessor interface. Figure 15 shows a block diagram of the OSD. The OSD block consists of a character display buffer RAM,a character-generation font ROM,character location generation,character boundary location generation and OSD shaping circuits. The Timing Generator Pixel Counter and Line counter of the KS0125 generate controls to define the OSD display area.The RAM address defines where the character will be displayed. The RAM data output acts as the pointer to select a particular character from the Character font ROM. The character location generator converts the 12-bit character font ROM outputs to serial character streams, while the boundary location generator creates a boundary to surround the character. Finally,the OSD shaping circuits performs character color selection and background color selection. The OSD CB,CR and Y outputs are properly shaped by band-limited filters to reduce the ringing caused by the abrupt amplitude changes

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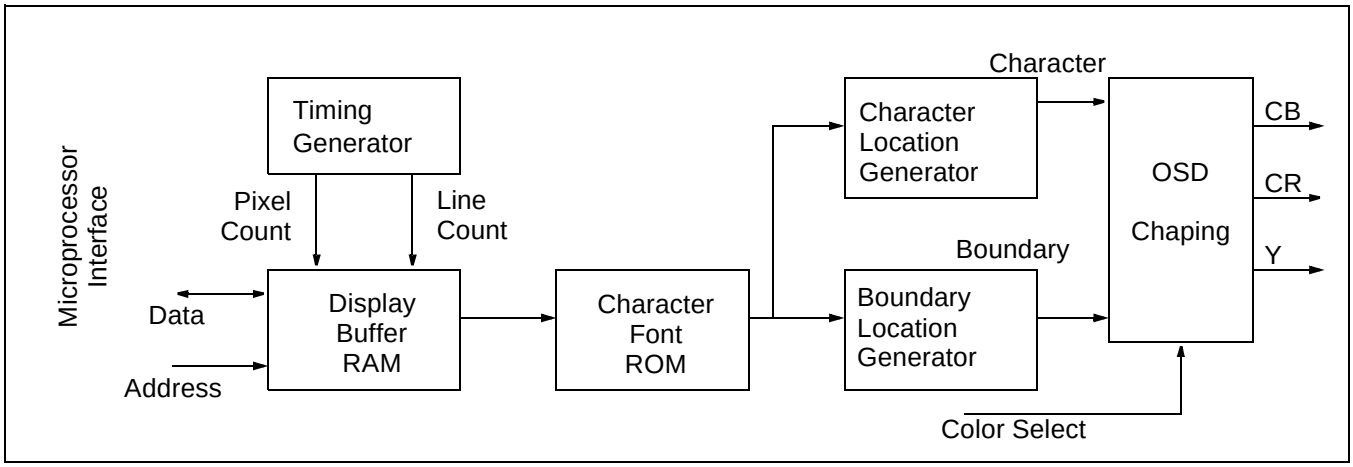

Figure 12. On Screen Display Block Diagram

OSD Color Selection And Background Color Selection

The OSD supports four different colors for the character display and two different background colors. The color select ion for the character and the background and the background are controlled by the programmable REGB control register . Tables 1 and 2 describle the OSD color selection and background color selection.

Notics that the user is recommended to choose the color white for the OSD character, bacause the KS0125 creates less flicking effect at the character boundary when white is chosen.

Table 1. OSD Character Color Selection

REGB BIT(6:5)	Color Selection	Comments
00	WHITE	Default, 80% Intensity
01	CYAN	80% Intensity, 60% Saturation
10	GREEN	80% Intensity, 60% Saturation
11	MEAENTA	80% Intensity, 60% Saturation

Table 2. OSD Background Color Selection

REGB BIT(6:5)	Background Color Selection	Comments
0X	WHITE	Character background is the video
10	GREEN	Video blanked
11	MEAENTA	Video blanked

OSD Display Area

The OSD display area is illustrated in figure 15-1. The starting and ending position in the horizontal direction are 176 and 786 in terms of pixel counts for both NTSC and PAL. The starting and ending position in the vertical direction are 41 and 241 for NTSC, and 47. Therefore, there are 200 scan lines for NTSC and 240 scan lines for PAL.

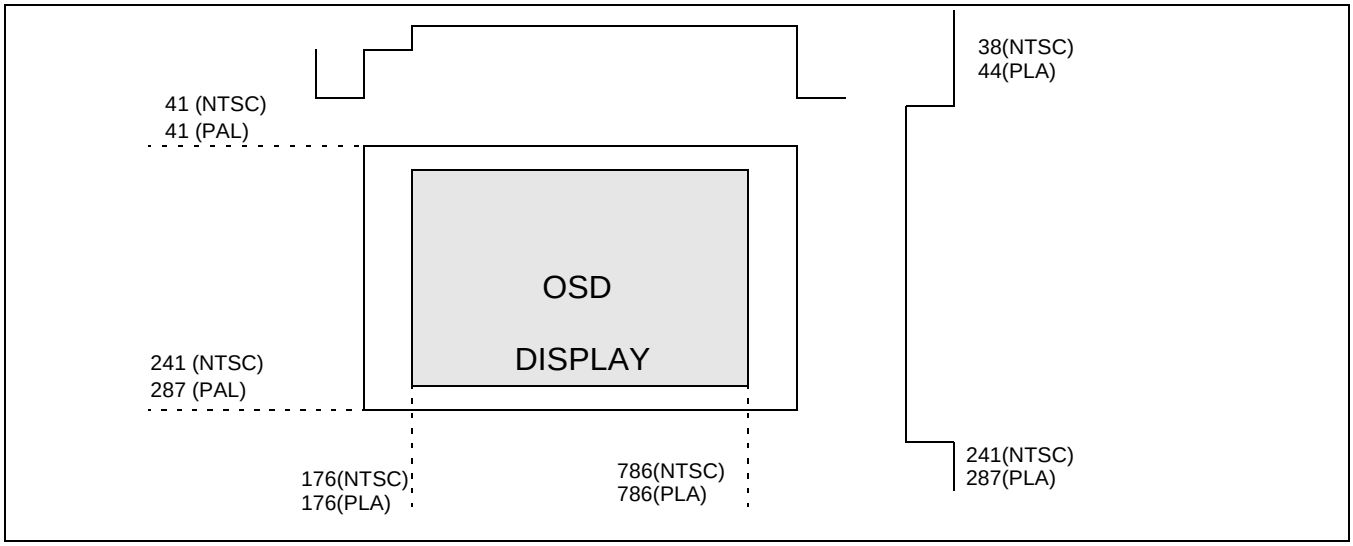

Figure 13. On Screen Display Area

OSD RAM Address

The OSD display area can fit in 25 characters in the horizontal direction and 10 characters in the vertical direction.The OSD RAM address is used to assign a location for a display character in the OSD display area. Table 3 describes the OSD RAM address and the character location mapping. Notice that the OSD RAM addresses between the On-Screen Lines are not continuously incremented. Instead, each On-Screen Line starts from address 32n in decimal, where n=0,1,2,....,9.

When programming the OSD, even though each OSD display line can hold 25 charactors (character 0 to character 24), the user is recommended to program an empty space (address 0AE Hex) for the last character for each OSD display line. This will avoid missing pixels at the last character position. In other words, the 25th character for each OSD line shall always be programmed as an empty space by using address 0AE for the OSD Font ROM.

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Table 3. OSD RAM Address Description

OSD RAM Address (HEXADECIMAL)	Character Location On Screen
000–018	On-Screen line1, character 0 to character 24
020–038	On-Screen line2, character 0 to character 24
040–058	On-Screen line3, character 0 to character 24
060–078	On-Screen line4, character 0 to character 24
080–098	On-Screen line5, character 0 to character 24
0A0–0B8	On-Screen line6, character 0 to character 24
0C0–0D8	On-Screen line7, character 0 to character 24
0E0–0F8	On-Screen line8, character 0 to character 24
100–118	On-Screen line9, character 0 to character 24
120–138	On-Screen line10, character 0 to character 24

OSD Font ROM

The OSD Font ROM contains a total of 250 characters. These character addresses are continuously incremented from 0 to 250 in decimal, (or 000 to 0F9 in hexadecimal).

Addressing The OSD Font Rom By The OSD RAM Data

The OSD RAM data is used as the character pointer to select a particular character from the OSD font ROM. Each character in the OSD Font ROM is designated to fit within a 10 x 12 dot matrix. The pointer only points to the top left corner bit of each character matrix. When a character is selected by the OSD RAM data during a display scan, the OSD ROM control circuitry will automatically generate all necessary addresses to go through all bit locations of the 10 x12 character matrix. Table 26 shows the contents of the OSD Font ROM,along with their address locations.

OSD Character Boundary

During the on screen display,the Boundary Location Generator generates a boundary to surround a character. The actual character size is 12 x 14 dot matrix. With the boundary surrounding a character, the character size becomes a 14 x 16 dot matrix.

Valid Time to Access the OSD RAM

There are two way to access the OSD RAM. One of them is using it when VFIG bit 7 is high. The other is using INT(pin # 78), as follows.

When INTEN=1

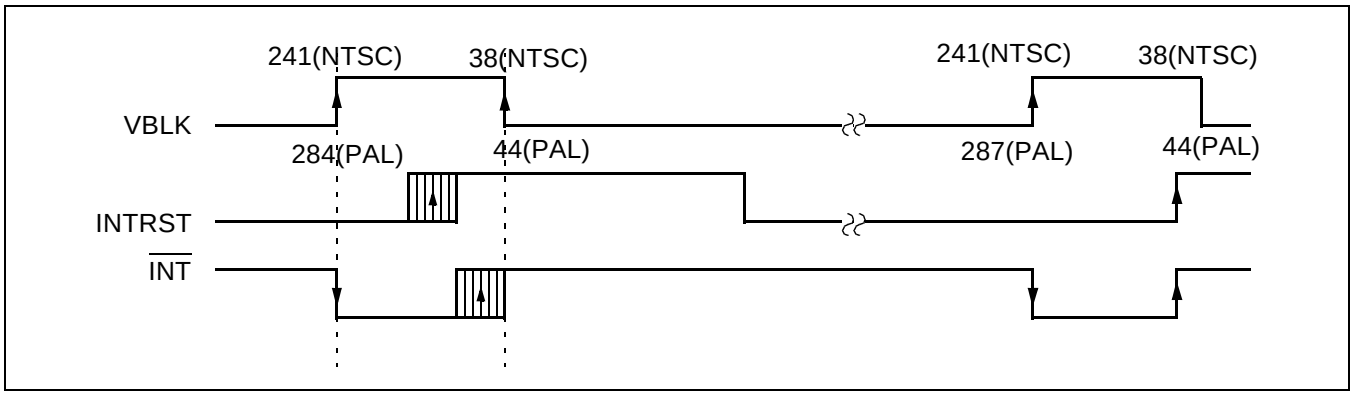

Figure 14.

When INTEN=1,$\overline{INT}$=high

Table 4. Font ROM Table

Font	Code	Font	Code	Font	Code	Font	Code	Font	Code	Font	Code	Font	Code	Font	Code
0	00	W	20	단	40	팩	60	구	80	く	A0	オ	C0	ㄱ	E0
1	01	X	21	림	41	편	61	부	81	=	A1	カ	C1	ㄲ	E1
2	02	Y	22	랙	42	힘	62	우	82	>	A2	キ	C2	ㄳ	E2
3	03	Z	23	램	43	한	63	주	83	?	A3	ク	C3	ㄴ	E3
4	04	a	24	면	44	행	64	곡	84	㎓	A4	ケ	C4	ㄵ	E4
5	05	b	25	반	45	거	65	꿈	85	삼	A5	コ	C5	ㄶ	E5
6	06	c	26	번	46	나	66	동	86	‖	A6	サ	C6	ㄷ	E6
7	07	d	27	번	47	디	67	분	87	″	A7	シ	C7	ㄸ	E7
8	08	e	28	방	48	더	68	복	88	″	A8	ス	C8	ㄹ	E8
9	09	f	29	쌍	49	레	69	속	89	#	A9	セ	C9	ㄺ	E9
A	0A	g	2A	성	4A	바	6A	음	8A	♭	AA	ソ	CA	ㄻ	EA
B	0B	h	2B	상	4B	시	6B	은	8B	㎐	AB	タ	CB	ㄼ	EB
C	0C	i	2C	쌕	4C	셔	6C	용	8C	㎒	AC	チ	CC	ㄽ	EC
D	0D	j	2D	선	4D	이	6D	준	8D	▪	AD	ツ	CD	ㄾ	ED
E	0E	k	2E	션	4E	아	6E	콤	8E		AE	テ	CE	ㄿ	EE
F	0F	l	2F	일	4F	제	6F	들	8F	기	AF	ト	CF	ㅀ	EF
G	10	m	30	열	50	끼	70	원	90	데	B0	ナ	D0	ㅁ	F0
H	11	n	31	없	51	껴	71	환	91	오	B1	ニ	D1	ㅂ	F1
I	12	o	32	영	52	자	72	의	92	모	B2	ヌ	D2	ㅃ	F2
J	13	p	33	임	53	제	73	좌	93	노	B3	ネ	D3	ㅄ	F3
K	14	q	34	양	54	쳐	74	화	94	하	B4	ノ	D4	ㅅ	F4
L	15	r	35	언	55	타	75	!	95	파	B5	ハ	D5	ㅆ	F5
M	16	s	36	역	56	그	76	%	96	다	B6	ヒ	D6	ㅇ	F6
N	17	t	37	정	57	고	77	&	97	줌	B7	フ	D7	ㅈ	F7
▮	18	u	38	전	58	로	78	(	98	플	B8	ヘ	D8	ㅉ	F8
P	19	v	39	장	59	스	79	)	99	어	B9	ホ	D9	ㅊ	F9
Q	1A	w	3A	집	5A	죠	7A	*	9A	마	BA	マ	DA	N/A	FA
R	1B	x	3B	절	5B	조	7B	,	9B	잔	BB	ミ	DB	N/A	FB
S	1C	y	3C	작	5C	그	7C	-	9C	ア	BC	ム	DC	N/A	FC
T	1D	z	3D	캡	5D	트	7D	.	9D	イ	BD	メ	DD	N/A	FD
U	1E	간	3E	탐	5E	프	7E	/	9E	ウ	BE	モ	DE	N/A	FE
V	1F	남	3F	탈	5F	표	7F	:	9F	エ	BF	ヤ	DF	N/A	FF

D/A CONVERTERS

The KS0125 contains three high speed current DACs. Each DAC can drive a 75 load. The three DACs operate at the 27 MHz clock rate. The voltage supply for the DAC must be decoupled from the power supply for the digital circuitry on the chip. The voltage between the analog supply (VDDA) and digital supply (VDD) must be maintained within one diode voltage drop (0.7 V). The DACs require two external 0.1 µF capacitors and one 787 Ω resistor connected as shown in Figure 15. Also shown in Figure 15 is an optional reconstruction filter for the DAC output to reduce sinx/x distortion

.

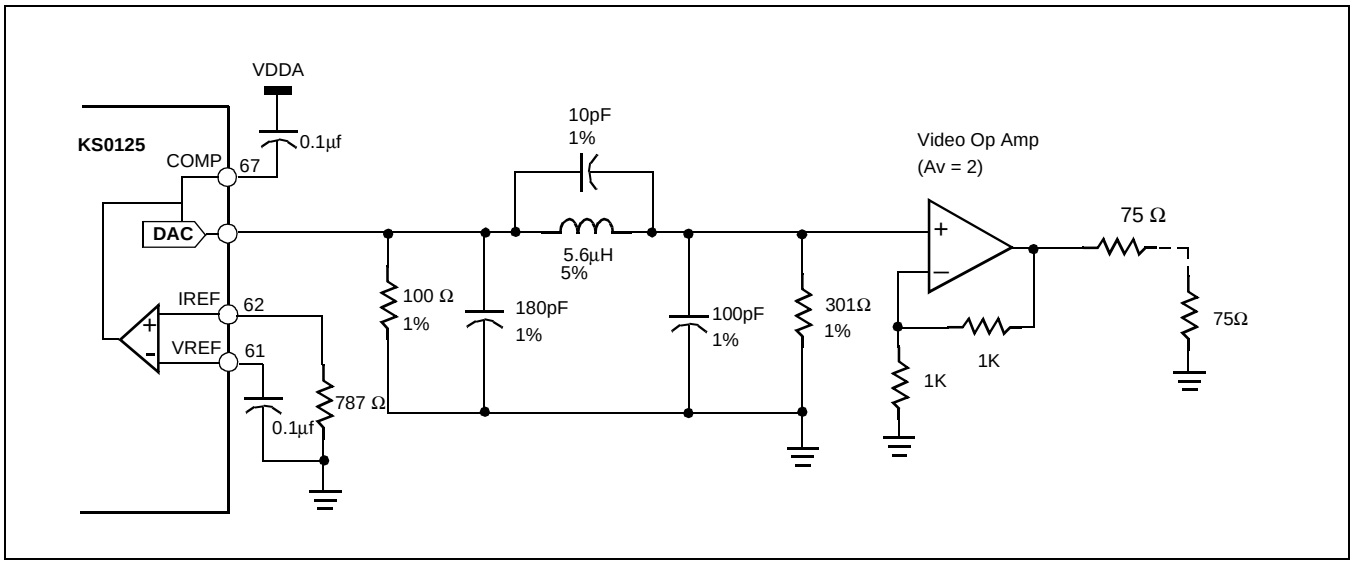

Figure 15. Typical DAC Configuration with Optional Reconstruction Filter

Host Interface

The KS0125 uses a parallel host interface for programming the control registers and OSD RAM. The bus consists of one address line, eight data lines, one read/write (R/$\overline{W}$) line, and one chip select ($\overline{CS}$) line. To access the control registers, an index is first written to the index register (A0 = 0). Then the data is read from or written to the data register (A0 = 1). Figure 16 shows how data is written to control register **REGB** (index 1) and how to read control register **VFLG** (index 2).

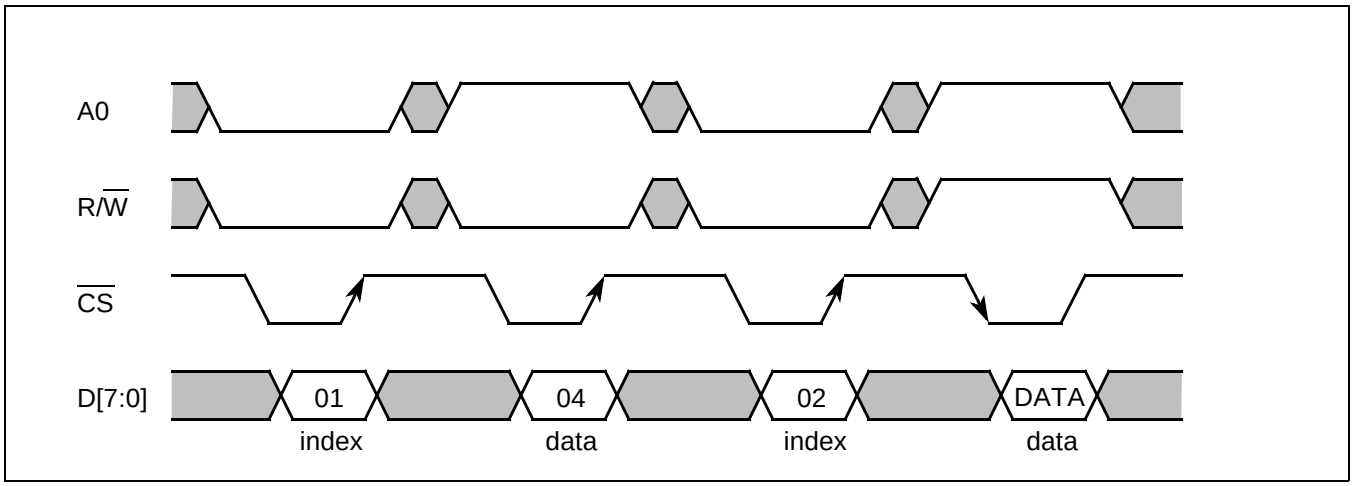

Figure 16. Control Register Write/Read Sequence

Writing to the OSD RAM is done by first writing the row number to the index register (the number must be offset by hex 10 to indicate that data written to the data register is intended for OSD RAM). A burst of 1 to 25 bytes is then written to the data register. The data will be transferred sequentially into the OSD RAM for the particular row starting from the first column location. Figure 17 provides an example of how to change the first three characters in the first row. Note that the OSD RAM can only be written.

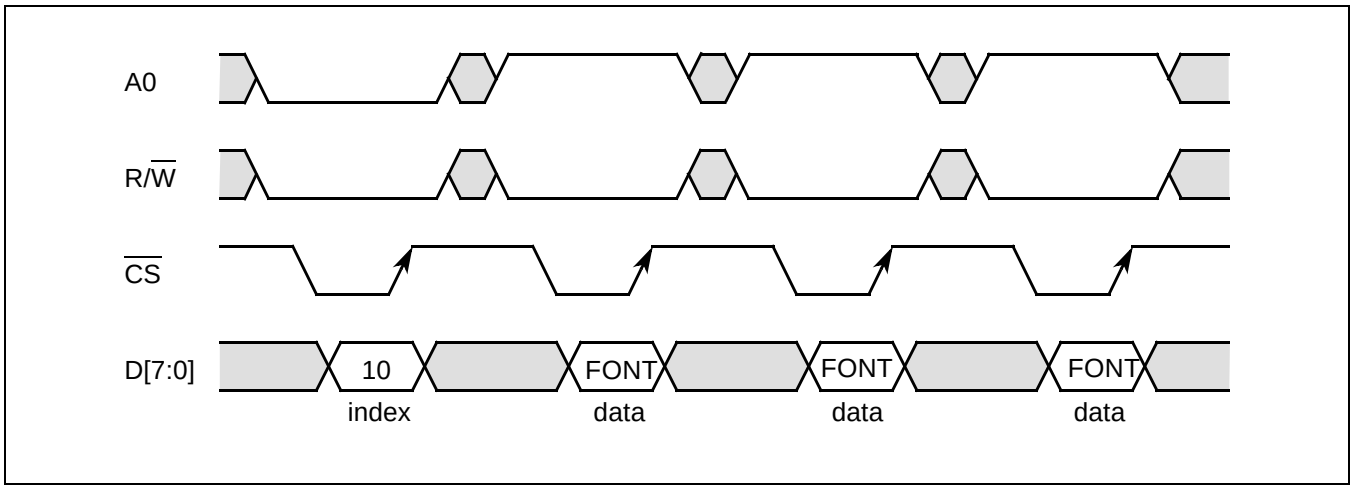

Figure 17. OSD RAM Write Sequence

For both control registers and OSD RAM, the number written to the index register remains unchanged until a new number is written to it. For OSD RAM write, the internal auto-increment pointer gets reset to 0 either after the 25th location is written, or the index register is written.

DETAILED REGISTER DESCRIPTION

The KS0125 contains eight user programmable control registers and one OSD RAM selection register. Table 2 is a register summary list.

Table 5. Register Summary

Index	Mnemonic	Power-On Default	Description
00h	REGA	79h	Control register A.
01h	REGB	04h	Control register B.
02h	VFLG	02h/82h	Vertical blank status and $\overline{INT}$ reset control. The msb is a read only vertical blank flag.
03h	HUE	00h	Hue control register.
04h	REGC	00h	Control register C.
05h	REGD	25h	Control register D.
06h	RESERVED	07h	Reserved.
07h	REGE	00h	Control register E.
08h – 0fh	RESERVED	–	Reserved. Should not be written to.
10h – ffh	OSDRAM	–	Internally, only bit 4 of the 8-bit index register is decoded. If bit 4 is a 1, data written to the data register (A0 = 1) is sent to the OSDRAM.

The following is a description of the bits in each register. The default value is followed by an asterisk (*). Register bits with no specific functions are indicated by a dash (–).

Control Register A									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
00h	REGA	CBW1	CBW0	VFIR	CRISP	GAMEN	GAMMA	COR1	COR0

COR[1:0] Luma coring selection.

- 00 No coring.
- 01 1 LSB coring.*
- 10 2 LSB coring.
- 11 3 LSB coring.

GAMMA Gamma correction selection.

- 0 Small peaking.*
- 1 Large peaking.

GAMEN Luma gamma correction enable.

- 0 Gamma correction disabled.
- 1 Gamma correction enabled.*

CRISP Luma crisper function enable.

- 0 Cripser function is disabled.
- 1 Crisper function is enabled (recommended for MPEG video).*

VFIR Vertical filter enable.

- 0 Vertical filter is disabled.
- 1 Vertical filter is enabled (recommended for MPEG video).*

CBW[1:0] Chroma low pass filter bandwidth selection.

- 00 or 11 Low bandwidth.
- 01 Medium bandwidth (preferred for most video formats).*
- 10 High bandwidth.

Note The default value for this REGA register is 79h.
During normal operation, users are recommended to program this register to 60h.

Control Register B									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01h	REGB	OSD	CHCLR1	CHCLR0	BGCLR1	BGCLR0	PDEN	FMT1	FMT0

FMT[1:0] Encoder output video format selection.

00 NTSC.*

x1 PAL-B,G,H.

10 Reserved.

PDEN NTSC pedestal insertion.

0 No pedestal (Japan NTSC).

1 Pedestal is inserted.*

BGCLR[1:0] OSD background color selection.

0x Transparent.*

10 Blue.

11 Black.

CHCLR[1:0] OSD character color selection.

00 White.*

01 Cyan.

10 Green.

11 Magenta.

OSD OSD enable.

0 OSD is disabled.*

1 OSD is enabled.

Vertical Blank Status and INT Reset									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
02h	VFLG	VBLK	-	-	-	-	-	1	INTRST

INTRST — $\overline{INT}$ reset control.

0 — Leave $\overline{INT}$ unchanged.*

1 — Force $\overline{INT}$ to the high state.

VBLK — Vertical blank flag. This is a read only status bit. The state of this bit tracks the state of the $\overline{VSYN}$ pin except that this is active high. This bit can be polled by software; when it is high, the OSD RAM can be updated.

Hue Control Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
03h	HUE	HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0

HUE[7:0] — Hue adjust. This number is unsigned. The nominal value is 0. The hue can be adjusted at a resolution of 1.40625 degrees.

Control Register C									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
04h	REGC	VFM	–	–	CKOSL	INFMT	MODE	–	–

MODE Master/slave timing mode selection.

0 Slave mode.*

1 Master mode.

INFMT Digital video input format selection.

0 Input is CCIR 601.*

1 Input is CCIR 656.

CKOSL CKO clock output frequency selection.

0 CKO frequency is 13.5 MHz.*

1 CKO frequency is 27 MHz. This selection is not available if CKI27 is the clock input.

VFM Vertical filter mode selection.

0 Only even field is interpolated.*

1 Both fields are interpolated.

Control Register D									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
05h	REGD	–	YCEN	CVBSEN	–	–	HAV2	HAV1	HAV0

HAV[2:0] Master mode active video start control. The KS0125 expects the first active pixel to be 122 13.5 MHz clocks after the leading edge of the HSYN (for PAL, the number is 132). The following offset, in number of 27 MHz clocks, provides additional phase shifts to compensate for any external data latency. **SHFHAV** is bit 4 of **REGE**.

000 +11+SHFHAV.

001 +9+SHFHAV.

010 +7+SHFHAV.

011 +5+SHFHAV.

100 +3+SHFHAV.

101 +1+SHFHAV.*

110 -1+SHFHAV.

111 -3+SHFHAV.

CVBSEN CVBS DAC control.

0 CVBS DAC is disabled.

1 CVBS DAC is enabled.*

YCEN LUMA and CHROMA DACs control.

0 LUMA and CHROMA DACs are disabled.*

1 LUMA and CHROMA DACs are enabled.

Control Register E									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
07h	REGE	–	–	–	SHFHAV	EAV	FLD	YCDLY	CKILL

CKILL Color kill.

0 Enable color.*

1 Force output to be black and white. Color burst is still inserted.

YCDLY Luma path data delay control.

0 No delay.*

1 One 27 MHz clock delay.

FLD Field identification in slave mode.

0 Use $\overline{\text{VSYN}}$ and $\overline{\text{HSYN}}$ for field identification.*

1 Use ODD input.

EAV Slave mode synchronization selection.

0 Use $\overline{\text{HSYN}}$, $\overline{\text{VSYN}}$ or ODD inputs for synchronization.*

1 Use EAV for synchronization.

SHFHAV One additional 27 MHz clock phase shift for the start of active pixel in master mode

0 No shift.*

1 One 27 MHz clock shift.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Units
Supply voltage (measured to VSS)	V_{DD}	-0.5 to + 7.0	V
Analog and digital supply voltage difference	ΔV_{AD}	-0.7 to +0.7	V
Digital input applied voltage(2) (measured to VSS)	V_i	-0.5	V
Digital input forced current(3,4)	A_i	-100 to +100	mA
Digital output applied voltage(2) (measured to VSS)	V_o	-0.5 to (V_{DD}+0.5)	V
Digital output forced current(3,4)	A_o	-100 to +100	mA
Digital short circuit duration (single output high state to VSS)	TDsc	1	sec
Analog short circuit duration (single output to VSS)	TA_{SC}	infinite	
Ambient operating temperature (case)	T_A	-60 to + 130	°C
Storage temperature	T_S	-65 to + 150	°C
Junction temperature	T_J	-65 to +150	°C
Vapor phase soldering (1 min.)	Tvsol	220	°C
Lead Soldering Temperature (10 sec., 1/4© from pin)	Tsol	300	°C

NOTES:

1. .Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.
2. Applied voltage must be current limited to the specified range, and measured with respect to VSS.
3. Forcing voltage must be limited to the specified range.
4. Current is specified as a conventional current, flowing into the device.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Units
Supply voltage (measured to VSS)	V_{DD}	4.75	5.0	5.25	V
Reference voltage	V_{ref}	–	1.235	–	V
Reference current	I_{ref}	–	1.569	–	mA
Analog output load	R_L	–	75	–	W
Ambient operating temperature, still air	T_A	0	–	70	°C

ELECTRICAL CHRACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Units
SUPPLY					
Total power supply current (digital plus analog, CKIN=27MHz.)	I_{DD}	–	–	200	mA
DIGITAL-TO-ANALOG CONVERTER					
DAC resolution	RES	10	–	–	bits
Voltage reference (VREF) output	V_{REF}	1.110	1.235	1.360	V
DAC gain factor	K_{DAC}	10.31	10.85	11.39	–
K_{DAC} imbalance between DACs	K_{IMBAC}	–5%	–	+5%	–
DAC reference current (V_{REF}=nominal)	I_{REF}	–	1.569	–	mA
Reference resistor (V_{REF}=nominal)	R_{REF}	–	787	–	Ω
Blanking level output voltage (NTSC and PAL modes)	V_{BLANK}	–	0.300	–	V
Video output compliance voltage	V_{OC}	–0.3	–	1.6	V
Total output load resistance	R_L	–	75	–	Ω
Analog output delay	T_{dly}	–	32	–	ns
DIGITAL I/O CHARACTERISTICS					
Digital input voltage, logic HIGH, TTL compatible inputs.	V_{IH}	2.5	–	V_{DD}	V
Digital input voltage, logic LOW, TTL compatible inputs	V_{IL}	V_{SS}	–	0.6	V
Digital input current, logic HIGH (V_{IN}=4.0 V)	I_{IH}		–	10	µA
Digital input current, logic LOW (V_{IN}=0.4 V)	I_{IL}		–	–10	µA
Digital output voltage, logic HIGH (I_{OH}= -400µA)	V_{OH}	2.4	–	V_{DD}	V
Digital output voltage, logic LOW (I_{OL}=3.2 mA)	V_{OL}	V_{SS}	–	0.4	V
DIGITAL VIDEO PORT TIMING					
Digital video input setup time to rising edge of pixel clock	t_{svid}	5	–	–	ns
Digital video input hold time from rising edge of pixel clock	t_{hvid}	5	–	–	ns
CKI27 frequency variation*	Δ_{CKI27}	–	–	50	ppm
XTLI frequency variation*	Δ_{XTLI}	–	–	50	ppm
Clock duty cycle (CKI27, XTLI)*	δ	40%	50%	60%	–

ELECTRICAL CHRACTERISTICS (Continued)

Characteristics	Symbol	Min	Typ	Max	Units
Pipeline delay from P[15:0] input to DAC input*	t_{PD}	–	41	–	27MHz periods
Clock input-to-output (CKI27 or XTLI to CKO) delay (65 pF load)*	t_{dlyCLK}	–	–	12	ns
Clock doubler short/long term jitter	δ_{CKdbl}	–	–	±1	ns
HOST INTERFACE TIMING					
$\overline{CS}$ low	$t_{pwl\overline{CS}}$	148	–	–	ns
$\overline{CS}$ high	$t_{pwh\overline{CS}}$	296	–	–	ns
R/$\overline{W}$ setup time to falling edge of $\overline{CS}$	$t_{sR/\overline{W}}$	8	–	–	ns
R/$\overline{W}$ hold time from rising edge of $\overline{CS}$	$t_{hR/\overline{W}}$	222	–	–	ns
A0 setup time to falling edge of $\overline{CS}$	t_{sA}	8	–	–	ns
A0 hold time from falling edge of $\overline{CS}$	t_{hA}	8	–	–	ns
Write mode data setup time to rising edge of $\overline{CS}$	t_{sD}	8	–	–	ns
Write mode data hold time from rising edge of $\overline{CS}$	t_{hD}	8	–	–	ns
Read mode delay from falling edge of $\overline{CS}$ To data valid	t_{validD}	–	–	75	ns
Read mode delay from rising edge of $\overline{CS}$ to data 3-state	$t_{3\text{-}stateD}$	–	–	10	ns

*: These parameters are guaranteed by by design.

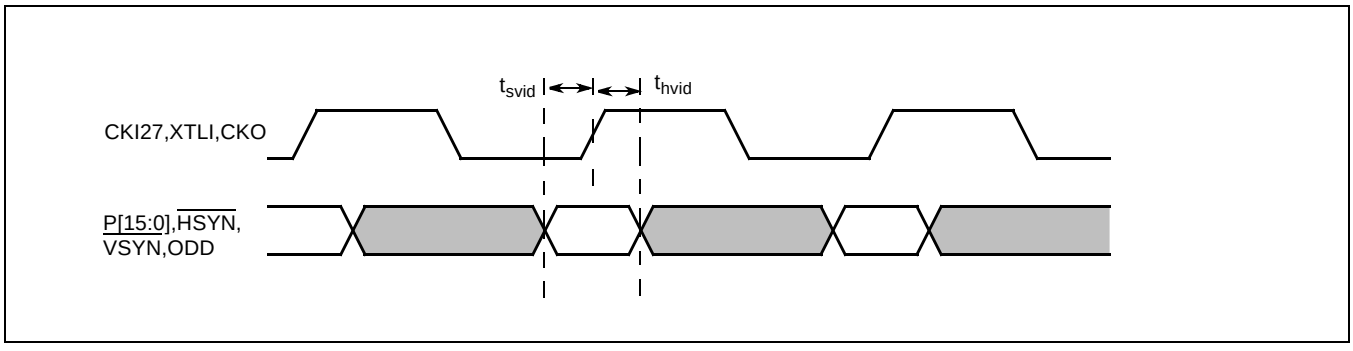

Figure 18. Video Port Data Setup and Hold Time

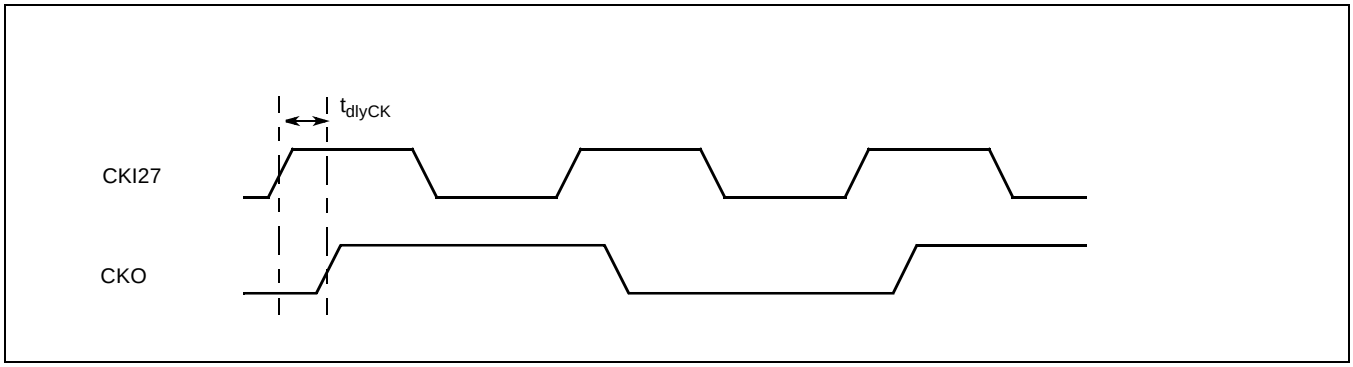

Figure 19. CKI27 to CKO Delay

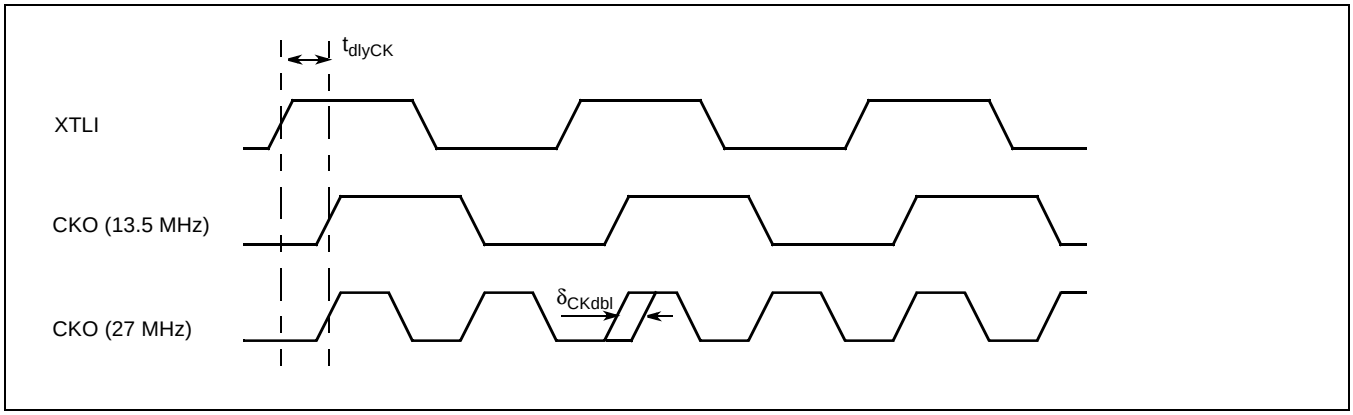

Figure 20. XTLI to CKO Delay

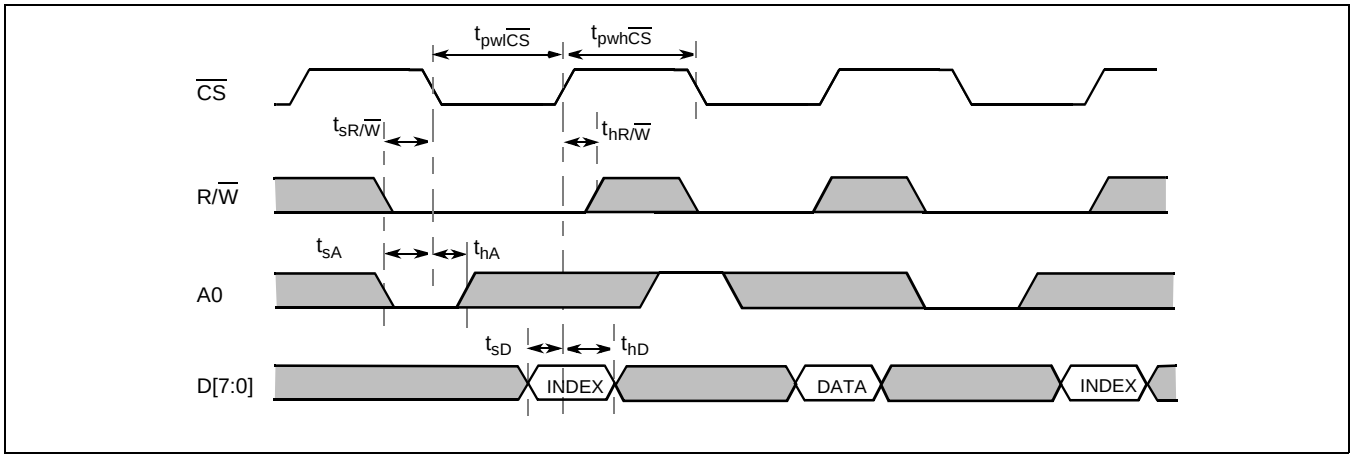

Figure 21. Write Protocol for the Host Interface

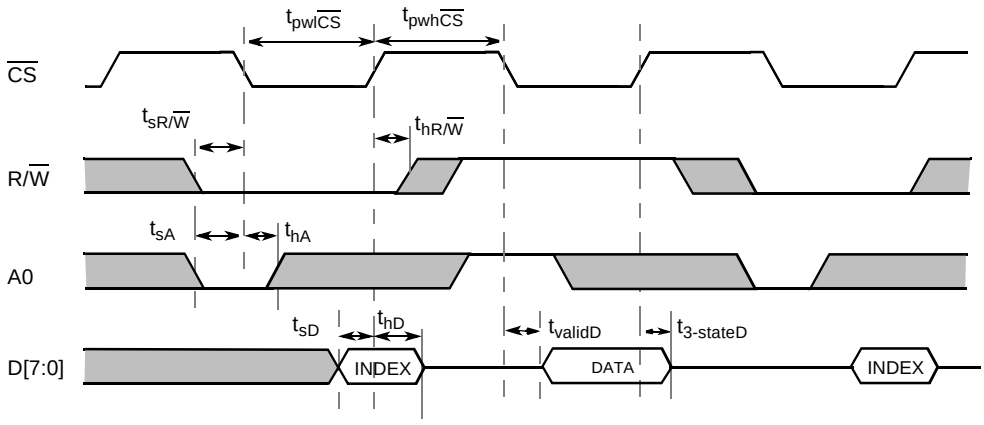

Figure 22. Read Protocol for the Host Interface

VIDEO PERFORMANCE

The KS0125 encoder meets the requirements listed in the table below when configured using the application circuit of Figure 15. The test methods and test signals meets the requirements of NTC Report No. 7or EIA/TIA-250. A Tektronix TSG1001 Programmable TV Generator and a Tektronix VM700A Video Measurement Set are used for measurement verification.

Video Performance Characteristics

Test Name	Symbol	Test Waveform	Min	Typ	Max	Unit
Amplitude response versus frequency	AMPRESP	Multiburst to 4.2 MHz	–	0.25	–	dB_{p-p}
Differential gain	DG	Modulated staircase or ramp (NTC-7 composite)	–	1.5	–	$\%_{p-p}$
Differential phase	DP	Modulated staircase or ramp (NTC-7 composite)	–	1.0	–	deg_{p-p}
Chroma nonlinear gain distortion	CNLG	Three-level chroma signal (NTC-7 combination)	–	1.0	–	IRE
Chroma nonlinear phase distortion	CNLP	Three-level chroma signal (NTC-7 combination)	–	1.0	–	deg
Chroma-to-luma intermodulation	CLIMD	Three-level chroma signal (NTC-7 Combination)	–	1	–	IRE
Chroma/luma gain equality	CLGI	12.5T modulated pulse (NTC-7 composite) YCDLY=LOW	–	102.5	–	%
Chroma/luma delay inequality (analog filter delay excluded)	CLDI	12.5T modulated pulse (NTC-7 Composite) YCDLY=LOW	–	5	–	ns
Luma nonlinear distortion	LNLD	5-step unmodulated staircase	–	2.5	–	%
Noise level	NOISE1	100% unmodulated ramp	–	–61	–	dB_{rms}
Noise level	NOISE2	100% unmodulated ramp	–	–72	–	dB_{rms}
Chroma AM noise	CAMN	Red field, 500kHz bandwidth	–	–56	–	dB_{rms}
Chroma PM noise	CPMN	Red field, 500kHz bandwidth	–	–58	–	dB_{rms}
Field time waveform distortion	FTWD	Field square wave	–	1.5	–	IRE_{p-p}
Line time waveform distortion	LTWD	18 µs 100 IRE bar (NTC-7 composite)	–	0.5	–	IRE_{p-p}
Long time waveform distortion: initial peak overshoot peak overshoot after 5 seconds	LOTWD	10% / 90% APL bounce		 15 1.5		 IRE IRE