élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2018/EL2018C

Fast, High Voltage Comparator with Transparent Latch

Features

- Fast response time—20 ns
- Wide input differential voltage range—24V to ±15V supplies
- Precision input stage—V_{OS} = 1 mV
- Low input bias current—I_B = 100 nA
- Low input offset current—I_{OS} = 30 nA
- ±4.5V to ±18V supplies
- 3-State TTL and CMOS compatible output
- No supply current glitch during switching
- High voltage gain—40 V/mV
- 50% power reduction in shutdown mode
- Input and latch remain active in shutdown mode
- P/N compatible with industry standard comparators

Applications

- Analog to digital converters
- ATE pin receiver
- Precision crystal oscillators
- Zero crossing detector
- Window detector
- Pulse width modulation generator
- "Go/no-go" detector

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2018CH	0°C to +75°C	TO-99	MDP0004
EL2018CJ	0°C to +75°C	CerDIP	MDP0010
EL2018CN	0°C to +75°C	P-DIP	MDP0031
EL2018H	−55°C to +125°C	TO-99	MDP0004
EL2018H/883B	−55°C to +125°C	TO-99	MDP0004
EL2018J	−55°C to +125°C	CerDIP	MDP0010
EL2018J/883B	−55°C to +125°C	CerDIP	MDP0010

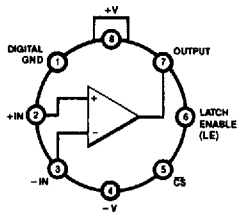
General Description

The EL2018 represents a quantum leap forward in comparator speed, accuracy and functionality. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures the part maintains speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and latch remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see: *Elantec's Military Processing-Monolithic Products.*

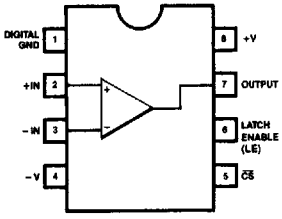
Connection Diagrams

TO-99 Metal Can



2018-1

8-Pin CerDIP
8-Pin Plastic DIP



2018-2

Top View

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Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	I_O	Continuous Output Current	25 mA
V_{IN}	Input Voltage	$+V_S$ to $-V_S$	T_A	Operating Temperature Range	
ΔV_{IN}	Differential Input Voltage	Limited only by Power Supplies		EL2018	−55°C to +125°C
				EL2018C	0°C to +75°C
I_{IN}	Input Current (Pins 1, 2 or 3)	±10 mA	T_J	Operating Junction Temperature	
I_{INS}	Input Current (Pins 5 or 6)	±5 mA		Ceramic DIP Package,	
P_D	Maximum Power Dissipation			Metal Can Package	175°C
	(Note 4—See Curves)			Plastic DIP Package	150°C
	CerDIP	1.5W	T_{ST}	Storage Temperature	−65°C to +150°C
	Metal Can	1.0W		Lead Temperature	
	Plastic DIP	1.25W		(Soldering, 10 seconds)	300°C
I_{OP}	Peak Output Current	50 mA			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series systems. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2018	EL2018C	
V_{OS}	Input Offset Voltage (Note 1) V_{CM} = 0V, V_O = 1.4V	25°C		1.0	3	I	I	mV
		T_{MIN}, T_{MAX}			5	I	III	mV
I_B	Input Bias Current V_{CM} = 0V, Pin 2 or 3	25°C		100	300	I	I	nA
		T_{MIN}, T_{MAX}			500	I	III	nA
I_{OS}	Input Offset Current V_{CM} = 0V	25°C		30	150	I	I	nA
		T_{MIN}, T_{MAX}			250	I	III	nA
CMRR	Common Mode Rejection Ratio (Note 2)	25°C	85	105		I	I	dB
		T_{MIN}, T_{MAX}	80			I	III	dB
PSRR	Power Supply Rejection Ratio (Note 3)	25°C	85	100		I	I	dB
		T_{MIN}, T_{MAX}	77			I	III	dB
V_{CM}	Common Mode Input Range	25°C	±12	±13		I	I	V
		T_{MIN}, T_{MAX}	±12			I	III	V
A_V	Voltage Gain V_{OUT} = 0.8V to 2.0V	25°C	15	40		I	I	V/mV
		T_{MIN}, T_{MAX}	10			I	III	V/mV
V_{OL}	Output Voltage Logic Low I_{OL} = 0 mA to 8 mA	25°C	−0.05	0.15	0.4	I	I	V
		T_{MIN}, T_{MAX}	−0.1		0.4	I	III	V

DC Electrical Characteristics $V_S = \pm 15V$ unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2018	EL2018C	
V_{oh}	Output Voltage Logic High $V_S = \pm 15V$	25°C	3.5	4.0	4.65	I	I	V
	$V_S = \pm 15V$	T_{MIN}, T_{MAX}	3.5		4.65	I	III	V
	$V_S = \pm 5V$	25°C	2.4			I	I	V
	$V_S = \pm 5V$	T_{MIN}	2.4			I	III	V
	$V_S = \pm 5V$	T_{MAX}	2.4			I	III	V
V_{odis1}	V_{OUT} Range, Disabled, $I_{OL} = -1$ mA $V_S = \pm 15V$	25°C	4.65			I	I	V
	$V_S = \pm 15V$	T_{MIN}, T_{MAX}	4.65			I	II	V
	$V_S = \pm 5V$	25°C		3.5		V	V	V
V_{odis2}	V_{OUT} Range, Disabled, $I_{OL} = 1$ mA $V_S = \pm 5V$ to $\pm 15V$	ALL	−0.3	−1		I	II	V
V_{inh}	LE or $\overline{CS}$ Inputs Logic High Input Voltage	25°C	2.0			I	I	V
		T_{MIN}, T_{MAX}	2.2			I	III	V
V_{inl}	LE or $\overline{CS}$ Inputs Logic Low Input Voltage	25°C			0.8	I	I	V
		T_{MIN}, T_{MAX}			0.8	I	III	V
I_{in}	LE or $\overline{CS}$ Inputs Logic Input Current $V_{IN} = 0V$ to 5V	25°C			±200	I	I	µA
		T_{MIN}, T_{MAX}			±300	I	III	µA
I_{s+en}	Positive Supply Current Enabled	25°C		8.4	10	I	I	mA
		T_{MIN}, T_{MAX}			11	I	III	mA
I_{s+dis}	Positive Supply Current Disabled	25°C		4.7	6	I	I	mA
		T_{MIN}, T_{MAX}			7	I	III	mA
I_{s-en}	Negative Supply Current Enabled	25°C		13.0	17	I	I	mA
		T_{MIN}, T_{MAX}			18	I	III	mA
I_{s-dis}	Negative Supply Current Disabled	25°C		5.0	6.5	I	I	mA
		T_{MIN}, T_{MAX}			6.5	I	III	mA

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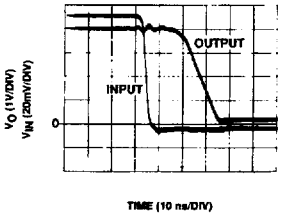
AC Electrical Characteristics $V_S = \pm 15V, T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level		Units
					EL2018	EL2018C	
T_{pd}	Propagation Delay, 5 mV Overdrive		20	40	I	III	ns
T_s	Setup Time		6	12	IV	IV	ns
T_h	Hold Time		−2	0	IV	IV	ns
T_{un}	Unlatch Time		23	40	IV	IV	ns
T_{mpw}	Minimum Clock Pulse Width		12		V	V	ns
T_{en}	Output 3-State Enable Delay		40	70	IV	IV	ns
T_{dis}	Output 3-State Disable Delay		150	300	IV	IV	ns

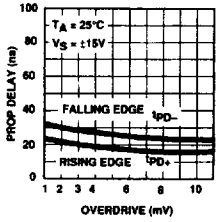
Note 1: $V_{OUT} = 1.4V$.
Note 2: $V_{CM} = 12V$ to $-12V$.
Note 3: $V_S = \pm 5V$ to $\pm 15V$.
Note 4: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

Typical AC Performance Curves

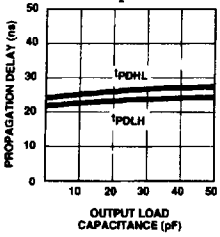
Propagation Delay (−)
5 mV Overdrive



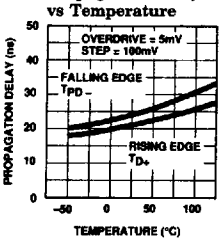
Propagation Delay
vs Overdrive



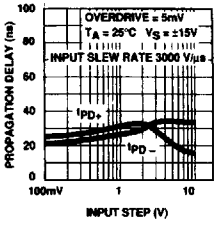
Propagation Delay vs
Load Capacitance



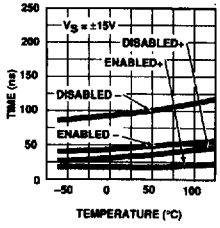
Propagation Delay
vs Temperature



Propagation Delay
vs Input Step



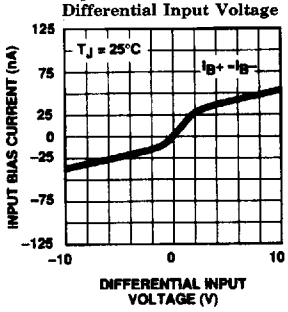
Enabled/Disabled Time
vs Temperature



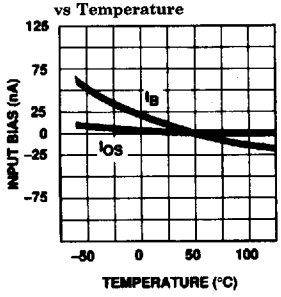
2018-3

Typical AC Performance Curves — Contd.

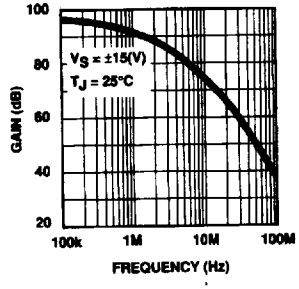
Input Bias Current vs Differential Input Voltage



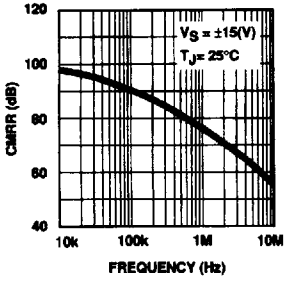
Input Bias Current vs Temperature



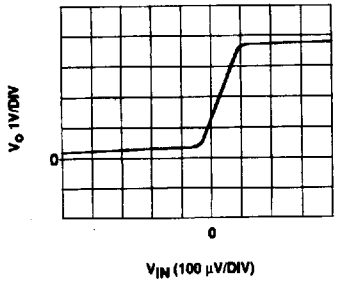
Open-Loop Gain vs Frequency



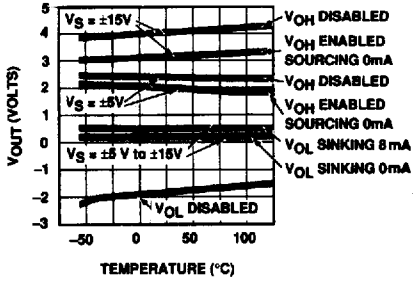
CMRR vs Frequency



V_O/V_I Transfer Characteristic



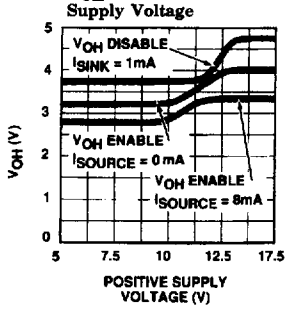
V_{OUT} vs Temperature



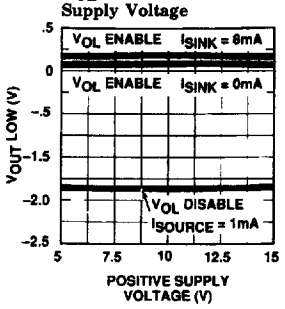
2018-4

Typical Performance Curves — Contd.

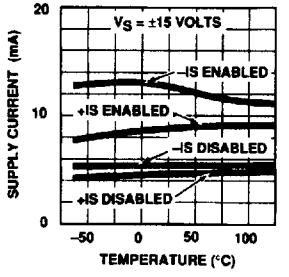
V_{OH} vs Positive Supply Voltage



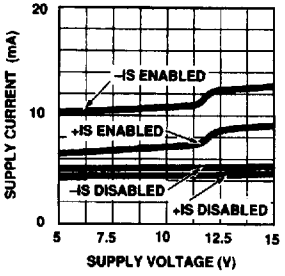
V_{OL} vs Positive Supply Voltage



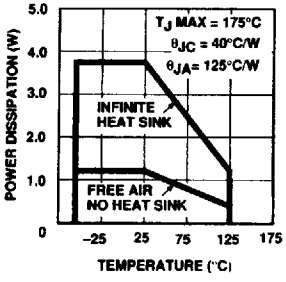
Supply Current vs Temperature



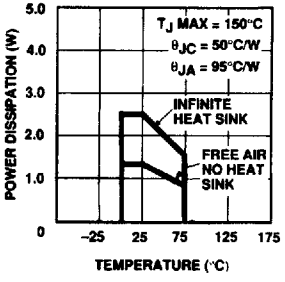
Supply Current vs Supply Voltage



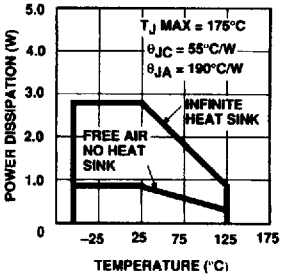
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature

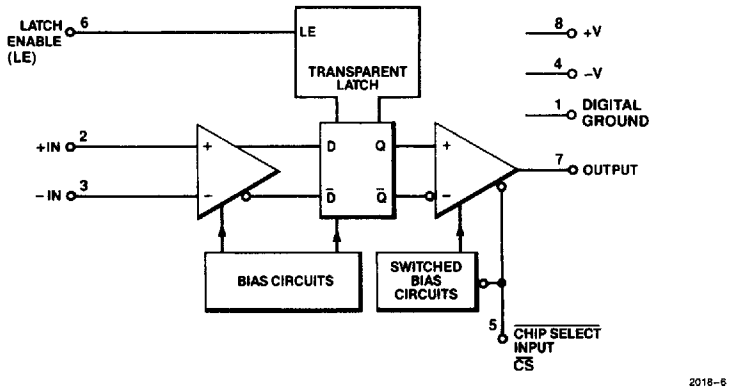


8-Lead TO-99 Metal Can Maximum Power Dissipation vs Ambient Temperature



2018-5

Block Diagram



Function Table

Inputs (time n−1)				Internal Q	Notes	Output
+IN	−IN	$\overline{CS}$	LE			
+	−	L	L	H	Normal Comparator Operation	H
−	+	L	L	L		L
+	−	H	L	H	Internal Normal Comparator Operation	High Z
−	+	H	L	L	Output Power Down Mode	High Z
X	X	L	H	Qn−1	Data Retained in Latch	Qn−1
X	X	H	H	Qn−1	Data Retained in Latch Power Down Mode	High Z

Application Hints

Device Overview

The EL2018 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Dielectric Isolation Process, which is immune to power sequencing and latch up problems.

Power Supplies

The EL2018 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.1 μF monolithic ceramic recommended) close to the power supply leads. Good ground plane construction techniques enhance stability, and the lead from pin 1 to ground should be short.

Front End

The EL2018 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V). The transfer function of the EL2018 is linear, and the output is stable when in the linear region.

The large common mode range (±12V minimum) and differental voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

EL2018/EL2018C

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Fast, High Voltage Comparator with Transparent Latch

Application Hints — Contd.

Recovery from Large Overdrives

Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device.

Input Slew Rate

All comparators have input slew rate limitations. The EL2018 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators.

Latch

The EL2018 contains a "transparent" latch. A "transparent" latch acts as an amplifier when the LE input is low and it "latches" and holds the value it had just before the LE transition from low to high.

It is possible to make an oscillation resistant design by putting a short duration "0" on the LE input whenever you wish to make a comparison. This gates the comparator on only for a brief instant, long enough to compare, but not long enough to oscillate. The minimum duration of this pulse is specified by the minimum clock width parameter in the AC electrical tables.

The $\overline{CS}$ input may be left floating and still produce a guaranteed logic "0" input (active). Floating the LE input will normally produce a logic "0" input also, but operation is not guaranteed.

Proper RF technique suggests that these inputs be grounded or pulled to ground if they are not used.

Output Stage

The output stage of the EL2018 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2018 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature

The EL2018 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in a large ATE system where there may be 1000 comparators, but only 10% are in use at any one time.

Due to the power saving feature and linear output stage, the EL2018 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2018 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

System Design Considerations

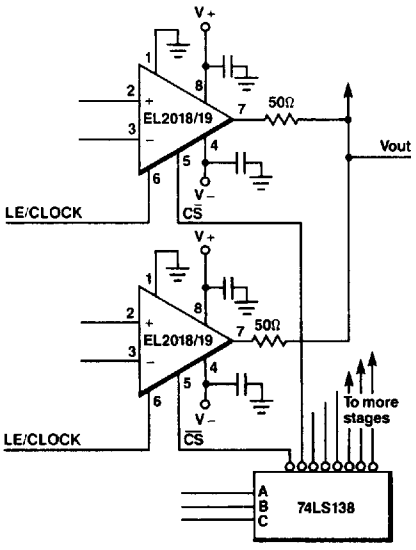
The most common problem users have with high speed comparators is oscillations due to output to input feedback. This can be avoided by using a ground plane, proper supply bypassing, and routing the inputs and outputs away from each other. Since the EL2018 has a gain bandwidth product of about 40 GHz, layout and bypassing are important to a successful system design. A unique alternative to the EL2018 is the EL2019, with its edge triggered master/slave flip flop.

Device Functions

The various operating states of the EL2018 are described in the function table on page 3-9.

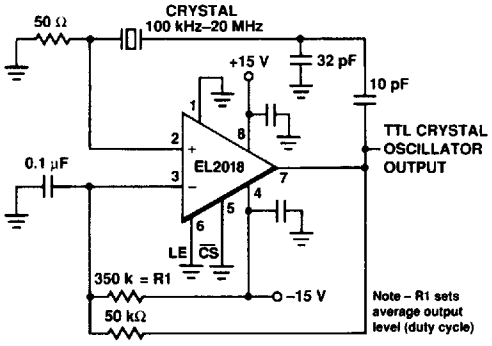
Typical Applications

Using the Power Down/ 3-State Feature



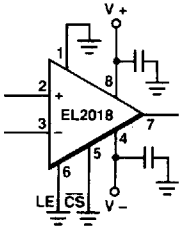
2018-7

Series Resonant Crystal Oscillator



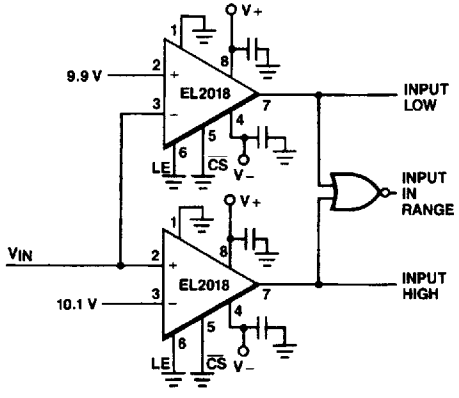
2018-8

Using the EL2018 in the Transparent Mode (Latch Not Used)



2018-9

A Wide Input Range Window Comparator



2018-10

V_{IN} Range +12V to −12V
with V_S = ±15V

EL2018/EL2018C

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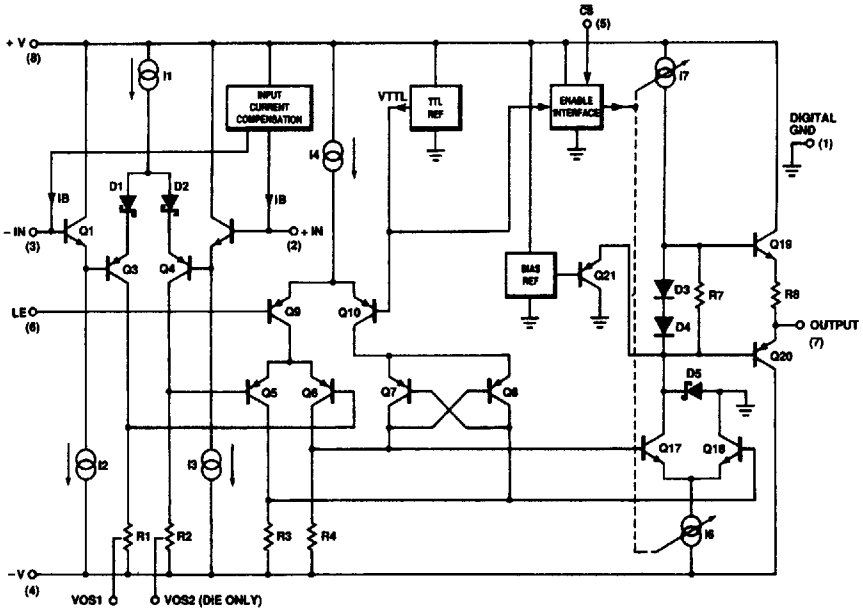
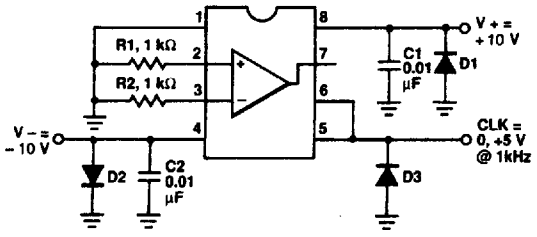
Fast, High Voltage Comparator with Transparent Latch

Equivalent Schematic



2018-11

Burn-In Circuit



2018-12

Pin numbers are for DIP packages.
All packages use the same schematic.

EL2018 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +V
*                   |     |     |     -V
*                   |     |     |     |     LE
*                   |     |     |     |     |     CS
*                   |     |     |     |     |     |     output
*                   |     |     |     |     |     |     |
.subckt M2018       2     3     8     4     6     5     7
*
* Input Stage
*
i1 8 10 700µA
r1 13 4 1K
r2 14 4 1K
q1 8 3 11 qn
q2 8 2 12 qn
q3 13 11 10 qp
q4 14 12 10 qp
i2 11 4 200µA
i3 12 4 200µA
*
* 2nd Stage & Flip Flop
*
*i4 8 24 700µA
i4 8 24 1mA
q9 22 6 24 qp
q10 18 17 24 qp
v1 17 0 2.5V
q5 15 14 22 qp
q6 16 13 22 qp
r3 15 4 1K
r4 16 4 1K
q7 16 15 18 qp
q8 15 16 18 qp
*
* Output Stage
*
i7 8 35 2mA
s1 35 20 5 0 sw
d2 35 8 ds
i6 26 34 5mA
s2 34 4 5 0 sw
d3 34 26 ds
q19 8 20 21 qn 2
q20 4 19 7 qp 2
r8 21 7 60
r7 20 19 4K
q17 19 16 26 qn 5
q18 0 15 26 qn 5
q22 20 20 30 qn 5
```

EL2018/EL2018C

ELANTEC INC

Fast, High Voltage Comparator with Transparent Latch

EL2018 Macromodel — Contd.

```
q23 19 19 30 qn 8
d1 0 19 ds
q21 0 17 19 qp
*
* Power Supply Current
*
ips 8 4 4mA
*
* Models
*
.model qn npn (is=2e-15 bf=400 tf=0.05nS cje=0.3pF cjc=0.2pF ccs=0.2pF)
.model qp pnp (is=0.6e-15 bf=60 tf=0.3nS cje=0.5pF cjc=0.5pF ccs=0.4pF)
.model ds d(is=2e-12 tt=0.05nS eg=0.62V vj=0.58)
.model sw vswitch (von=0.4V voff=2.5V)
.ends
```