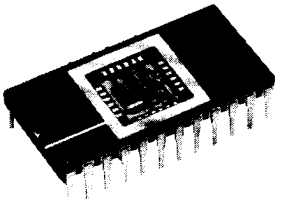
ILC DATA DEVICE CORPORATION

12 BIT MULTIPLYING D/A CONVERTER
Double Buffered; Voltage Output



DESCRIPTION

The DAC-02701 is a double buffered 4 quadrant multiplying DAC with a 10 volt full scale output. It has two-stage transparent input latches for direct microprocessor compatibility, and features 12 bit parallel data transfer. Packaged in a small hermetically sealed 24 pin DDIP, the DAC-02701 offers 12 bit monotonicity over its full –55°C to +125°C operating temperature range. Input registers and multiplying DAC are implemented with low power CMOS technology, offering compatibility with both CMOS and TTL logic families. Data transfer from a 16 bit data bus can be accomplished with one byte. MIL-STD-883B screening is available.

APPLICATIONS

With its small hermetic package, wide operating temperature range, and versatile performance, the DAC-02701 is ideal for the most demanding military and industrial requirements. Typical applications include equipment for computer interface and control, function generation and signal conditioning.

The DAC-02701 two-stage input latches are especially useful in applications that require simultaneous update of multiple DAC channels from a single data bus. These applications include X-Y and sine-cosine coordinate generation.

FEATURES

- *μP COMPATIBLE: DOUBLE BUFFERED INPUT LATCHES*
- *±10 V FULL SCALE VOLTAGE OUTPUT*
- *12 BIT MONOTONIC OVER –55°C TO +125°C TEMPERATURE RANGE*
- *12 BIT PARALLEL DATA TRANSFER*
- *4 QUADRANT MULTIPLICATION*
- *SMALL HERMETIC 24 DDIP PACKAGE*

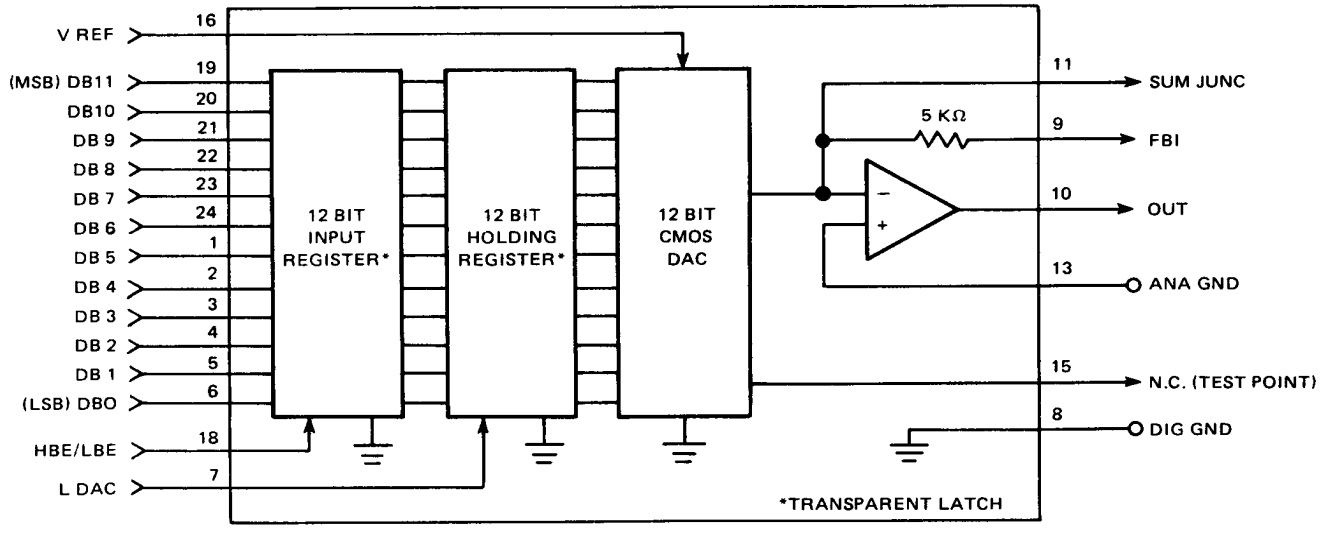


FIGURE 1. DAC-02701 BLOCK DIAGRAM

SPECIFICATIONS – Typical values @ +25°C, V_{REF} = +10V, and ±15 volt power supply voltages unless otherwise noted:

PARAMETER	UNITS	VALUE	
		11 Bit Mono	12 Bit Mono
RESOLUTION	bits	12	12
ACCURACY			
Linearity Error			
Full temp range	%F.S.R.	±0.1 max	±0.05 max
Offset Error			
Full temp range	mV	±10 max	±3 max
Gain Error			
Full temp range	%F.S.R.	±0.2 max	±0.2 max
Monotonicity			
Full temp range	bits	11	12
DYNAMIC CHARACTERISTICS			
Settling Time (1)	µsec	25 max	
Reference Feedthrough (2)	mV p-p	1	
DIGITAL INPUTS			
Logic Compatibility		CMOS and TTL	
Voltage Input			
Logic "1"	V	+2.4 to +V_{DD}	
Logic "0"	V	–0.3 to +0.8	
Current Load			
Logic "1"	µA	1 max	
Logic "0"	µA	1 max	
Strobe Pulse Width (3)	nsec	250 min	
Data Setup Time	nsec	250 min	
Data Hold Time	nsec	0 min	
Coding		Complementary Offset Binary	
REFERENCE			
Input Voltage	V	±10	
Input Impedance	KΩ	2.5 min	
ANALOG OUTPUT			
Voltage	V	±10	
Current	mA	±4 max	
Impedance	Ω	0.1 max	
POWER SUPPLIES			
V_{DD}			
Nominal	V	+15 ±0.45	
Current Drain	mA	10 max	
Range	V	+5 to +16 max	
Rejection Ratio	%/%	0.005 max	
V_{EE}			
Nominal	V	–15 ±0.45	
Current Drain	mA	10 max	
Range	V	Same as V_{DD}	
Rejection Ratio	%/%	0.005 max	
TEMPERATURE RANGE			
Operating			
–1 Option	°C	–55 to +125	
–2 Option	°C	–25 to + 85	
Storage	°C	–65 to +150	
PHYSICAL CHARACTERISTICS			
Package		24 pin DDIP	
Size	in	1.22 x 0.6 x 0.15	
		(31.0 x 15.3 x 3.8 mm)	
Weight	oz	0.09 (2.5g)	

NOTES:
(1) Output settling time to within 0.01% of final value for a 10 volt digital input change
(2) V_{REF} = 20 V p-p at 1 KHz
(3) LDAC and HBE/LBE strobes are level triggered

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a block diagram of the DAC-02701. Functional elements of the unit include a 12 bit input register, a 12 bit holding register, a 12 bit CMOS multiplying DAC, and a current to voltage converter op amp.

Both sets of registers are level triggered and function as transparent latches. This allows the DAC-02701 to be configured for double buffered, single buffered, or direct flow through operation, by proper use of the 2 strobe signals. The input registers are implemented with low power CMOS technology, and are compatible with both CMOS and TTL logic families.

Four (4) quadrant multiplication is accomplished by the 12 bit CMOS DAC. It provides a current output which is the product of its reference input voltage and the digital input stored in the holding register. The external reference may be AC or DC, unipolar or bipolar. Output coding is Complementary Offset Binary. The output op amp is used to convert the DAC current to a voltage.It offers a low impedance source of the 10 volt full scale output. Separate analog and digital grounds are provided to allow flexible use of noise reduction techniques. The analog and digital ground pins must be tied together at one point in the system, preferably close to the DAC-02701.

FOUR QUADRANT MULTIPLICATION

The DAC-02701 output voltage is the product of the applied external reference voltage and the 12 bit digital input word. Four quadrant multiplication refers to the fact that the reference voltage may be either positive or negative, and the digital input word may be either positive or negative. Furthermore, the external reference may be either DC or AC. The DAC-02701 output is therefore the product of both the magnitude and polarity of the two inputs.

INPUT CODING

The DAC-02701 input coding is Complementary Offset Binary. Figure 2 shows various digital input codes and the analog output resulting from each one. It is to be noted that most significant bit (MSB) functions as a polarity control. When the MSB is a logic "0", the output is the same polarity as the external reference. When the MSB is a logic "1", the output is the opposite polarity from the external reference. The eleven LSBs therefore function as a digitally controlled attenuator.

MICROPROCESSOR INTERFACING

Two-stage 12 bit input registers, each independently strobed, make the DAC-02701 easy to interface to a 12 bit or 16 bit microprocessor data bus. Figure 3 illustrates the most general microprocessor interface. The DAC-02701 is mapped into two memory locations; one each for the input register and holding register. Address decoding provides HBE/LBE select for the input register, and LDAC select for the holding register. The microprocessor WRITE signal is then used to generate the HBE/LBE strobe or LDAC strobe, which transfer the data into the appropriate register.

The microprocessor interface shown in Figure 3 is most often used in applications that require simultaneous update of multiple DAC channels from a single data bus. Data is sequentially transferred from the bus to each DAC input register. Then all DACs are updated in parallel by strobing their holding registers simultaneously.

For data bus interfaces with random update requirements, the configuration of Figure 3 may be simplified. These applications require only single buffering of the 12 bit input data. The DAC-02701 holding register can therefore be placed in its transparent mode by permanently tying the LDAC strobe line to a logic "1" level. The DAC-02701 can also be operated with both input register stages in the transparent mode. When HBE/LBE and LDAC strobes are both tied to logic "1", input data will flow through directly to the DAC. The DAC output will then respond directly to input data changes.

TIMING DIAGRAM

Figure 4 is a DAC-02701 timing diagram. It illustrates data and strobe signal timing relationships. The HBE/LBE strobe pulse width must be 250 nanoseconds minimum. Data set-up time, prior to the falling edge of HBE/LBE, is 250 nanoseconds minimum. The LDAC strobe pulse width must be 250 nanoseconds minimum. In order to ensure isolation of the holding register from the data bus, the rising edge of LDAC must follow the falling edge of HBE/LBE by zero (0) nanoseconds minimum.

OFFSET AND GAIN TRIMS

Some applications may require a lower gain error and/or DC offset error than the DAC-02701 exhibits after factory adjustment. Figure 5 illustrates the connections required to trim gain and DC offset errors to zero. Multi-turn trimpots, with temperature coefficients less than 100 ppm/°C are recommended for best results. Metal film fixed resistors, with temperature coefficients less than 100 ppm/°C, are also recommended.

POWER SUPPLIES AND DECOUPLING

Recommended power supply voltages for the DAC-02701 are ±15 volts. It will operate satisfactorily, though, over the range ±5 volts to ±16 volts. If power supplies lower than 15 volts are used, the allowable reference and output voltage swings are less than the specified ±10 volts. This is due to limitations in the output op amp. As an example, if ±5 volt power supplies are used, the reference and output swings will be restricted to typically ±3 volts.

Capacitive decoupling of all power supplies is recommended to minimize noise. Tantalum or electrolytic capacitors of 1 μf or greater will filter out low frequency noise. Ceramic capacitors of 0.01 μf will filter out high frequency noise. For best results, all capacitors should be placed as close as possible to the DAC.

GROUNDING AND LAYOUT PRECAUTIONS

The DAC-02701 provides separate analog and digital grounds to allow flexible use of noise reduction techniques. The ANA GND and DIG GND pins must be tied together at one point in the system, preferably very close to the DAC-02701. The objective of the grounding scheme should be to minimize the AC and DC digital current flow in the return path of the analog signals.

DIGITAL INPUT	ANALOG OUTPUT
0000 0000 0000	$+V_{REF}$
0010 0000 0000	$+V_{REF}$ (3/4)
0100 0000 0000	$+V_{REF}$ (1/2)
0111 1111 1111	$+V_{REF}$ (1/2048)
1000 0000 0000	0
1000 0000 0001	$-V_{REF}$ (1/2048)
1100 0000 0000	$-V_{REF}$ (1/2)
1110 0000 0000	$-V_{REF}$ (3/4)
1111 1111 1111	$-V_{REF}$ (2047/2048)

FIGURE 2. INPUT CODING

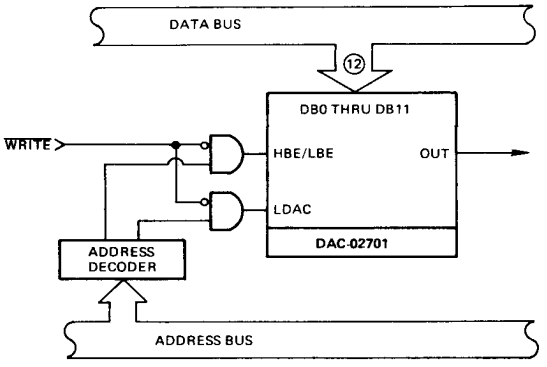


FIGURE 3. MICROPROCESSOR INTERFACE

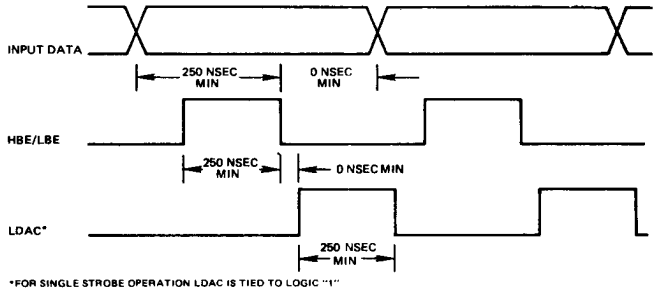


FIGURE 4. TIMING DIAGRAM

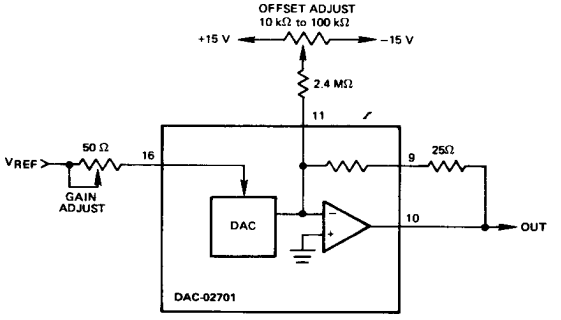


FIGURE 5. OFFSET AND GAIN TRIMS

A grounding configuration which works well is to tie together the ANA GND and DIG GND pins at the DAC-02701 package. A single connection is then made between the analog ground of the DAC-02701 and the analog ground of the load. System power ground should be connected close to the load.

In general, ground noise is minimized by using wide ground conductor paths, which exhibit a lower impedance. To minimize crosstalk and inductive affects, digital input lines and analog output lines should be separated from each other, and made as short as possible.

Unused digital inputs must be connected to either ground or V_{DD}. When digital inputs are routed directly to another printed circuit board, it is recommended that a high value (1Mohm) resistor be connected between each input and ground. This will prevent static charge buildup and resulting damage when the PC board is removed from the circuit.

REALIABILITY

Low power CMOS integrated circuits, and a minimum chip count have resulted in a very low calculated failure rate of the DAC-02701. The predicted MTBF is 6,000,000 hours. in accordance with MIL-HDBK-217C at +25°C in ground fixed applications.

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PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	DB5	13	ANA GND
2	DB4	14	N.C.
3	DB3	15	N.C. (TEST POINT)
4	DB2	16	V_{REF}
5	DB1	17	+15 V (V_{DD})
6	DB0 (LSB)	18	HBE/LBE
7	LDAC	19	DB11 (MSB)
8	DIG GND	20	DB10
9	FB1	21	DB9
10	OUT	22	DB8
11	SUM JUNC	23	DB7
12	−15 V (V_{EE})	24	DB6

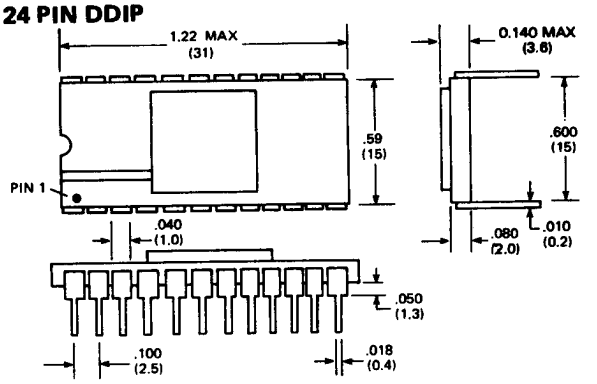
ORDERING INFORMATION

DAC-02701 −1 0 3

- Monotonicity Grade:
  - 3 = 12 bit over temp range
  - 2 = 11 bit over temp range
- Reliability Grade:
  - 0 = Screened to MIL-STD-883 but without pre burn-in testing, burn-in, and QCI testing.
  - 1 = Fully compliant with MIL-STD-883.
  - 2 = Screened to MIL-STD-883 but without QCI testing.
- Operating Temperature Range:
  - 1 = −55°C to +125°C
  - 2 = −25°C to +85°C

MECHANICAL OUTLINE

24 PIN DDIP



NOTES:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

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