Am3101

64-Bit Write Transparent, Inverting Output, Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Ultra-fast version: Address access time 15 ns
- Low power: I_{CC} typically 50 mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- High speed
- Fully decoded 16-word x 4-bit Schottky RAMs

GENERAL DESCRIPTION

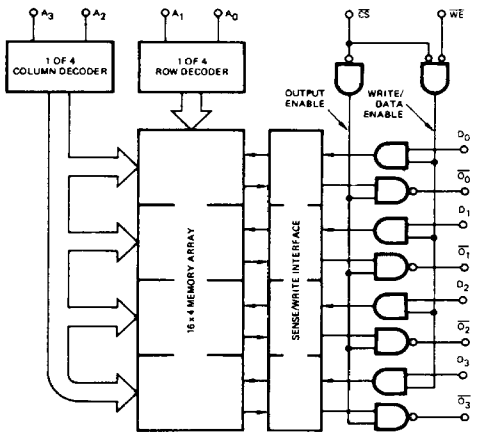
The Am3101 is comprised of 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and is ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active-LOW chip select ($\overline{CS}$) input and open-collector OR tieable outputs.

An active-LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW, the information on the four data inputs, D_0 to D_3, is written into the addressed memory word. During the write cycle, the outputs are active and invert the four data inputs, D_0 to D_3.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O_0}$ to $\overline{O_3}$.

When the chip select line is HIGH, the four outputs of the memory go to an inactive high-impedance state.

BLOCK DIAGRAM



BD000761

MODE SELECT TABLE

Input		Data Output Status $\overline{O_0} - \overline{O_3}$	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Data in (Inverted)	Write
L	H	Selected Word (Inverted)	Read
H	X	Output Disabled	Deselect

H = HIGH L = LOW X = Don't Care

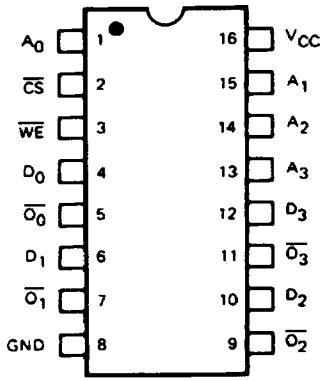
PRODUCT SELECTOR GUIDE

Family Part No.	Am3101				
Open-Collector (Write Transparent) Part No.	Am3101-15	Am3101-20	Am3101-25	Am3101-35	Am3101-50
I_{CC}	70 mA	70 mA	70 mA	70 mA	70 mA
Access Time	15 ns	20 ns	25 ns	35 ns	50 ns
Temperature Range	C	M	C	C	M

Publication # 03203 Rev. D Amendment /0
Issue Date: January 1987

CONNECTION DIAGRAMS
Top View

DIPs*



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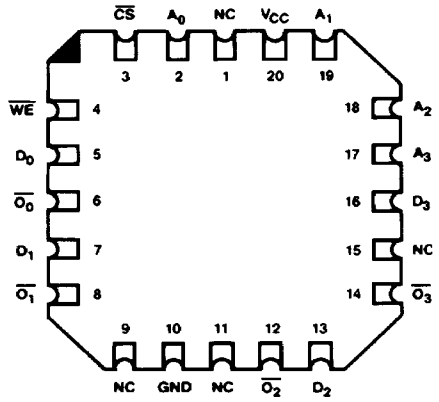
LCC



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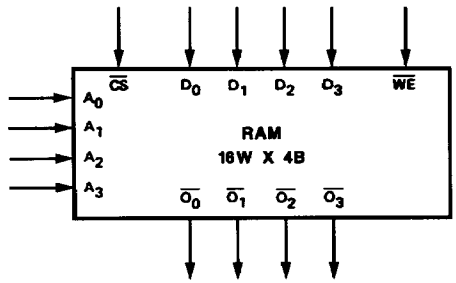
*Also available in 16-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



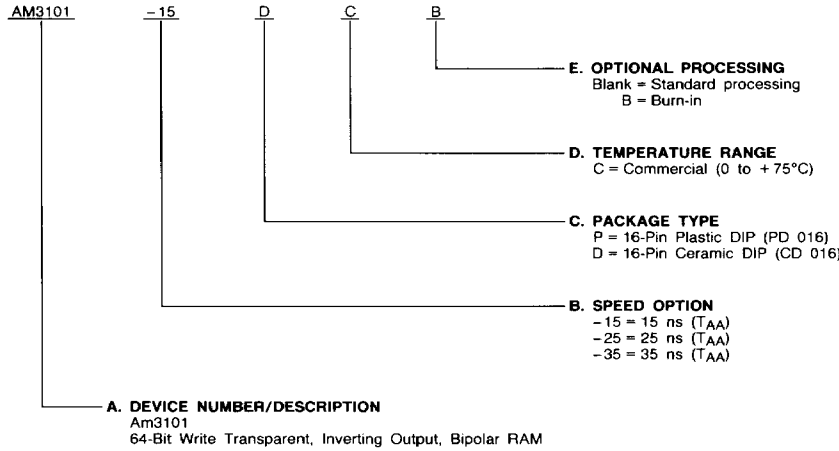
LS000212

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM3101-15	PC, PCB, DC, DCB
AM3101-25	
AM3101-35	

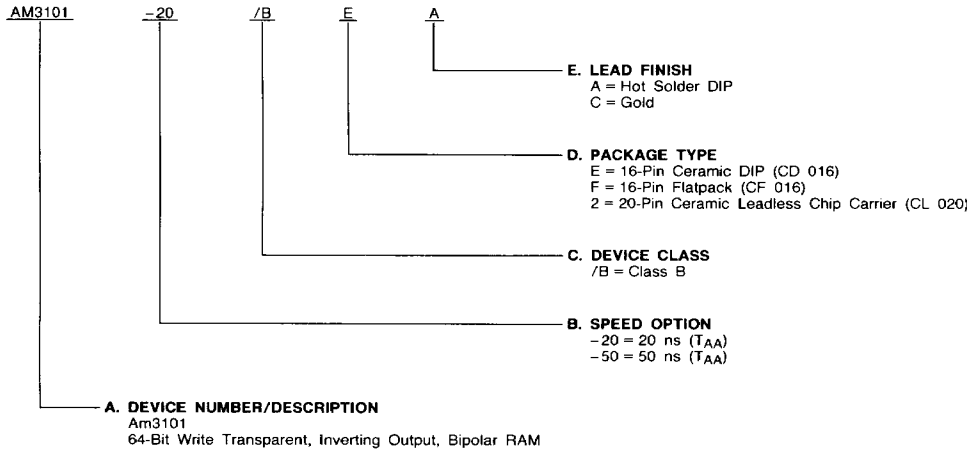
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM3101-20	/BEA, /BFA, /B2C
AM3101-50	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
Output Current into Outputs ..... 20 mA
DC Input Current ..... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military* (M) Devices
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

(See note 3)

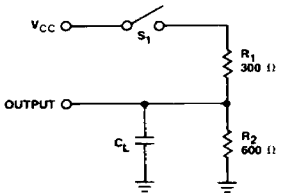
*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified; Included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted.

Parameter Symbol	Parameter Description	Test Conditions		Am3101/3101-1 Min.	Typ.	Max.	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		350	450	mV
			I_{OL} = 20 mA		380	500	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)		2.0			Volts
V_{IL}	Input HIGH Level	Guaranteed Input Logical LOW Voltage for all inputs (Note 2)				0.8	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V	$\overline{WE}$, $D_0 - D_3$, $A_0 - A_3$		−15	−250	μA
			$\overline{CS}$		−30	−250	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			0	10	μA
I_{CC}	Power Supply Current	All inputs = GND Outputs = Open V_{CC} = Max.			50	70	mA
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA			−0.85	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$=V_{IL} V_{OUT} = 2.4 V, V_{CC} = Max.			0	40	μA

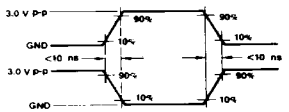
Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_C = T_J$.
$\theta_{JA} \approx 50$ °C/W (with moving air) for Ceramic DIP.
$\theta_{JC} \approx 10 - 17$ °C/W for Flatpack and Leadless Chip Carrier.

SWITCHING TEST CIRCUIT



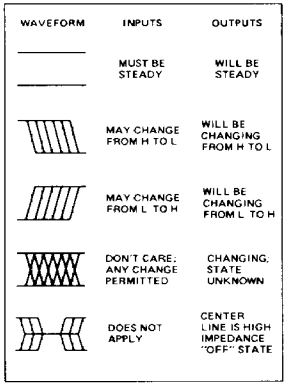
TC000171

SWITCHING TEST WAVEFORM



TW000031

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING CHARACTERISTICS over Commercial operating range unless otherwise specified

No.	Parameter Symbol	Parameter Description	Am3101-15		Am3101-25		Am3101-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Standard Power Devices									
1	$t_{PLH}(A)$	Delay from Address to Output		15		25		35	ns
2	$t_{PHL}(A)$								
3	$t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data		15		15		17	ns
4	$t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery - See Note 1)		15		20		35	ns
5	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	0		0		0		ns
6	$t_h(A)$	Hold Time Address (After Termination of Write)	0		0		0		ns
7	$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	20		20		25		ns
8	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	0		0		0		ns
9	$t_{pw}(\overline{WE})$	MIN Write Enable Pulse Width to Insure Write	20		20		25		ns
10	$t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (Hi-Z)		15		15		17	ns
11	$t_{PLH}(DI)$	Delay from Data Input to Correct Data Output ($\overline{WE} = \overline{CS} = V_{IL}$)		15		25		35	ns
12	$t_{PHL}(DI)$								

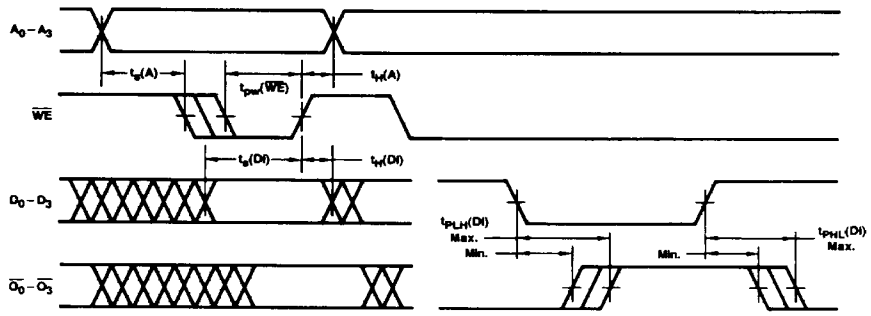
Notes: See notes following Military Switching Characteristics.

SWITCHING CHARACTERISTICS over Military operating range unless otherwise specified; Included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted.

No.	Parameter Symbol	Parameter Description	Am3101-20		Am3101-50		Units
			Min.	Max.	Min.	Max.	
Standard Power Devices							
1	$t_{PLH}(A)$	Delay from Address to Output		20		50	ns
2	$t_{PHL}(A)$						
3	$t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data		20		25	ns
4	$t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery - See Note 1)		15		50	ns
5	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	0		0		ns
6	$t_h(A)$	Hold Time Address (After Termination of Write)	0		0		ns
7	$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	20		25		ns
8	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	0		0		ns
9	$t_{pw}(\overline{WE})$	MIN Write Enable Pulse Width to Ensure Write	20		25		ns
10	$t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (Hi-Z)		15		25	ns
11	$t_{PLH}(DI)$	Delay from Data Input to Correct Data Output ($\overline{WE} = \overline{CS} = V_{IL}$)		20		50	ns
12	$t_{PHL}(DI)$						

Notes: 1. Output is conditioned to data in (inverted) during write to ensure correct data is present on all outputs during write and after write is terminated.
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
3. All delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), t_{PLZ} ($\overline{WE}$), t_{PLZ} ($\overline{CS}$), t_{PZL} ($\overline{WE}$) and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30$ pF; and with both the input and output timing referenced to 1.5 V.

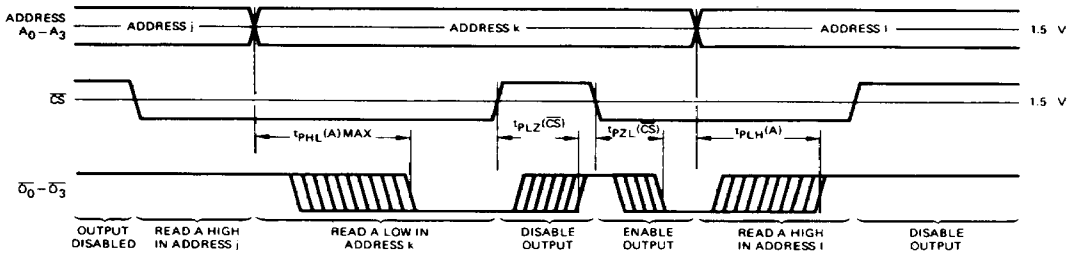
SWITCHING WAVEFORMS



WF001081

Write Mode

Write Cycle Timing. The cycle is initiated by an address change. After t_S(A) Min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) Min. must be allowed before the address may be changed again. The output will be the complement of the data input while the write enable ($\overline{WE}$) is LOW.



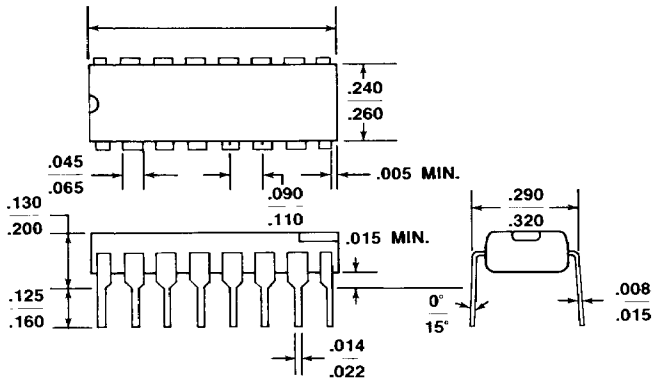
WF001071

Read Mode

Switching delays from address and chip select inputs to the data output.

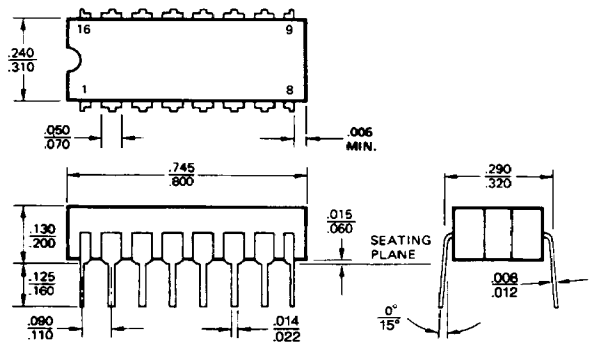
PHYSICAL DIMENSIONS*

PD 016



PID# 06957A

CD 016

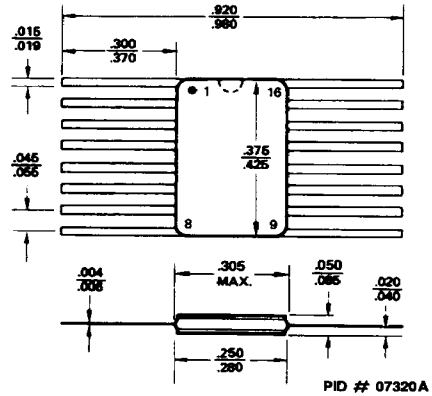


PID # 07319A

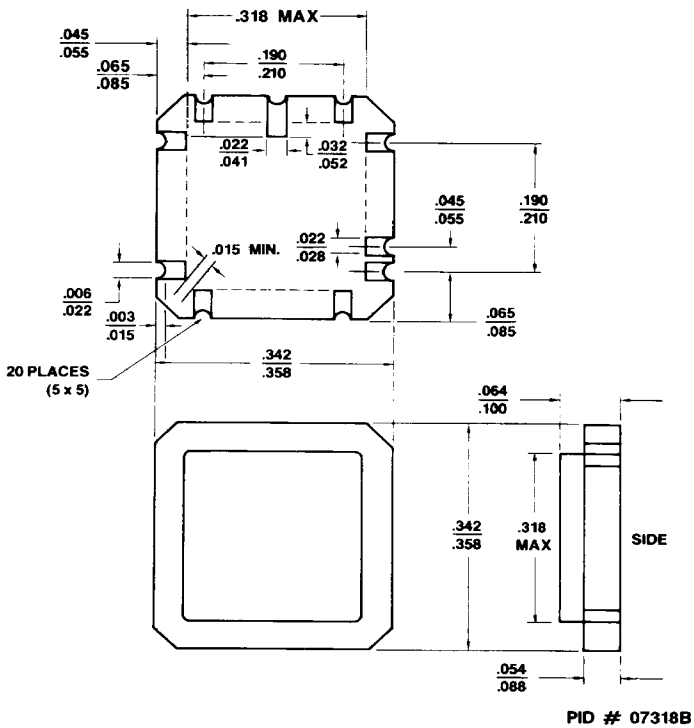
*For reference only.

PHYSICAL DIMENSIONS (Cont'd.)

CF 016



CL 020



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