High Speed, 14-Bit, 2 MHz Sampling A/D Converters

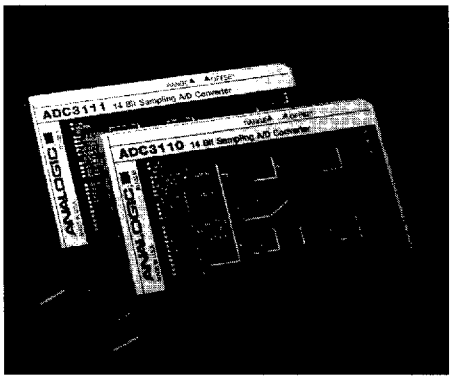
With Built-In Sample-and-Hold Amplifiers

Introduction

The ADC3110/ADC3111 series of products consists of 14-bit, 2 MHz A/D converters with built-in sample-and-hold amplifiers, designed for use in applications requiring high speed and high resolution front ends such as ATE, medical imaging, radar, communications, and analytical instrumentation. This family of sampling A/D converter products is ideally suited for both single channel performance requiring low distortion processing of high frequency signals (ADC3110) and multiplexed signal sources requiring fast front end settling time (ADC3111).

The ADC3110/ADC3111 fits easily into sockets currently using Analogic's ADAM826 family of products and can be utilized to upgrade existing designs to 2 MHz performance where 14 bits are required.

Superior performance and ease-of-use make the ADC3110/ADC3111 the ideal solution for those applications requiring a sample-and-hold amplifier directly at the input to the A/D converter. Having the S/H amplifier integrated with the A/D converter benefits the system designer in two ways. First, the S/H has been designed specifically to complement the performance of the A/D converter; for example, the acquisition time, hold mode settling and droop rate have been optimized for the A/D converter, resulting in exceptional overall performance. Second, the designer achieves true 14-bit performance, avoiding degradation due to ground loops, signal coupling, jitter and digital noise introduced when separate S/H and A/D converters are interconnected. Furthermore, the accuracy, speed, and quality of the ADC3110/ADC3111 are fully ensured by thorough, computer-controlled factory tests of each unit.



Features

- 14-Bit Resolution
- 2 MHz Sampling Rate
- Signal-to-Noise Ratio: 84 dB
- Peak Distortion: –82 dB @ 100 kHz
- Total Harmonic Distortion: –76 dB @ 100 kHz
- High Input Impedance: $10^6\Omega$
- ADAM826-1 Footprint
- Ease-of-Use
- Built-in S/H Amplifier
- No Missing Codes
- Differential Linearity: ±0.75 LSB
- Integral Linearity: ±0.006%
- Binary, Offset Binary, or Two's Complement Coding Formats
- Electromagnetic/Electrostatic Shielding

Applications

- Radar
- Automatic Test Equipment
- Analytic Instrumentation
- Data Acquisition Systems
- Spectroscopy
- Seismic Instrumentation
- High Resolution Imaging

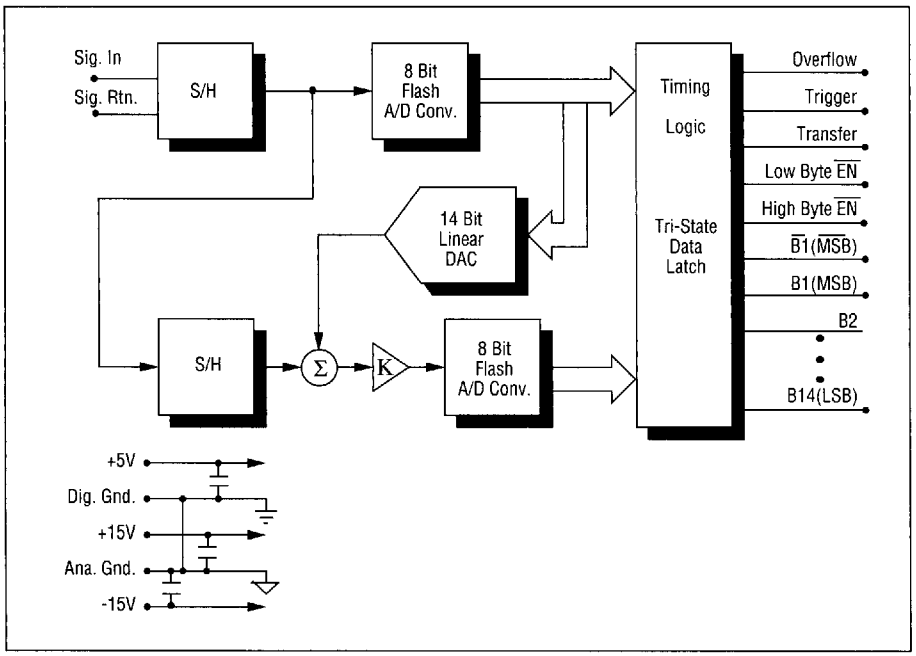


Figure 1. ADC3110/ADC3111 Block Diagram.

ANALOGIC®
The World Resource for Precision Signal Technology

ADC3110/ADC3111

Specifications [1]

ANALOG INPUT

Input Range
0V to +10V, ±2.5V, ±5V (see ordering guide)

Input Bias Current
50 µA Typ.

Input Capacitance
15 pF Max.

Input Resistance
1 MΩ Min.

DIGITAL INPUTS

Compatibility
CMOS, TTL

Logic Levels
Logic "0"
0.8V Max.

Logic "1'
2.0V Min.

Trigger
Positive Edge Triggered

Loading
1 TTL Load

Pulse Width
90 ns Min., 210 ns Max.

High Byte Enable
Active Low, O/U Flow, B1-B6, $\overline{B1}$

Low Byte Enable
Active Low, B7-B14

Propagation Delay
10 ns Max.

DIGITAL OUTPUTS

Fan-Out
1 TTL Load Max.

Logic Levels
Logic "0"
+0.4V Max.

Logic "1"
+2.4V Min.

Output Coding
0V to 5V
Binary

±2.5V, ±5V
Offset Binary, 2's Complement

Transfer Pulse [2]
Data Valid on Positive Edge

Over/Under Flow
Valid Data = Logic "0"

DYNAMIC CHARACTERISTICS

Maximum Throughput Rate
2 MHz Min.

S/H Aperture Delay
20 ns Max.

S/H Aperture Jitter
10 ps RMS Max.

S/H Feedthrough [3]
–85 dB Max.

Full Power Bandwidth
2 MHz Typ.

Small Signal Bandwidth
20 MHz Typ.

Signal-to-Noise Ratio (ADC3110) [4]
80 dB Min., 84 dB Typ.

Peak Distortion (ADC3110) [5, 11]
100 kHz
–82 dB Typ.

540 kHz
–76 dB Typ., –72 dB Max.

Total Harmonic Distortion (ADC3110) [6, 11]
100 kHz
–76 dB Typ.

540 kHz
–74 dB Typ., –72 dB Max.

THD + Noise (ADC3110) [7, 11]
100 kHz
–73 dB Typ.

540 kHz
–72 dB Typ., –69 dB Max.

Step Response (ADC3111) [8]
350 ns to 0.006% of final value

TRANSFER CHARACTERISTICS

Resolution
14 bits

Quantization Error
±0.5 LSB Max.

Integral Nonlinearity
±0.005% FSR Max.

Differential Nonlinearity
±0.75 LSB Max.

No Missing Codes
Guaranteed from 0°C to 60°C

Absolute Accuracy
±0.2% FSR Max.

Offset Error [9]
±5 mV Max.

Gain Error [9]
0.1% FSR Max.

Noise [10]
180 µV RMS Max.

STABILITY (0°C TO 60°C)

Nonlinearity
±2 ppm/°C Max., ±1 ppm/°C Typ.

Offset Voltage
±15 ppm/°C Max.

Gain
±15 ppm/°C Max.

Warm-Up Time
5 minutes Max.

Supply Rejection
Offset
±20 ppm FSR/% Typ.
±40 ppm FSR/% Max.

Gain
±20 ppm FSR/% Typ.
±40 ppm FSR/% Max.

POWER REQUIREMENTS [12]

±15V Supplies
14.5V Min., 15.5V Max.

+5V Supply
+4.75V Min., +5.25V Max.

+15V Current Drain
90 mA Typ.

–15V Current Drain
100 mA Typ.

+5V Current Drain
250 mA Typ.

Power Consumption
4.1W Typ.

ENVIRONMENTAL & MECHANICAL

Temperature Range Rated Performance
0°C to 60°C

Storage
–25°C to 80°C

Relative Humidity Non-Condensing
0 to 85% up to 60°C

Dimensions
3" x 5" x 0.44" (76.2 x 127 x 11.18 mm)

Shielding
Electromagnetic 5 sides, Electrostatic 6 sides

Case Potential
Ground

Specifications subject to change without notice.

Notes:

1. All specifications guaranteed at 25°C ambient with power of ±15V and +5V unless otherwise noted.
2. Setup time 25 ns typical, 10 ns Max.
3. Measured with a full scale 1 MHz input.
4. Signal-to-noise ratio represents the ratio of the RMS value of the signal to the total RMS noise below th Nyquist rate. Specification is characterized on ±5V range with a full scale input of 0 dB.
5. Peak distortion represents the ratio of the highest spurious frequency component below the Nyquist rate to the signal.
6. Total harmonic distortion represents the ratio of the RMS sum of all harmonics up to the 100th harmonic to the RMS value of the signal.
7. THD + noise represents the ratio of the RMS value of the signal to the total RMS noise below the Nyquist plus the total harmonic distortion up to the 100th harmonic.
8. Step response represents the time required to achieve the specified accuracies after a full scale step change.
9. Externally adjustable to zero.
10. Includes noise from S/H (hold mode) and A/D converter.
11. Specifications characterized on ±5V range, with an input at 10 dB below full scale.
12. Analogic highly recommends the use of linear power supplies with its high performance, high resolution A/D converters. However, if system requirements provide only a +5V supply and limited space, the use of the Analogic SP7015 DC-to-DC converter will provide a low noise solution which will not degrade the ADC3110/ADC3111 performance.

Coding and Trim Procedure

Figure 2 shows the output coding of the ADC3110/ ADC3111 A/D converter. The coding format for the ADC3110-M3/ ADC3111-M3 is unipolar binary. For the ADC3110-M4/ ADC3111-M4, the standard coding format is offset binary; the user can convert this coding to two's complement simply by using the available B1 (MSB) instead of $\overline{B1}$ ($\overline{MSB}$).

To trim the offset of the 0V to +5V unit, apply 152 µV to the analog input. Adjust the offset trim potentiometer such that the 13 MSBs are "0" and the LSB alternates equally between "0" and "1". To trim the offset of the bipolar ±5V (±2.5V) unit, apply –305 µV (–152 µV) to the analog input and adjust the offset trim potentiometer such that each of the 14 bits alternates equally between "0" and "1".

To trim the gain of the unipolar 0V to +5V unit, apply +4.999542V to the analog input and adjust the gain trim potentiometer such that the 13 MSBs are "1" and the LSB alternates equally between "0" and "1". To trim the gain of the bipolar ±5V (±2.5V) unit, apply +4.999085V (2.499542V) to the analog input and adjust the gain trim potentiometer such that the 13 MSBs are "1" (B1 in the case of two's complement, and the LSB alternates equally between "0" and "1".

Unipolar Binary		**0V to +5V**	**0V to +10V**
MSB	LSB		
1 1 1 1 1 1 1 1 1 1 1 1 1 1 =		+4.99969V	+0.99939V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 =		0.00000V	0.00000V
B1, B2,	B14 =	Pin Label	
Offset Binary		**±5V Input**	**±2.5V Input**
MSB	LSB		
1 1 1 1 1 1 1 1 1 1 1 1 1 1 =		+4.99939V	+2.49970V
1 0 0 0 0 0 0 0 0 0 0 0 0 0 =		0.0000V	0.00000V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 =		–5.0000V	–2.50000V
B1, B2,	B14 =	Pin Label	
2's Complement		**±5V Input**	**±2.5V Input**
MSB	LSB		
0 1 1 1 1 1 1 1 1 1 1 1 1 1 =		+4.99939V	+2.49970V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 =		0.0000V	0.00000V
1 0 0 0 0 0 0 0 0 0 0 0 0 0 =		–5.0000V	–2.50000V
B1, B2	B14 =	Pin Label	

Figure 2. Output Coding for the ADC3110/ADC3111.

Timing Considerations

The timing diagram in Figure 3 shows the timing characteristics of the ADC3110/ADC3111 A/D converter. Upon a low-to-high transition of the Trigger Input, the internal logic of the ADC3110/ADC3111 locks out any additional Trigger pulses until the next high-to-low transition of the Transfer pulse although care should still be taken not to inadvertently trigger the ADC before this time to prevent possible corruption of the succeeding conversion. At the time of the Trigger, the input S/H amplifier (see Figure 1) goes into the Hold mode. Approximately 175 ns later, the second S/H goes into the Hold mode with the input S/H amplifier returning to the Sample mode to begin acquiring the next sample. 10 ns prior to the low to high transition of the next transfer pulse, the data is valid.

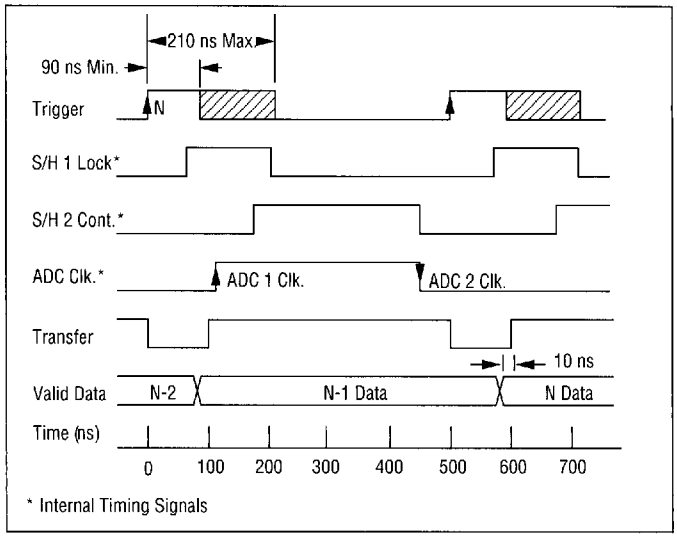


Figure 3. ADC3110/ADC3111 Timing Diagram.

Layout Considerations

Because of the high resolution of the ADC3110/ADC3111 A/D converter, it is necessary to pay careful attention to the printed circuit layout for the device. It is, for example, important to separate analog and digital grounds and to return them separately to the system power supply. Digital grounds are often noisy or "glitchy", and these glitches can have adverse effects on the performance of the ADC3110/ ADC3111 if they are introduced to the analog portions of the A/D converter's circuitry. At 14-bit resolution, the size of the voltage step between one code transition and the succeeding one is only 305 µV (610 µV for -M4 units), so it is evident that any noise in the analog ground return can result in erroneous or missing codes. It is therefore important to configure a low-impedance ground-plane return on the printed circuit board. This is the point where the Analog and Digital power returns should be made common, NOT at the supplies. Note that the ground-potential metal case used for the ADC3110/ADC3111 provides shielding against electromagnetic interference on five sides and against electrostatic interference on six sides.

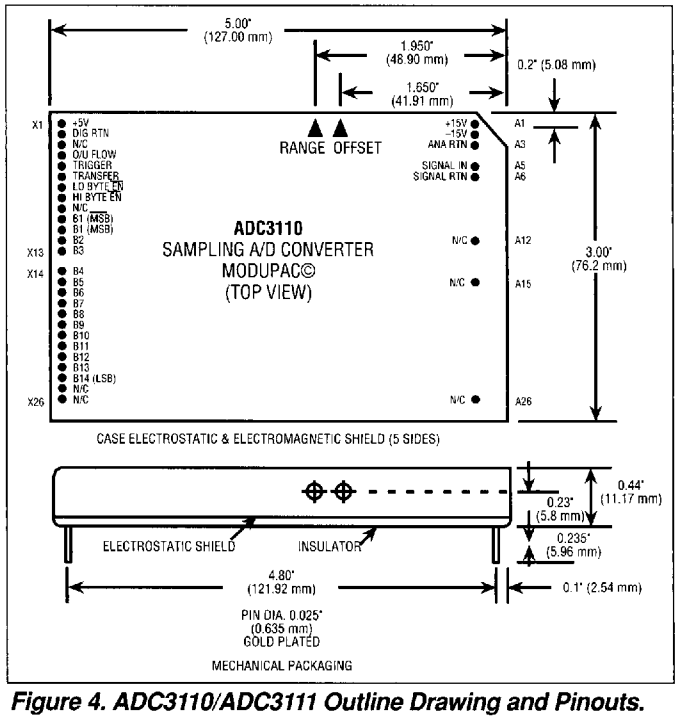


Figure 4. ADC3110/ADC3111 Outline Drawing and Pinouts.

PRINCIPLES OF OPERATION

The ADC3110/ADC3111 are 14-bit sampling A/D converters with throughput rates to 2 MHz, and two internally configurable input ranges. The ADC 3110/ ADC3111M-3 is 0V to +5V and the ADC3110/ADC3111M-4 is ±5V.

To understand the operating principles of the ADC3110/ ADC3111 A/D converter, refer to Figures 3 and 5. The simplified block diagram of Figure 5 illustrates the two successive passes in the sub-ranging conversion scheme of the ADC3110/ADC3111. The scale factors and voltages used in the details are that of the ±5V unit. Numbers in parenthesis are those of the +5V unit.

The first pass starts at a low-to-high transition of the trigger pulse. This signal directly places S/H 1 into the Hold mode and starts the timing logic. S/H 1 will stay in the Hold mode only as long as the trigger pulse remains high; therefore the internal logic generates a S/H 1 lock command 90 ns after the trigger, locking S/H 1 into the Hold mode allowing the trigger signal to return low and locking out any further trigger commands until the end of the first pass. In the first pass, the output of S/H 1 is attenuated by a factor of 5 (2.5) to convert the 10V (5V) full scale range to the 2V full scale range of ADC 1. After 110 ns, S/H 1 and the attenuator have settled to 9-bit accuracy at which time ADC 1 digitizes the first pass. The eight bits take two paths, to the internal logic and to the eight most significant bits of a 14-bit accurate D/A converter. At 175 ns after trigger, S/H 1 has settled to 14-bit accuracy and S/H 2, now placed in Hold, has also acquired to 14-bit accuracy. The purpose of S/H 2 is to allow S/H 1 to now return to the Sample mode and begin acquiring new data while S/H 2 is holding for the second pass.

In the second pass, the output of the D/A converter is subtracted from the output of S/H 2. The maximum error voltage of ±0.5 LSB at the 8-bit level is 10V/256 (5V/256) or 39 mV (19.5 mV) is amplified by 12.8 (25.6) to achieve 1/4 full scale range of ADC 2 thus allowing a 2-bit overlap safety margin. The effective resolution therefore becomes 6 + 8, or 14 bits. At 450 ns after trigger, the error signal has settled to 14-bit accuracy. ADC 2 now digitizes the second pass and S/H 2 goes into the Sample mode. At 500 ns after trigger, the converter can now begin the next conversion but the data from the previous conversion is not yet latched into the output registers. This occurs at 10 ns prior to a low-to-high transition of the transfer pulse or at 590 ns after trigger.

The ADC3110/ADC3111 has a tri-state output structure. Users can enable the six MSBs, $\overline{B1}$, and the Overflow/ Underflow bit with the HI BYTE EN pin and the eight LSBs with the LO BYTE EN pin, (both are active low). This feature makes it possible to transfer data from the ADC3110/ ADC3111 to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered, (see Figure 10).

1/4 full scale range, or 2-bit overlap in the second pass, is a scheme used in the ADC3110/ADC3111 to provide an output word that is accurate and linear to 14 bits. This method corrects for any gain and linearity errors in the amplifying circuitry, as well as in the 8-bit flash ADC 1 A/D converter. Without the use of this overlapping correction scheme, it would be necessary that all the components in the ADC3110/ADC3111 be accurate to the 14-bit level. While such a design might be possible to realize on a laboratory benchtop, it would be clearly impractical to achieve on a production basis. The key to the conversion technique used in the ADC3110/ADC3111 is the 14-bit accurate and 14-bit linear D/A converter, which serves as the reference element for the conversion's second pass. The use of the proprietary sub-ranging architecture in the ADC3110/ ADC3111 results in a sampling A/D converter that offers unprecedented speed and transfer characteristics at the 14-bit level.

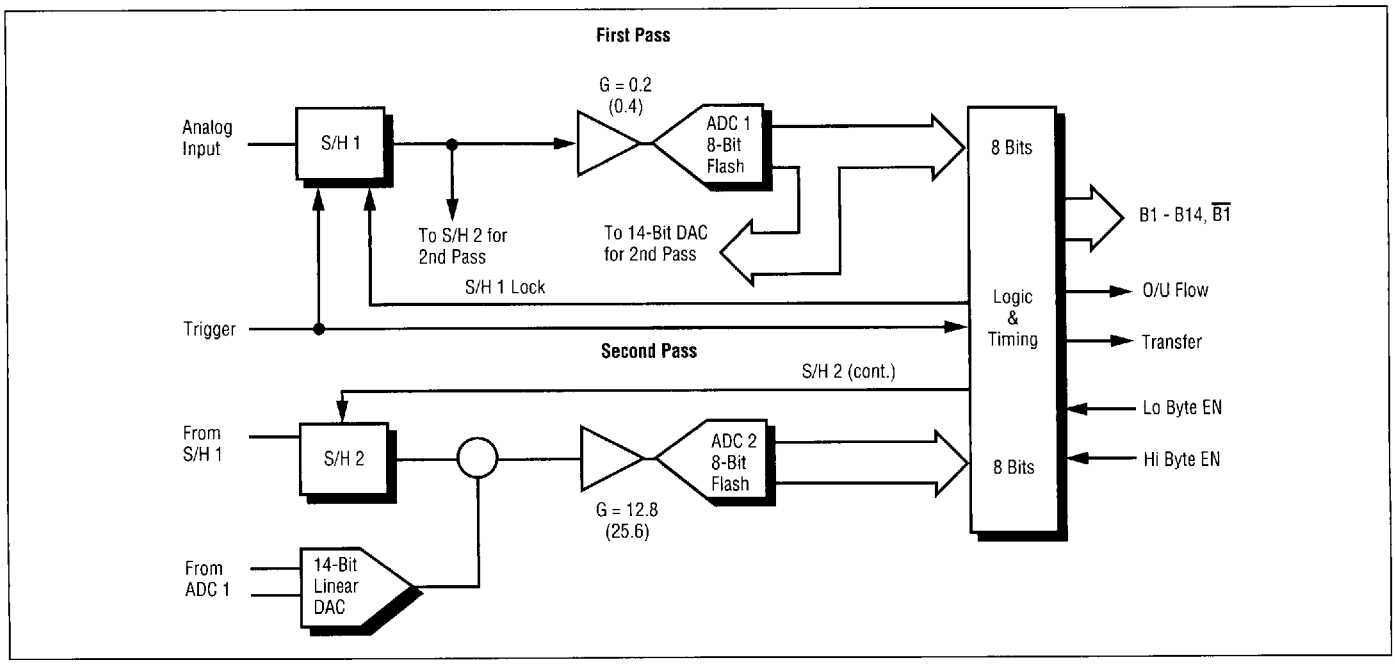


Figure 5. Operating Principle of the ADC3110/ADC3111.

ADC3110/ADC3111 PERFORMANCE TESTING

In order to guarantee that all ADC3110/ADC3111s shipped meet or exceed published specifications, Analogic takes great efforts in performing a multitude of tests on each module prior to shipment. Such results are then sent to the customer in conjunction with each ADC3110/ADC3111 as a testimony of the performance results.

Amplitude Domain Testing

The Amplitude Domain Testing is performed by means of proprietary Automatic Test Equipment inclusive of a 22-bit digital-to-analog converter, whose reference is traceable to the National Institute of Standards Technology. A block diagram is outlined in Figure 6. By means of this test equipment, Analogic can test such parameters as integral linearity, differential linearity, A/D converter noise, maximum positive and negative errors, conversion time, gain error, offset error, power supply current, and power supply rejection. A typical "Amplitude Domain" data sheet is shown in Figure 7. For further information on the definitions of such specifications, please refer to the "Analogic Data Conversion Systems Digest".

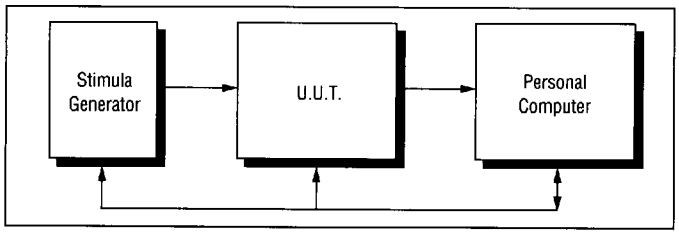


Figure 6. "Amplitude Domain" Test System.

Frequency Domain Testing

This test is performed to simulate, as much as possible, real-time applications where a constantly varying input signal is applied to the ADC3110. A block diagram of Analogic's "Frequency Domain" test system is shown in Figure 8. As a result, a data sheet, such as the one reproduced in Figure 9, is delivered to the customer with each ADC3110.

The data sheet is divided into two sections including the nature of the input data, the type of FFT performed and the results of the FFT test. This data can possibly be misleading if not thoroughly understood. For example, in an audio application, one of the most important parameters is the absence of aliased harmonic distortion. While harmonic distortion directly related to the fundamental does not produce audible discomfort, aliased harmonics can be very bothersome. Such specification is not often provided nor is calculated as part of the total harmonic distortion, and thus misleading the end user. Analogic definitions are summarized as follows:

Peak Distortion: Ratio, expressed in dB, between the RMS value of the highest spurious spectral component below the Nyquist rate and the RMS value of the input signal.

$$\text{Peak Distortion} = \frac{20 \log \text{ RMS value of max. spurious component}}{\text{RMS value of input signal}}$$

Signal-to-Noise Ratio: Ratio, expressed dB, between the RMS value of the signal and the total RMS noise below the Nyquist rate.

Total Harmonic Distortion: Ratio, expressed in dB, between the RMS sum of all the components below the Nyquist rate that are harmonically related to the signal and the RMS value of the signal.

Direct Harmonic Distortion: Ratio, expressed in dB, between the RMS sum of all the components below the Nyquist rate that are harmonically related to the signal and the RMS value of the signal.

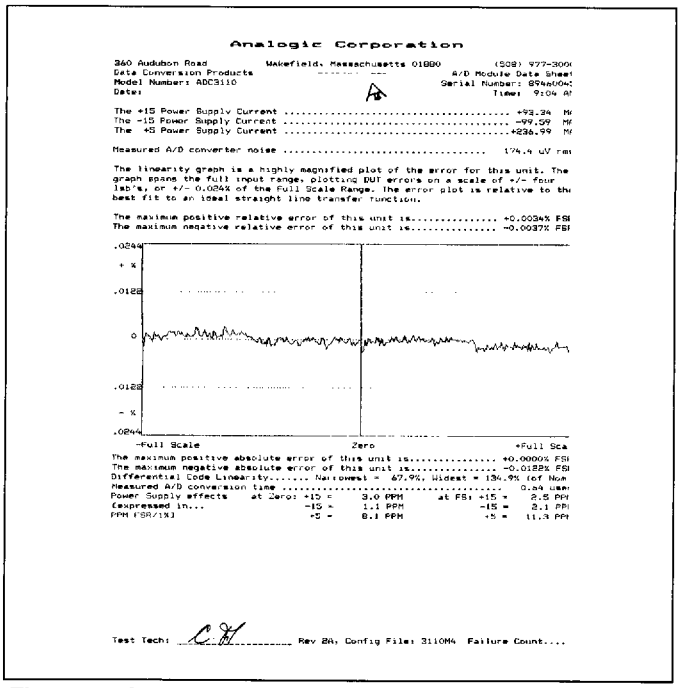


Figure 7. "Amplitude Domain" Data Sheet.

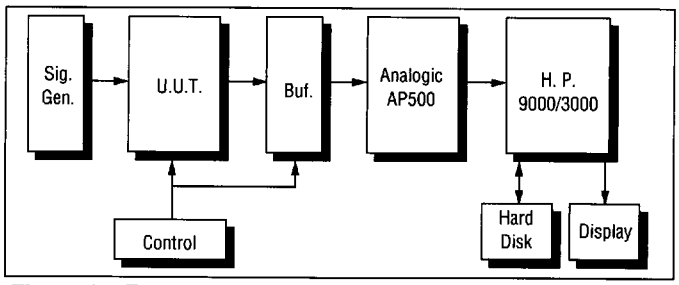


Figure 8. "Frequency Domain" Test System.

Reflected Harmonic Distortion: Ratio, expressed in dB, between the RMS sum of all aliased harmonics and the RMS value of the signal.

Note that the estimated RMS noise, based on those frequency bins not correlated with the test signal, is first removed from the harmonic frequency bins before the above distortion values are calculated.

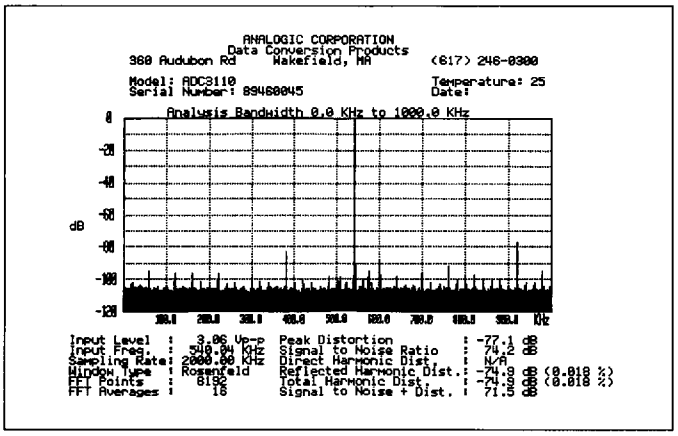


Figure 9. "Frequency Domain" data sheet.

TYPICAL APPLICATION

Figure 10 shows a typical application circuit for the ADC3111 A/D converter: an 8-channel, high resolution, high speed data acquisition system tied into an 8-bit Bus. This circuit could be part of an automatic test system or the front end of a data acquisition and control system. The 14-bit resolution of the ADC3111 provides 84 dB dynamic range for each channel, and the 2 MHz throughput rate provides approximately 250 kHz throughput per channel.

For interlacing with a 16-bit Bus, the Tri-state latch is no longer necessary but the use of digital buffers may still be required to prevent coupling of high frequency noise from the microprocessor bus into the A/D converter. Note that in Figure 10, the signal return is NOT tied to the ground-plane return but instead is common at a strategic point inside the ADC3110/ADC3111.

The ability of the ADC3111 Sample-and-Hold amplifier to acquire new data to within ±1 LSB after a full scale step change at the analog input, and the superb DC characteristics exhibited by the ADC3111 are the key factors in establishing this part as the ideal choice for high speed data acquisition systems. The addition of an input buffer may be required to minimize the channel-to-channel offset that may occur due to input bias currents. A channel-to-channel "on resistance" difference of 6Ω will create a 1 LSB offset difference (50 µA x 6Ω = 300 µV). It should be noted that for single channel applications, the ADC3110 Sample-and-Hold amplifier has been optimized for lower distortion.

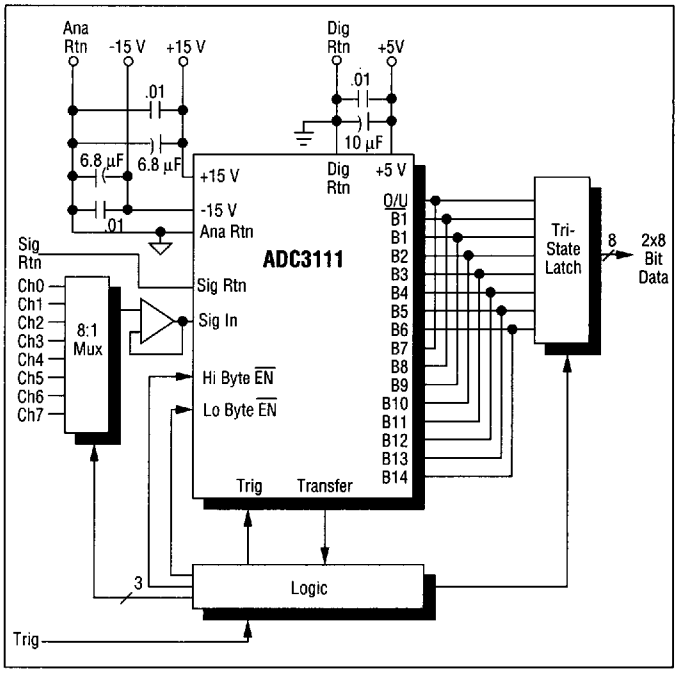


Figure 10. Typical Single-Ended Application Circuit and Connection to an 8-bit Bus.

Ordering Guide

ADC311 -M

0 — Frequency Domain
1 — Time Domain
1 — 0V to +10V
3 — 0V to +5V input
4 — ±5V input
6 — ±2.5V input

DC-to-DC Converter SP7015

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