# Octal D-type transparent latch with 5-volt tolerant inputs/outputs; damping resistor; 3-state

## 74LVC2573A
## 74LVCH2573A

## FEATURES

- **5-volt tolerant inputs/outputs, for interfacing with 5-volt logic.**
- **Wide supply voltage range of 2.7 V to 3.6 V.**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Flow-through pin-out architecture**
- **Bushold on all data inputs (LVCH2573A only).**
- **Integrated 30Ω damping resistor.**

## DESCRIPTION

The 74LVC(H)2573A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment. The 74LVC(H)2573A is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable (OE) input are common to all internal latches. The '2573' consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the $D_n$ inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When OE is LOW, the contents of the eight latches are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the latches.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f \leq 2.5$ ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | propagation delay $D_n$ to $Q_n$; LE to $Q_n$ | $C_L$ = 50 pF $V_{CC}$ = 3.3 V | 4.4 5.0 | ns |
| $C_I$ | input capacitance | | 5.0 | pF |
| $C_{PD}$ | power dissipation capacitance per latch | notes 1 and 2 | 20 | pF |

### Notes to the quick reference data

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   $f_i$ = input frequency in MHz; $C_L$ = output load capacity in pF;
   $f_o$ = output frequency in MHz; $V_{CC}$ = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_I$ = GND to $V_{CC}$.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGES | | | |
|---|---|---|---|---|
| | PINS | PACKAGE | MATERIAL | CODE |
| 74LVC(H)2573AD | 20 | SO | plastic | SOT163-1 |
| 74LVC(H)2573ADB | 20 | SSOP | plastic | SOT339-1 |
| 74LVC(H)2573APW | 20 | TSSOP | plastic | SOT360-1 |

## PINNING

| PIN | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | OE | output enable input (active LOW) |
| 2, 3, 4, 5, 6, 7, 8, 9 | $D_0$ to $D_7$ | data inputs |
| 19, 18, 17, 16, 15, 14, 13, 12 | $Q_0$ to $Q_7$ | 3-state latch outputs |
| 10 | GND | ground (0 V) |
| 11 | LE | latch enable input (active HIGH) |
| 20 | $V_{CC}$ | positive supply voltage |

The '2573' is functionally identical to the '2373', but the '2373' has a different pin arrangement.

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Fig.1 Pin configuration.
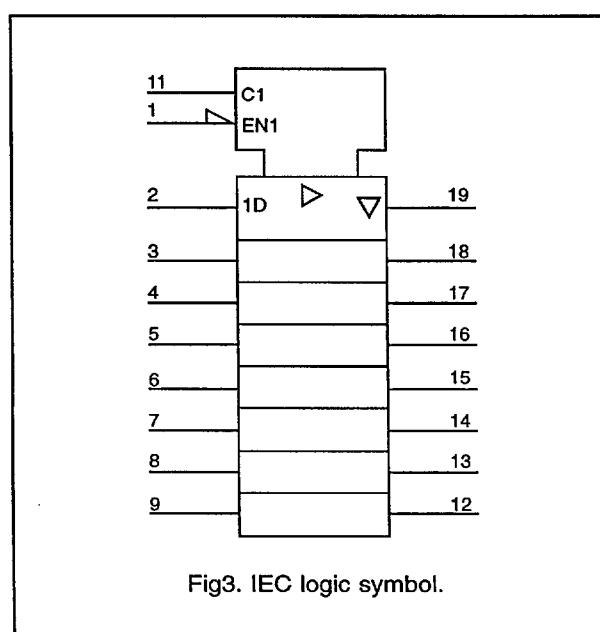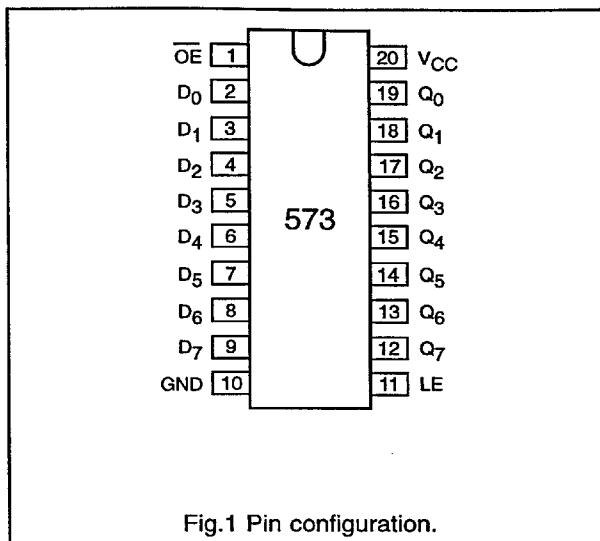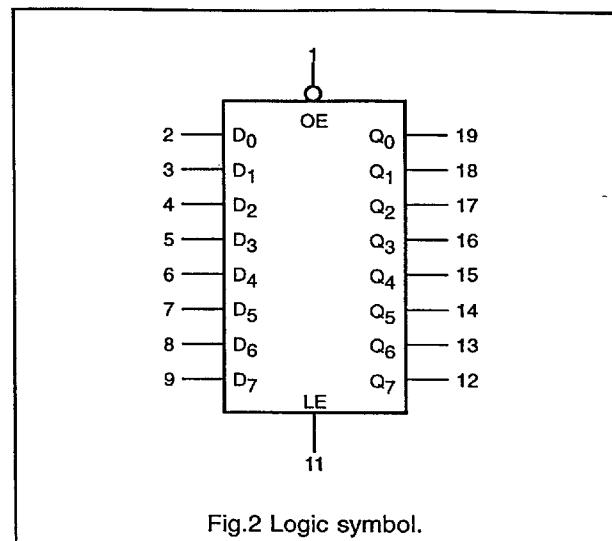


Fig.2 Logic symbol.



Fig3. IEC logic symbol.
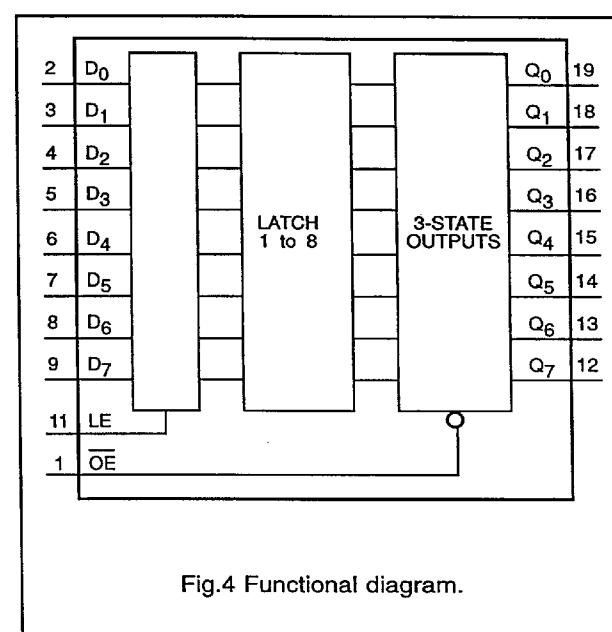


Fig.4 Functional diagram.
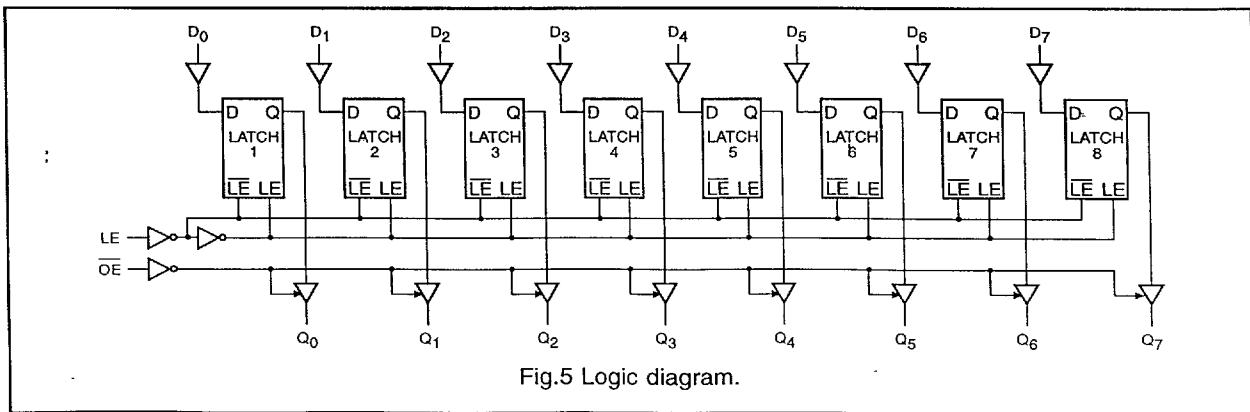


Fig.5 Logic diagram.

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### FUNCTION TABLE

| OPERATING MODES | INPUTS | | | INTERNAL LATCHES | OUTPUTS |
| --- | --- | --- | --- | --- | --- |
| | $\overline{OE}$ | LE | $D_n$ | | $Q_0$ to $Q_7$ |
| enable and read register (transparent mode) | L | H | L | L | L |
| | L | H | H | H | H |
| latch and read register | L | L | l | L | L |
| | L | L | h | H | H |
| latch register and disable outputs | H | L | l | L | Z |
| | H | L | h | H | Z |

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

### DC CHARACTERISTICS FOR 74LVC(H)2573A
For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".

### AC CHARACTERISTICS FOR 74LVC(H)2573A
GND = 0 V; $t_r = t_f \le 2.5$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | UNIT | TEST CONDITIONS | |
| --- | --- | --- | --- | --- | --- | --- | --- |
| | | −40 to +85 | | | | $V_{cc}$ (V) | WAVEFORMS |
| | | MIN. | TYP. | MAX. | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay $D_n$ to $Q_n$ | −<br>1.5<br>1.5 | 21<br>4.7<br>4.3* | −<br>9.5<br>8.5 | ns | 1.2<br>2.7<br>3.0 to 3.6 | Figs 6, 10 |
| $t_{PHL}/t_{PLH}$ | propagation delay LE to $Q_n$ | −<br>1.5<br>1.5 | 23<br>5.3<br>4.6* | −<br>11<br>9.5 | ns | 1.2<br>2.7<br>3.0 to 3.6 | Figs 7, 10 |
| $t_{PZH}/t_{PZL}$ | 3-state output enable time $\overline{OE}$ to $Q_n$ | −<br>1.5<br>1.5 | 17<br>4.4<br>3.8* | −<br>11<br>9.0 | ns | 1.2<br>2.7<br>3.0 to 3.6 | Figs 8, 10 |
| $t_{PHZ}/t_{PLZ}$ | 3-state output disable time $\overline{OE}$ to $Q_n$ | −<br>1.5<br>1.5 | 8.0<br>4.0<br>3.5* | −<br>6.5<br>6.0 | ns | 1.2<br>2.7<br>3.0 to 3.6 | Figs 8, 10 |
| $t_w$ | LE pulse width HIGH | −<br>− | 3.0<br>3.0* | −<br>− | ns | 2.7<br>3.0 to 3.6 | Fig.7 |
| $t_{su}$ | set-up time $D_n$ to LE | 1.0<br>1.0 | 0.2<br>0.2* | −<br>− | ns | 2.7<br>3.0 to 3.6 | Fig.9 |
| $t_h$ | hold time $D_n$ to LE | 1.0<br>1.0 | 0<br>0* | −<br>− | ns | 2.7<br>3.0 to 3.6 | Fig.9 |

**Notes:** All typical values are measured at $T_{amb} = 25$ °C.
\* Typical values are measured at $V_{cc} = 3.3$ V.

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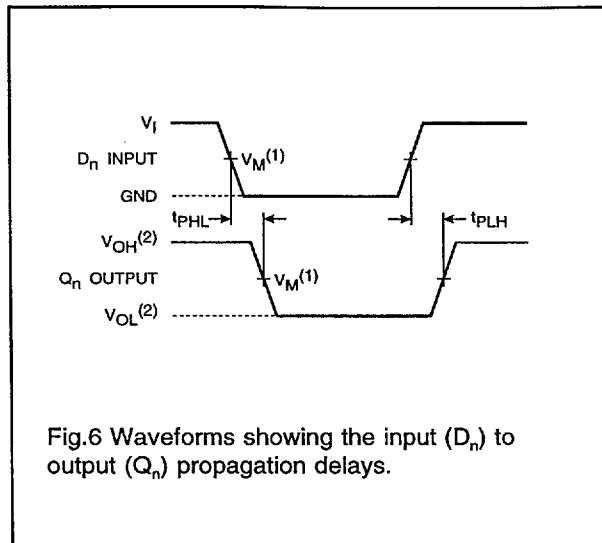
## AC WAVEFORMS

Fig.6 Waveforms showing the input (D$_n$) to output (Q$_n$) propagation delays.
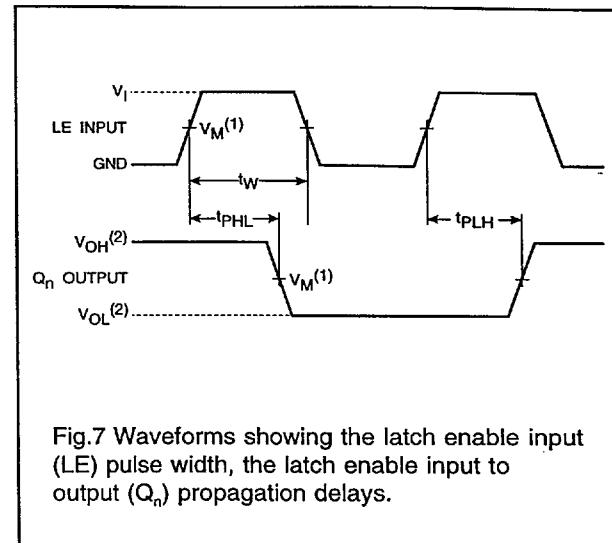
Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q$_n$) propagation delays.
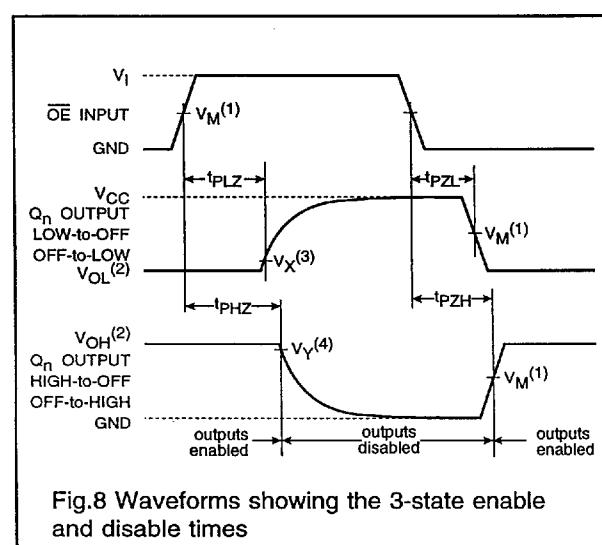
Fig.8 Waveforms showing the 3-state enable and disable times
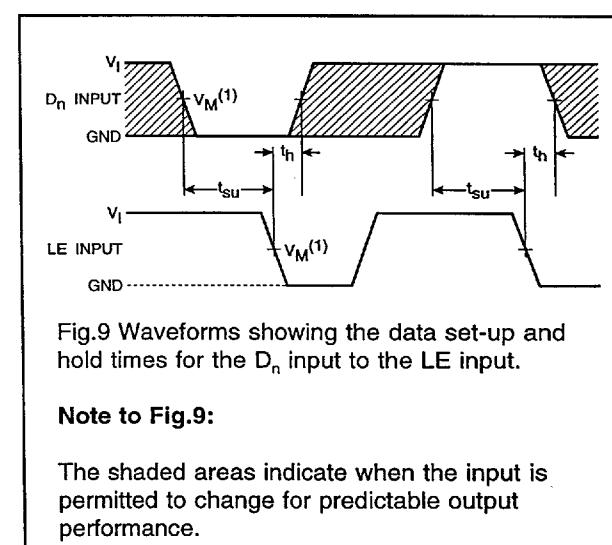
Fig.9 Waveforms showing the data set-up and hold times for the D$_n$ input to the LE input.

**Note to Fig.9:**

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.10 Load circuitry for switching times.

| V$_{CC}$ | V$_I$ |
|---|---|
| < 2.7 V | V$_{CC}$ |
| 2.7 - 3.6 V | 2.7 V |

| Test | S$_1$ |
|---|---|
| t$_{PLH}$/t$_{PHL}$ | Open |
| t$_{PLZ}$/t$_{PZL}$ | 2 • V$_{CC}$ |
| t$_{PHZ}$/t$_{PZH}$ | GND |

**Notes:**

(1) V$_M$ = 1.5 V at V$_{CC}$ ≥ 2.7 V
V$_M$ = 0.5 · V$_{CC}$ at V$_{CC}$ < 2.7 V

(2) V$_{OL}$ and V$_{OH}$ are the typical output voltage drop that occur with the output load

(3) V$_X$ = V$_{OL}$ + 0.3 V at V$_{CC}$ ≥ 2.7 V
V$_X$ = V$_{OL}$ + 0.1 · V$_{CC}$ at V$_{CC}$ < 2.7 V

(4) V$_Y$ = V$_{OH}$ – 0.3 V at V$_{CC}$ ≥ 2.7 V
V$_Y$ = V$_{OH}$ – 0.1 · V$_{CC}$ at V$_{CC}$ < 2.7 V

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