VITESSE

Product Preview

VSP945/VSP946

High Performance Pentium™ Processor Cache Controller with i486-Compatible System Interface

FEATURES

- Optimizes Pentium™ Processor Performance
- Zero Wait States: 2–1–1–1 Read/Write Back
- 66-MHz Operation with Migration Path to 80-MHz
- Cache Sizes Supported: 128K, 256K, 512K, and 1MByte
- Uses Standard Asynchronous SRAMs for Tag & Data Storage
- Supports up to 32K Tag Entries, 1GByte Cacheable Memory
- A 33 MHz, 32-bit, i486™-Compatible System Bus Interface
- 4-Deep Write Buffer to Eliminate Cache Miss Penalty
- Snoop Filtering to Reduce CPU Stalls
- Read By-Pass to Streamline CPU Operation
- Software Transparent -- No BIOS to Configure
- Optional Upgrade Path
- Simplified Clock and Address Signal Distribution
- TTL Compatible Inputs and Outputs
- +5, +2 Volt Power Supplies
- Low Power System Solution
- Power Dissipation: 5 Watts (Max)
- VSP945: Thermally Enhanced 184 Plastic Quad Flat Package
- VSP946: Thermally Enhanced 208 Plastic Quad Flat Package

FUNCTIONAL DESCRIPTION

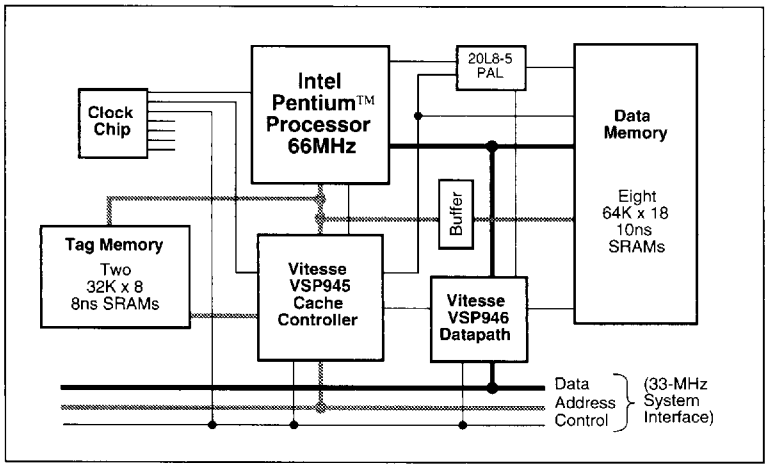
Vitesse's VSP945 is a high performance serial cache controller specifically designed for use in uniprocessor systems based on the Intel Pentium™ processor. The VSP945 is intended to be used in conjunction with the VSP946 Datapath Chip, also from Vitesse. The complete chipset provides all of the control functions to implement a second-level copy-back cache subsystem up to 1MByte in size.

The high speed VSP945 allows the system designer to use standard asynchronous SRAMs for Tag and Data storage while allowing the processor to run at full speed (zero wait-states). The VSP945 integrates all cache management functions for bus arbitration between the processor and main memory. In addition, the VSP945 provides bursting reads and writes on both the CPU bus and system bus, as well as providing an advanced bus snooping mechanism. A 4-deep write buffer supports zero-wait-state operation on write-miss cycles as well as supporting concurrent copy-back operation. The chip is configured to allow the designer to specify cache sizes of 128K, 256K, 512K, or 1MByte.

In addition to controlling the address and tag data directly, the VSP945 interfaces with the VSP946 Datapath Chip to provide control for data and parity on the processor bus. The VSP946 Datapath Chip provides a buffer function for the datapath between the system bus and processor.

The VSP945 provides significant power and cost savings by allowing the designer to use commodity SRAMs for tag entries and data storage, compared to other solutions that require special SRAMs. The system bus interface simplifies system integration and provide a wide range of price/performance targets. For high performance servers and PCs operating at 66-MHz, the VSP945 provides the highest system performance level at the lowest cost. Planned upgrades will offer the same solution for systems operating at 80-MHz and beyond.

1MBYTE CACHE SIMPLIFIED SYSTEM DIAGRAM (66-MHZ)



CACHE CONFIGURATION

Size	*Tag RAM*	*Data RAM*
128 KB	2: 8Kx8	16: 8Kx8
256 KB	2: 8Kx8	32:8Kx8
512 KB	2: 32Kx8	16: 32Kx8
1,024 KB	2: 32Kx8	8: 64Kx16

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741 Calle Plano, Camarillo, CA 93012 • (805) 388-3700 • FAX (805) 987-5896