

January 1993

DESCRIPTION

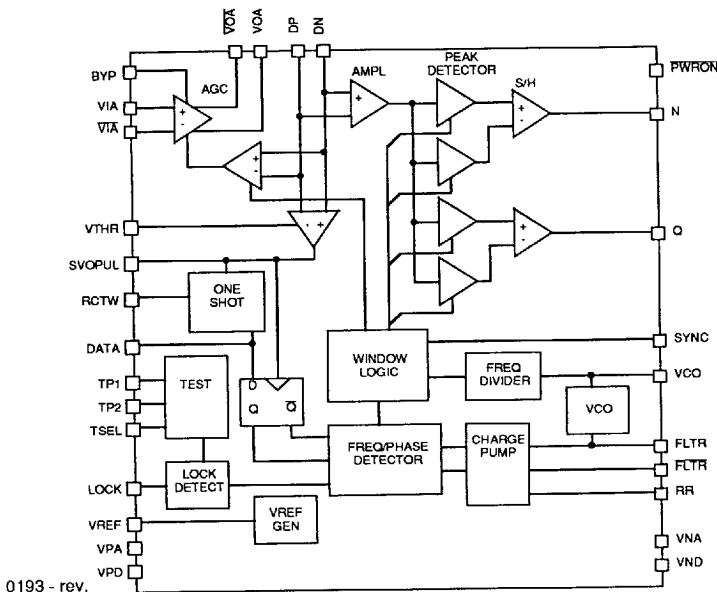
The SSI 32H6215 Servo Demodulator is a BiCMOS device intended for use in Winchester disk drives with dedicated surface head positioning systems. It processes a di-bit quadrature pattern read from the servo surface by a preamplifier, such as the SSI 32H6110, and generates normal and quadrature (N and Q) position reference signals. These signals provide the servo controller with position error feedback. A complete position control system can be realized with the SSI 32H6215 and its companion device, the SSI 32H4633 Servo Controller and Servo Motor Pre-Driver.

The SSI 32H6215 incorporates an input amplifier with automatic gain control and offset cancellation, a phase locked loop and sync separator to recover timing information, and pulse peak detectors to recover the position information. External components are used to set the operating characteristics of the SSI 32H6215, such as AGC response, VCO center frequency, PLL response and sync separator threshold. Its high performance analog/digital circuitry is capable of supporting servo frame rates of up to 500 kHz.

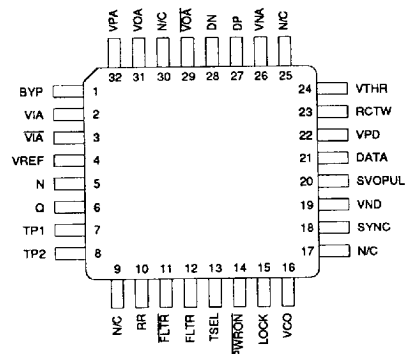
FEATURES

- Servo signal demodulation for dedicated surface head positioning systems
- Supports industry standard di-bit quadrature servo pattern with frame rates up to 500 kHz
- N, Q outputs convey track crossing and position error information
- PLL for timing recovery and synchronization
- Adjustable sync separator threshold
- AGC reference level adjustment
- Precision bandgap voltage reference output
- Advanced BiCMOS process dissipates less than 200 mW (5V)
- Available in 32-lead TQFP package

BLOCK DIAGRAM



PIN DIAGRAM



32-Lead TQFP

8253965 0009883 050 SII

SSI 32H6215

Servo Demodulator

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA	-	Analog Supply: 5V power supply.
VPD	-	Digital Supply: 5V power supply.
BYP	-	AGC Bypass: AGC bypass capacitor.
VOA	O	AGC Output: AGC analog output
VOA	O	AGC Output: AGC analog output.
DP	O	Differential Positive Input: Positive input of peak detect circuit.
DN	O	Differential Negative Input: Negative input of peak detect circuit.
VNA	-	Analog Ground.
VND	-	Digital Ground.
VTHR	-	Pulse Threshold: A resistor which sets a threshold for SYNC and DATA pulse detection must be connected between this pin and VCC (digital 5V supply).
SVOPUL	O	Servo Output Level.
RCTW	-	RC Timing Window: A resistor and capacitor must be connected in parallel between this pin and analog ground to set a timing window which is used in detecting SYNC pulses.
DATA	O	Data Output: Active high TTL compatible digital output that indicates the presence of a data pulse in the servo frame. This signal is updated on the falling edge of the sync pulses.
TP1	I/O	Test Point 1.
TP2	I/O	Test Point 2.
TSEL	I	Test Select.
PWRON	I	Power On: Active low power on input.
LOCK	O	Lock Output: An open collector output that indicates the lock status of the PLL.
SYNC	O	Sync Output: TTL compatible digital clock whose falling edge indicates the presence of valid analog signal on the N and Q outputs. There is one SYNC cycle per servo frame.
VCO	O	VCO Output: TTL compatible digital clock which is 32 times the sync frequency (servo frame).
FLTR	-	Phase Lock Loop Filter: An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground.
FLTR	-	Phase Lock Loop Filter: An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground.
VREF	O	Reference Voltage: All analog voltages are referenced to this voltage.

SSI 32H6215 Servo Demodulator

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
N	O	N Output: This sampled and held analog output is the normal position reference output. N is referenced to VREF and is periodic in radial displacement with a period of 4 tracks.
Q	O	Q Output: This sampled and held analog output is the quadrature position reference output. Q is referenced to VREF and is periodic in radial displacement with a period of 4 tracks.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
VCC voltage	0 to 8V
VPA voltage	0 to 8V
Voltage on PLL inputs	-0.5 to VCC + 0.5V
Voltage on other inputs	0 to 8V
Storage Temp.	-45 to 160°C
Solder Temp. 10 sec. duration	260°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VPA, analog voltage		4.5		5.5	V
Supply noise				0.1	Vpp
VCC, digital supply		4.5		5.5	V
Ta, ambient temperature		0		70	°C
VCO operating range				16	MHz
Load resistance		10			kΩ
Load capacitance				50	pF

DC CHARACTERISTICS

IPA, VPA current				30	mA
ICC, VCC current				20	mA
Sleep current	IPA + ICC			0.5	mA
VOH, digital output high		2.4			V
VOL, digital output low				0.5	V
IREF, VREF output current capacity		10			mA
VREF output voltage					V

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Servo Demodulator

AGC AMPLIFIER

Input signals are AC coupled to VIA/\overline{VIA} , VOA/\overline{VOA} outputs are AC coupled to DP/DN. A 1000 pF capacitor (CBYP) is connected from BYP to VCA. Unless otherwise specified outputs are measured differentially at VOA/\overline{VOA} , $F_{IN} = 4$ MHz.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Range		25		375	mVpp
DP-DN Voltage	$VIA - \overline{VIA} = 0.1V_{pp}$	0.9		1.1	Vpp
DP-DN Voltage variation	$25mV < VIA - \overline{VIA} < 375mV$			8	%
Gain Range		2.5		40	V/V
Differential input impedance		4.7	6	8.4	k Ω
Single ended input impedance			3.3		k Ω
Output offset voltage	Gain = 22	-200		200	mV
Input noise voltage	Gain = 22, VIA/\overline{VIA} short		10		nV/ \sqrt{Hz}
CMRR	Gain = 22, $f_c = 5MHz$	40			dB
PSRR	Gain = 22, $f_c = 5MHz$	45			dB
Single ended output resistance			150		Ω

AGC CONTROL

The input signals are AC coupled into DP/DN, CBYP = 1000 pF to VPA.

Decay current	Normal delay (ID)		4		μA
Attack current	Normal attack (ICH)		0.18		mA
BYP Leakage current		-10		10	nA

VOLTAGE REFERENCE

Voltage		1.9	2	2.1	V
Output Impedance				20	Ω
Output current capability		-0.5		5	mA

N,Q OUTPUTS

Output impedance				250	Ω
Volts per track		0.9	1	1.1	V/track
Offset voltage				20	mV

ELECTRICAL SPECIFICATIONS (continued)

VCO

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCO center frequency f_c		TBD		TBD	MHz
Frequency dynamic range VCO		± 25		± 45	%
VCO control gain KVCO		0.14 ω_i		0.26 ω_i	Rad/(V-s)
Phase detector gain constant KD		0.83 KD		1.17 KD	A/rad
KVCO x KD product accuracy		-28		28	%
VCO output frequency f_{VCO}				16	MHz
Precision external resistor RR			12.5		k Ω

VALID PULSE DETECTOR

Input voltage range Vsd	At, DP, DN	0.9	1	1.1	Vpp
Threshold voltage Vthr	Resistor divider from VPA to Vref	Vref			V
Threshold input current Ithr	DP, DN shorted, Vth r= Vref + 0.5V			TBD	μ A
Detector zero crossing Tdp	Vsd=1.1Vpp Measured at SVOPUL T.P.			TBD	nsec

SYNC SEPARATOR

Timing window Tw	Rw(Ω), Cw(F)		0.92 RwCw		Sec
Window resistance Rw		10			k Ω
RCTW output low voltage Vol				0.1	V

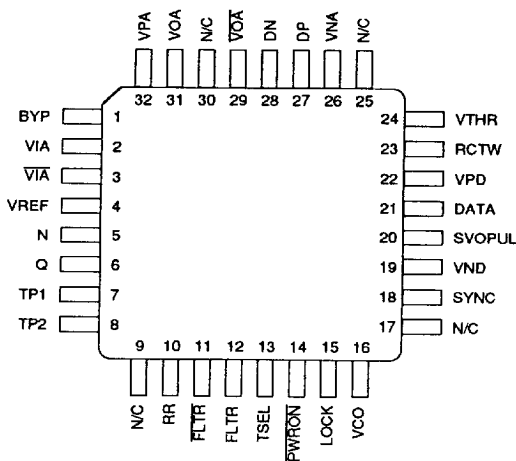
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Servo Demodulator

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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