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# SSI 32D5391

## Data Sync/1, 7 RLL ENDEC with Write Precomp. and Window Shift

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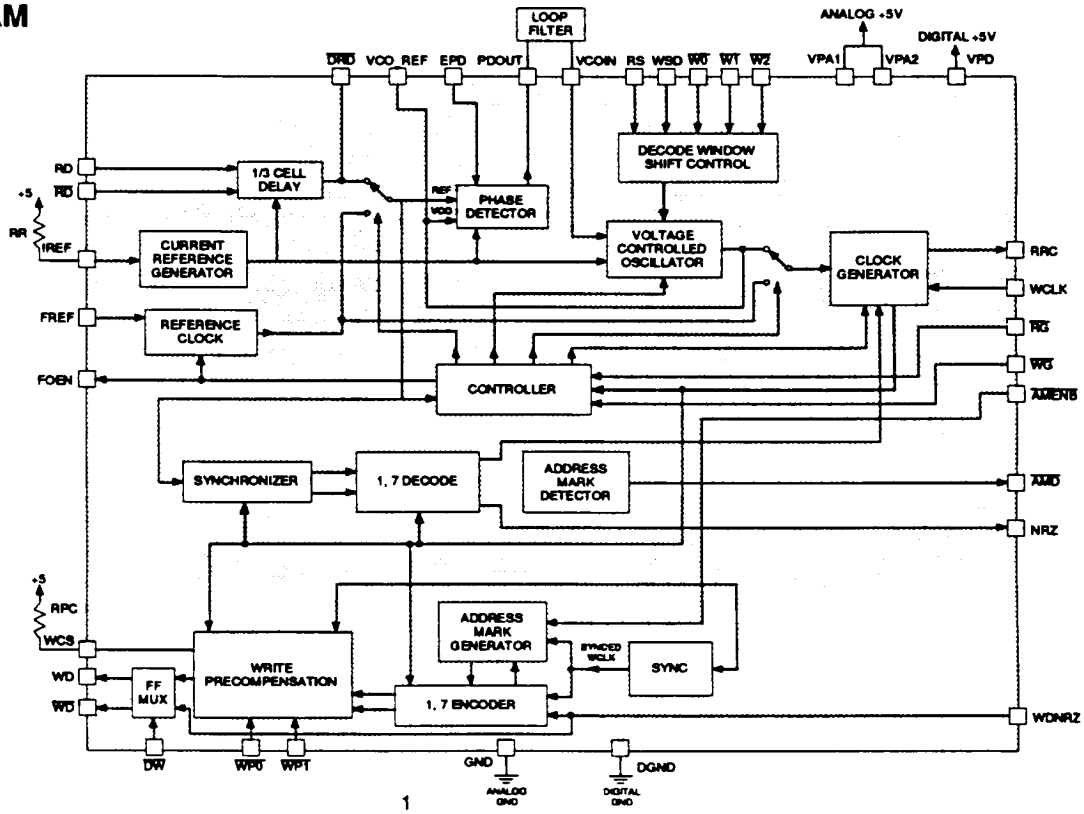
## DESCRIPTION

The SSI 32D5391 Data Synchronizer/1, 7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 1, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The VCO frequency setting elements are incorporated within the SSI 32D5391 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5391 utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of external devices. The SSI 32D5391 requires a single +5V supply.

## FEATURES

- **Data synchronizer and 1, 7 RLL ENDEC**
- **24 to 40 Mbit/s operation**
  - **Data rate programmed with a single external resistor or current source**
- **Direct write capability**
- **Fast acquisition phase locked loop with improved zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable decode window symmetry control**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Uses standard 5V ± 5% supply**
- **44-pin PLCC package**

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### DATA/CLOCK RECOVERY CIRCUIT

The circuit is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1, 7 RLL encoding format. In the read mode the circuit performs data synchronization, sync field search and detect, address mark detect, and data decoding. In the write mode, the circuit converts NRZ data into the 1, 7 RLL format described in Table 1, performs write precompensation, generates the preamble field and inserts address marks as requested.

This data rate is established by a single 1% external resistor, RR, connected from the IREF pin to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = (185/DR) - 1.7\ k\Omega$$

Where: DR = data rate in Mbit/s

Alternately, the IREF pin can be driven from the SSI 32D4661 in a constant density recording application.

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode, the harmonic phase detector updates the PLL with each occurrence of a DLYD DATA pulse. In the write and idle modes, the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE ($\overline{RG}$) and WRITE GATE ($\overline{WG}$) inputs control the mode of the data/clock recovery section of the chip.

$\overline{RG}$ is an asynchronous input and may be initiated or terminated at any position on the disk. $\overline{WG}$ is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

### READ OPERATION

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, $\overline{RG}$, initiates the PLL locking sequence and selects the PLL reference input; a low level (Read Mode) selects the RD input and a high level selects the external reference clock.

In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of VCO. As depicted in Figure X, $\overline{DRD}$ is a 1/3 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of RD. A decode window is developed from the VCO clock.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS controls.

In the non-read modes, the PLL is locked to the external reference clock. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

### ADDRESS MARK DETECT

In soft sector read operation the circuit must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark consists of two sets of 7 "0" patterns followed by two sets of 11 "0" patterns. To begin the read lock sequence the Address Mark Enable ($\overline{AMENB}$) is asserted low by the controller. The address mark detect ($\overline{AMD}$) circuit then initiates a search of the read data (RD) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0"s within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0"s. If $\overline{AMD}$ does not detect 9 "0"s within 5 RD bits after detecting 6 "0"s it will restart the address mark detect sequence and look for 6 "0"s. When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence, the $\overline{AMD}$ transitions low. $\overline{AMD}$ will remain low for the duration of $\overline{AMENB}$. When $\overline{AMENB}$ is released, $\overline{AMD}$ will be released.

### PREAMBLE SEARCH

After the Address Mark (AM) has been detected, a Read Gate ($\overline{RG}$) can be asserted low, initiating the remainder of the read lock sequence. When $\overline{RG}$ is asserted, an internal counter counts positive transitions of the incoming read data (RD) looking for 3 consecutive "3T" preambles. Once the counter reaches count 3 (finds 3 consecutive 3T preambles) the internal read gate enables, switching the phase detector from the external reference clock to the delayed read data

input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

### VCO LOCK AND BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 positive transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the internal RRC source switches from the external reference clock to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with the data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

### HARD SECTOR OPERATION

In hard sector operation, a high $\overline{AMENB}$ disables the Address Mark Detection circuitry and $\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

### WRITE MODE

In the write mode the circuit converts NRZ data from the controller into 1, 7 RLL formatted data for storage on the disk. The circuit can operate with a soft or hard sector hard drive. An internal flip-flop divides the encoded write data before it is presented at WD/$\overline{WD}$. In a system application, this device requires a Read/Write preamp that does not have an internal flip-flop (such as the SSI 32R2010R).

In soft sector operation the circuit generates a "7, 7, 11, 11" address mark and a preamble pattern ("3T's"). In hard sector operation the circuit generates a 19 x "3T" preamble pattern but no preceding address mark.

WDNRZ data is clocked into the circuit and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The circuit recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin.

The circuit performs write precompensation according to the algorithm outlined in Table 3.

### SOFT SECTOR

In soft sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC source switch from RD and 2VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After delay of 1 NRZ time period (min) from $\overline{RG}$ high, the write gate ($\overline{WG}$) can be enabled low while NRZ is maintained (NRZ write data) low. The address mark enable ($\overline{AMENB}$) is made active (low) a minimum of 1 NRZ time period later. The address mark (consisting of 7 "0"s, 7 "0"s, 11 "0"s, 11 "0"s) and the 19 x "3T" preamble is then written by WD. While the preamble is being written, WCLK is clocking in an all "0" NRZ bit pair. The first non-zero NRZ byte input is assumed to be the sync byte. At the end of the write cycle, 8 WCLK cycles of blank NRZ time passes to insure the encoder is flushed of data; $\overline{WG}$ then goes high. WD stops toggling a maximum of 1 NRZ time periods after $\overline{WG}$ goes high.

### HARD SECTOR

In hard sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC switch references and VCO lock (internal) goes inactive as with soft sector but the $\overline{AMENB}$ (Address Mark Enable) is kept high.

The circuit then sequences from $\overline{RG}$ disable to $\overline{WG}$ enable and NRZ active as in soft sector operation.

## TEST POINTS

The SSI 32D5391 provides two (2) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{\text{DRD}}$, delayed read data – the positive edges represent the data bit position

(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder

The following figure describes the relationship between the various test points:

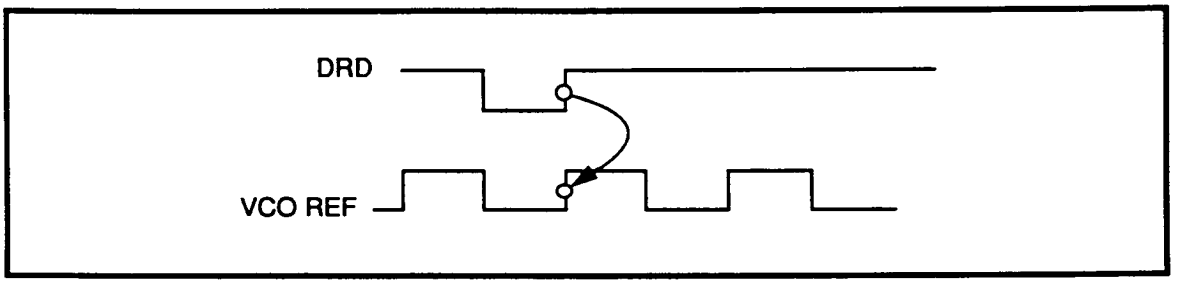



**FIGURE 1: Test Point Relationships**

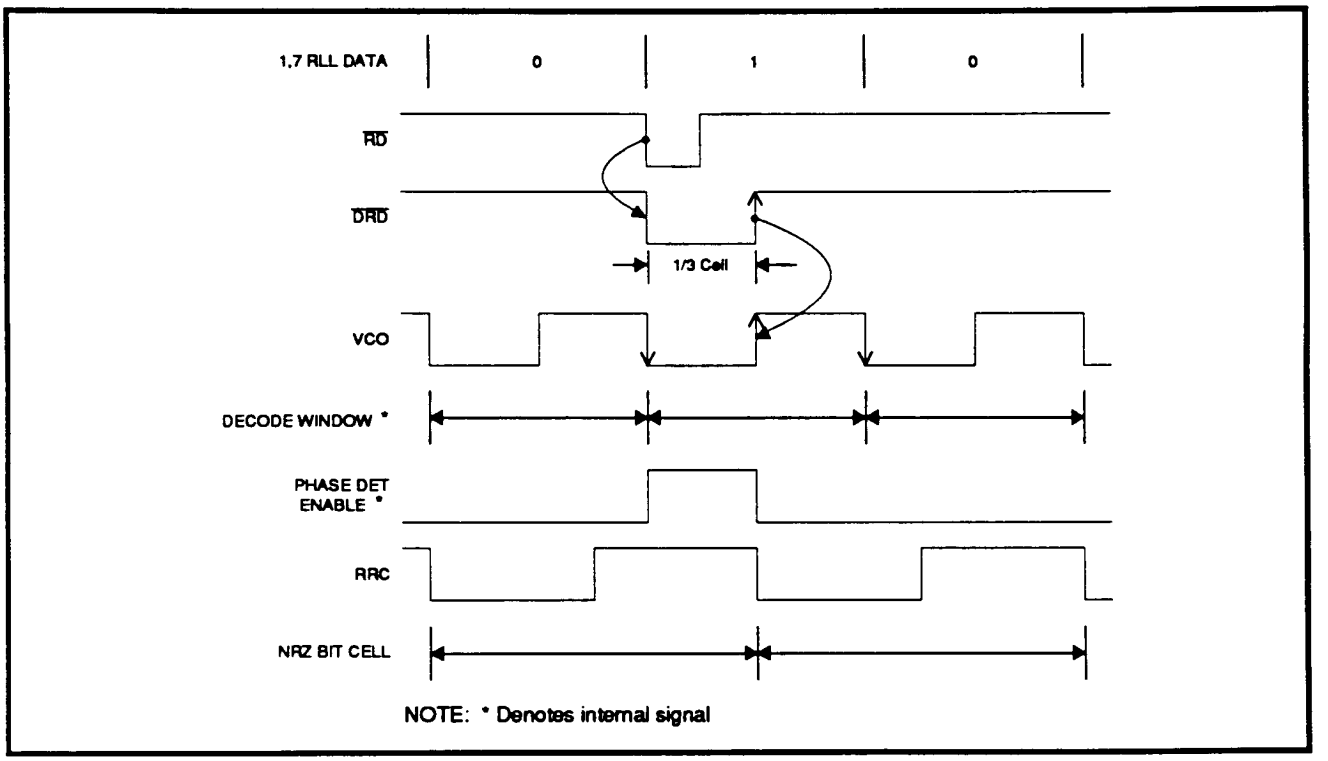



**FIGURE 2: Data Synchronization Waveform**

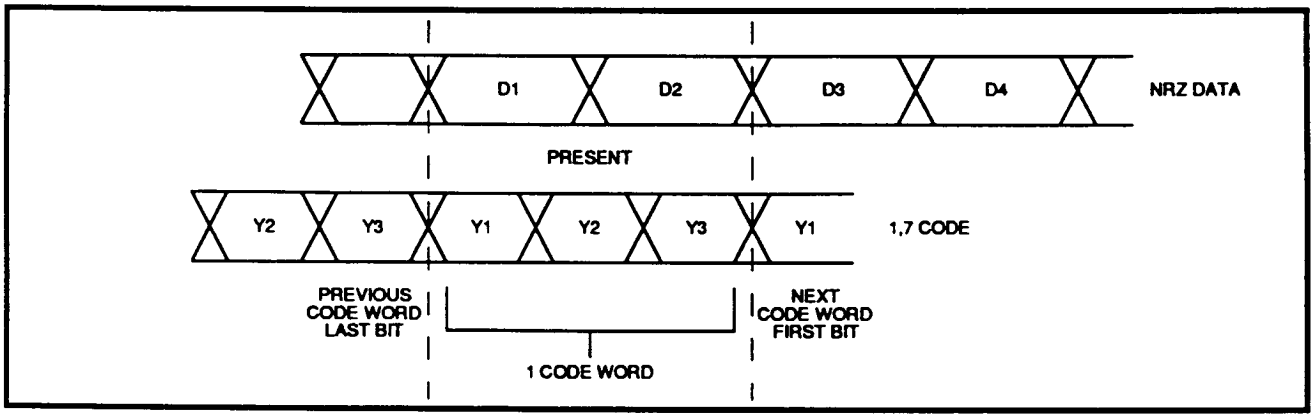



**FIGURE 3: NRZ Data Word Comparision to 1, 7 Code Word (See Tables 1, and 2 for Decode Scheme)**

**TABLE 1: Decode Table for (1, 7) RLL Code Set**

| ENCODED READ DATA | | | DECODED DATA | |
|---|---|---|---|---|
| Previous | Present | Next | | |
| Y Y | Y Y Y | Y Y | D D | |
| 2' 3' | 1 2 3 | 1 2 | 1 2 | |
| 0 0 | 0 0 0 | X X | 0 1 | |
| 1 0 | 0 0 0 | X X | 0 0 | |
| 0 1 | 0 0 0 | X X | 0 1 | |
| X X | 1 0 0 | X X | 1 1 | |
| X 0 | 0 1 0 | 0 0 | 1 1 | |
| X 0 | 0 1 0 | 1 0 | 1 0 | |
| X 0 | 0 1 0 | 0 1 | 1 0 | |
| X 1 | 0 1 0 | 0 0 | 0 1 | |
| X 1 | 0 1 0 | 1 0 | 0 0 | |
| X 1 | 0 1 0 | 0 1 | 0 0 | |
| 0 0 | 0 0 1 | X X | 0 1 | |
| 1 0 | 0 0 1 | X X | 0 0 | |
| 0 1 | 0 0 1 | X X | 0 0 | (Preamble) |
| X X | 1 0 1 | X X | 1 0 | |

**TABLE 2: Encode Table for (1, 7) RLL Code Set**

| NRZ DATA | | | | ENCODED WRITE DATA | | | |
|---|---|---|---|---|---|---|---|
| Present | | Next | | Previous | Present | | |
| D | D | D | D | Y | Y | Y | Y |
| 1 | 2 | 3 | 4 | 3 | 1 | 2 | 3 |
| 0 | 0 | 0 | X | X | 0 | 0 | 1 |
| 0 | 0 | 1 | X | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | X | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | X | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | X | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

NOTE: X = Don't Care

**TABLE 3: Clock Frequency**

| $\overline{WG}$ | $\overline{RG}$ | VCO REF | RRC | DECCLK | ENCCLK | MODE |
|---|---|---|---|---|---|---|
| 1 | 1 | FREF | 2FREF/3 | N/A | N/A | IDLE |
| 1 | 0 | RD | 2VCO/3 | VCO | FREF | READ |
| 0 | 1 | FREF | 2FREF/3 | FREF | FREF | WRITE |
| 0 | 0 | Undefined | Undefined | Undefined | Undefined | Undefined |

Note 1: Until the VCO locks to the new source, the VCO entries will be FREF.

2: Until the VCO locks to the new source, the 2VCO/3 entries will be 2FREF/3.

**TABLE 4: Write Precompensation Algorithm**

| BIT | BIT | BIT | BIT | BIT | COMPENSATION |
|---|---|---|---|---|---|
| n-2 | n-1 | n | n+1 | n+2 | BIT n |
| 1 | 0 | 1 | 0 | 1 | NONE |
| 0 | 0 | 1 | 0 | 0 | NONE |
| 1 | 0 | 1 | 0 | 0 | EARLY |
| 0 | 0 | 1 | 0 | 1 | LATE |

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

**TABLE 5: Write Precompensation Magnitude**

| $\overline{WP1}$ | $\overline{WP0}$ | MAGNITUDE (WP) |
|---|---|---|
| 0 | 0 | 3 |
| 0 | 1 | 2 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The nominal magnitude,
TPC = WP x TPC0 is externally set with a resistor on pin WCS.

**TABLE 6: Window Shift Direction**

| WSD | DIRECTION |
|---|---|
| 0 | Early window (+TS) |
| 1 | Late window (-TS) |

**TABLE 7: Window Shift Magnitude**

| $\overline{W2}$ | $\overline{W1}$ | $\overline{W0}$ | MAGNITUDE (WP) |
|---|---|---|---|
| 1 | 1 | 1 | No shift |
| 1 | 1 | 0 | 4% Minimum shift |
| 1 | 0 | 1 | 8% |
| 1 | 0 | 0 | 12% |
| 0 | 1 | 1 | 15% |
| 0 | 1 | 0 | 18% |
| 0 | 0 | 1 | 20% |
| 0 | 0 | 0 | 22% Maximum shift |
| With resistor, RRS, connected between pins RS and VPA:<br>TS = TS0 [RRS/(RRS + 0.8)]<br>2kΩ < RRS < 16 kΩ | | | |

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA1, VPA2 | I | 5 volt analog power supply pins |
| VPD | I | 5 volt digital power supply pin |
| AGND | - | Analog ground pin |
| DGND | - | Digital ground pin |
| $\overline{\text{AMENB}}$ | I | ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry. Active low TTL input levels. |
| $\overline{\text{DW}}$ | I | DIRECT WRITE ENABLE : Used to enable the direct write mode. A high level allows normal write operation. A low level enables the encoder bypass path mode. In this bypass mode, WDNRZ will directly drive the WD output independent of the state of WG. Pin $\overline{\text{DW}}$ has an internal pull up resistor. TTL input levels. |
| EPD | I | ENABLE PHASE DETECTOR: A low level (coast mode) disables the phase detector and enables the Test Mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on the VCO IN pin. (In the Test Mode, functions normally driven by the VCO are switched to FREF.) Pin EPD has an internal pull-up resistor. TTL input levels. |
| FREF | I | REFERENCE FREQUENCY INPUT: The pin frequency is at one and one-half time the data rate. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. |
| RD, $\overline{\text{RD}}$ | I | READ DATA: Encoded Read Data from the disk drive read channel. Differential +5 volts offset ECL (PECL) input levels. |
| $\overline{\text{RG}}$ | I | READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A low level selects the RD input and enables the read mode/address detect sequences. A high level selects the XTAL input. See Table 2, TTL input levels. |
| $\overline{\text{W0}}$, $\overline{\text{W1}}$, $\overline{\text{W2}}$ | I | WINDOW CONTROL BITS: In Read Mode, pins $\overline{\text{W0}}$ and $\overline{\text{W1}}$ and $\overline{\text{W2}}$ control the magnitude of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels. |
| WCLK | I | WRITE CLOCK: Write mode bit clock. Must be synchronous with the WDNRZ input. For short cable delays, WCLK may be connected directly to pin RRC. For long cable delays, WCLK should be connected to an RRC return line matched to the WDNRZ data bus line delay. TTL input levels. |
| WDNRZ | I | NRZ WRITE DATA INPUT PIN: This pin can be connected to the NRZ to form a bidirectional data port. Pin WDNRZ has an internal pull-up resistor. TTL input levels. |
| $\overline{\text{WP0}}$, $\overline{\text{WP1}}$ | I | WRITE PRECOMPENSATION CONTROL BITS: In Write Mode, pins $\overline{\text{WP0}}$ and $\overline{\text{WP1}}$ control the magnitude of the write precompensation. Each pin has an internal pull-up resistor. TTL input levels. |
| $\overline{\text{WG}}$ | I | WRITE GATE: Enables the write mode. See Table 2. Active low TTL input levels. |
| WSD | I | WINDOW SYMMETRY DIRECTION CONTROL: Controls the direction of the decode window shift. Pin WSD has an internal pull-up resistor. TTL input levels. |

**OUTPUT PINS**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{AMD}$ | O | ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when $\overline{WG}$ is low or $\overline{AMENB}$ is high. When $\overline{AMENB}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMENB}$ resets pin $\overline{AMD}$. TTL output levels. |
| $\overline{DRD}$ | O | DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and VCO_REF outputs can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit jitter. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| FOEN | O | REFERENCE CLOCK ENABLE: When this output is high, the FREF clock is controlling the internal timing. When this output is low, the FREF clock is internally disabled. The output from pin FOEN can be used to disable the clock applied to the FREF pin to reduce VCO jitter during read modes. TTL output levels. |
| NRZ | O | NRZ READ DATA OUTPUT: Tristate output pin that is enabled when read gate is active. This pin can be connected to the WDNRZ pin to form a bidirectional data port. TTL input levels. |
| RRC | O | READ CLOCK: A multiplexed bit clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When $\overline{RG}$ goes low, RRC initially remains synchronized to 2FREF/3. After 19 read data pulses, RRC is synchronized to the Read Data. When $\overline{RG}$ goes high, RRC is synchronized back to the 2FREF/3. TTL output levels. |
| VCO REF | O | VCO REFERENCE: An open emitter ECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to Delayed Read Data. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| WD, $\overline{WD}$ | O | WRITE DATA: Encoded write data output. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to the FREF reference clock. Differential ECL output levels. Termination resistors are required. |
| **ANALOG PINS** | | |
| IREF | I | CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase detector gain are a function of the current sourced into this pin. |
| PD OUT | I/O | PHASE DETECTOR OUTPUT: Drives the loop filter input. |
| RS | I | WINDOW SYMMETRY ADJUST PIN: This pin allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls $\overline{W0}$ and $\overline{W1}$ and $\overline{W2}$ this pin can be used to scale the magnitude of the preset window shift. Connect resistor to VPA. |
| VCO IN | I/O | VCO CONTROL INPUT: Driven by the loop filter output. |
| WCS | I | WRITE PRECOMPENSATION SET: Pin for the reference current to set the write precompensation magnitude value. Connect resistor to VPA. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Supply Voltage, VPA1, VPA2, VPD | -0.3 to 6V |
| Storage Temperature | -65 to 150°C |
| Lead Temperature (Soldering 10 sec.)<br>FOEN,NRZ, WD, WD*, AMD*, DRD*, | 260°C |
| VCOREF pins | -0.3 to (VPA/VPD+0.3),V<br>or +12mA |
| All other pins | -0.3 to (VPA/VPD+0.3)V |

### RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply Voltage, VPA1 = VPA2 = VPD = VCC | 4.75 < VCC < 5.25V |
| Junction Temperature, Tj | 0 < Tj < 135°C |
| Ambient Temperature, Ta | 0 < Ta < 70°°C |

### ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75 < VPA/VPD < 5.25, 0°C < T(ambient) < 70 °C, 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

### POWER SUPPLY CURRENTS AND POWER

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| ICC (VPA, VPD)<br>Supply Current | Outputs and test point pins open, Ta = 70 °C | | 150 | 195 | mA |
| PWR<br>Power Dissipation | Outputs and test point pins open, Ta = 70 °C | | 0.75 | 1.03 | W |

### DIGITAL INPUTS AND OUTPUTS

**TTL Compatible Inputs:** $\overline{\text{AMENB}}$, EPD, WDNRZ, DW, RG, $\overline{\text{W0}}$, $\overline{\text{W1}}$, $\overline{\text{W2}}$, WCLK, WG, $\overline{\text{WP0}}$, $\overline{\text{WP1}}$, FREF Pins

| | | | | | |
|---|---|---|---|---|---|
| Input Low Voltage (VIL) | | -0.3 | | 0.8 | V |
| Input High Voltage (VIH) | | 2.0 | | VPD+0.3 | V |
| Input Low Current | VIL = 0.4 V | 0.0 | | -0.4 | mA |
| Input High Current | VIH = 2.4 V | | | 100 | µA |
| Input Low Current (FREF) | VIL = 0.4 V | 0.0 | | -0.4 | mA |
| Input High Current (FREF) | VIH = 2.4 V | | | 350 | µA |

**ELECTRICAL CHARACTERISTICS (continued)**

**DIGITAL INPUTS AND OUTPUTS (continued)**

**TTL Compatible Outputs:** $\overline{AMD}$, FOEN, NRZ, RRC pins.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Output Low Voltage | Iol = 4.0 mA | | | 0.5 | V |
| Output High Voltage | Ioh= -400µA | 2.4 | | | V |

**Digital Differential Inputs:** RD, $\overline{RD}$ Pins

| | | | | | |
|---|---|---|---|---|---|
| Input Low Voltage (VIL) | | VPA-2.2 | | VIH-0.5 | V |
| Input High Voltage (VIH) | | VIL+0.5 | | VPA-0.5 | V |
| Differential Voltage | $\lvert V_{RD} - \overline{V}_{\overline{RD}} \rvert$ | 0.5 | | | V |
| Input Low Current | VIL = Min | -100 | | | µA |
| Input High Current | VIH = Max | | | +100 | µA |

**Digital Differential Outputs:** WD, $\overline{WD}$ Pins

| | | | | | |
|---|---|---|---|---|---|
| Output Low Voltage | Iol = TBD | VPD-2.1 | | | V |
| Output High Voltage | Ioh = TBD | | | VPD-0.7 | V |
| Differential Voltage | $\lvert V_{WD} - \overline{V}_{\overline{WD}} \rvert$ | 0.5 | | | V |

**Test Point Output Levels**

| | | | | | |
|---|---|---|---|---|---|
| Test Point Output<br>High Level (DRD, VCOREF) | 262Ω to VPA,<br>402Ω to GND, VPA = 5V | | VPA<br>-1.02 | | V |
| Test Point Output<br>Low Level (DRD,VCOREF) | 262Ω to VPA,<br>402Ω to GND, VPA = 5V | | | VPA<br>-1.625 | V |

**DYNAMIC CHARACTERISTICS AND TIMING**

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| Read Data Pulse Width (TPRD) | | 8 | | (2)TVCO<br>-8 | ns |
| Read Data Rise Time (TRRD) | 20% to 80%, CL ≤ 10 pF | | | 5 | ns |
| Read Data Fall Time (TFRD) | 80% to 20%, CL ≤ 10 pF | | | 5 | ns |
| Read Clock Rise Time (TRRC) | 0.8V to 2.0V, CL ≤ 15 pF | | | 10 | ns |
| Read Clock Fall Time (TFRC) | 2.0V to 0.8V, CL ≤ 15 pF | | | 8 | ns |
| NRZ (out) Set Up &<br>Hold Time (TDS, TDH) | | 10 | | | ns |
| RRC duty cycle | except during re-sync | 40 | | 60 | % |
| (TRD) | during re-sync | 40 | | | % |
| $\overline{AMB}$ Set Up &<br>Hold Time (TAS, TAH) | | 10 | | | ns |
| RRC re-sync period (Tdc2) | | TORC | | (2)TORC | ns |
| 1/3 Cell Delay | TD=1.8 (RR + 1.7); RR = kΩ | 0.8TD | | 1.2TD | ns |

**WRITE MODE**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Write Data Pulse Width(TWD) | CL ≤ 15 pF, @1.5V<br>TC=1.8(Rc+0.53) | TFREF<br>-TC-1 | | TFREF | ns |
| Write Data Rise Time (TRWD) | 20% to 80% Points<br>110Ωto VPD, 160Ωto DGND | | | 5 | ns |
| Write Data Fall Time (TFWD) | 80% to 20% Points<br>110Ωto VPD, 160Ωto DGND | | | 5 | ns |
| Write Data Clock Rise Time (TRWC) CL ≤ 15 pF | 0.8V to 2.0V, | | | 10 | ns |
| Write Data Clock Fall Time (TFWC) CL ≤ 15 pF | 2.0V to 0.8V, | | | 8 | ns |
| NRZ Set Up Time (TSNRZ) | | 5 | | | ns |
| NRZ Hold Time (THNRZ) | | 5 | | | ns |
| Precompensation Time Shift Magnitude Accuracy (TPC) | TPCO = 0.22 (Rc + 0.53)<br>Rc min=1 KΩ, Rc max=0.3TXTAL | | | | |
| | $\overline{W0}$ = 1, $\overline{W1}$ =1 | -0.5 | | 0.5 | ns |
| | $\overline{W0}$ = 0, $\overline{W1}$ =1 | | TPCO | | ns |
| | $\overline{W0}$ = 1, $\overline{W1}$ =0 | | 2TPCO | | ns |
| | $\overline{W0}$ = 0, $\overline{W1}$ =0 | | 3TPCO | | ns |

**DATA SYNCHRONIZATION**

| | | | | | |
|---|---|---|---|---|---|
| VCO Center Frequency Period (TVCO) | VCO IN=2.7V, VPA=VPD=5V<br>TO=3.6 (RR+1.7),<br>RR=(185/DR)-1.7K | 0.8TO | | 1.2TO | ns |
| VCO Frequency Dynamic Range | 1.0 V ≤ VCO IN<br>≤ VPA - 0.6V<br>VPA=VPD = 5 V | ± 25 | | ± 45 | % |
| VCO Control Gain (KVCO) | wo = 2π/TO<br>1.0 V ≤ VCO IN<br>≤ VPA - 0.6V | 0.14 wo | | 0.26 wo | rad/s V |
| Phase Detector Gain (KD) | VPA = VPD = 5V<br>Read: KD = 660/(RR+0.53)<br>PLL REF = $\overline{RD}$, 1T Pattern<br>Non-Read: KD = 330/(RR+0.53) | 0.83KD | | 1.17KD | µA/rad |
| KVCO x KD Product Accuracy | | -28 | | +28 | % |
| VCO Phase Restart Error | Referred to RRC | -1 | | +1 | rad |
| Decode Window Centering Accuracy | | | | ±0.75 | ns |
| Decode Window | | TVCO -0.75 | | | ns |

MODE CONTROL

| RG | WG | $\overline{AMENB}$ | MODES | DESCRIPTION |
|---|---|---|---|---|
| 1 | 1 | 1 | Idle | Idle mode. VCO locked to external FREF reference. RRC synchronized to FREF NRZ tri-stated. $\overline{AMD}$ high. |
| 1 | 1 | 0 | AM Search | Read mode Address Mark search. VCO locked to external FREF reference. RRC synchronized to FREF. NRZ tri-stated. $\overline{AMD}$ active. |
| 1 | 0 | 1 | Read Data | Read mode preamble search and data acquisition. VCO switched from FREF to RD after preamble lock.RRC synchronized to RD after 19 "3T" patterns. NRZ active. |
| 1 | 0 | 0 | Undefined | Illegal state. |
| 0 | 1 | 0 | Write AM | Write mode Address Mark insertion. VCO locked to external FREF reference. Byte clock and 4-bit clock synchronized to FREF. WD, $\overline{WD}$ active. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ high. |
| 0 | 1 | 1 | Write Data | Write mode preamble insertion and data write. VCO locked to external FREF reference. RRC synchronized to FREF. WD, $\overline{WD}$ active. NRZ0 tri-stated. $\overline{AMD}$ high. |
| 0 | 0 | 1 | Undefined | Illegal state. |
| 0 | 0 | 0 | Undefined | Illegal state. |

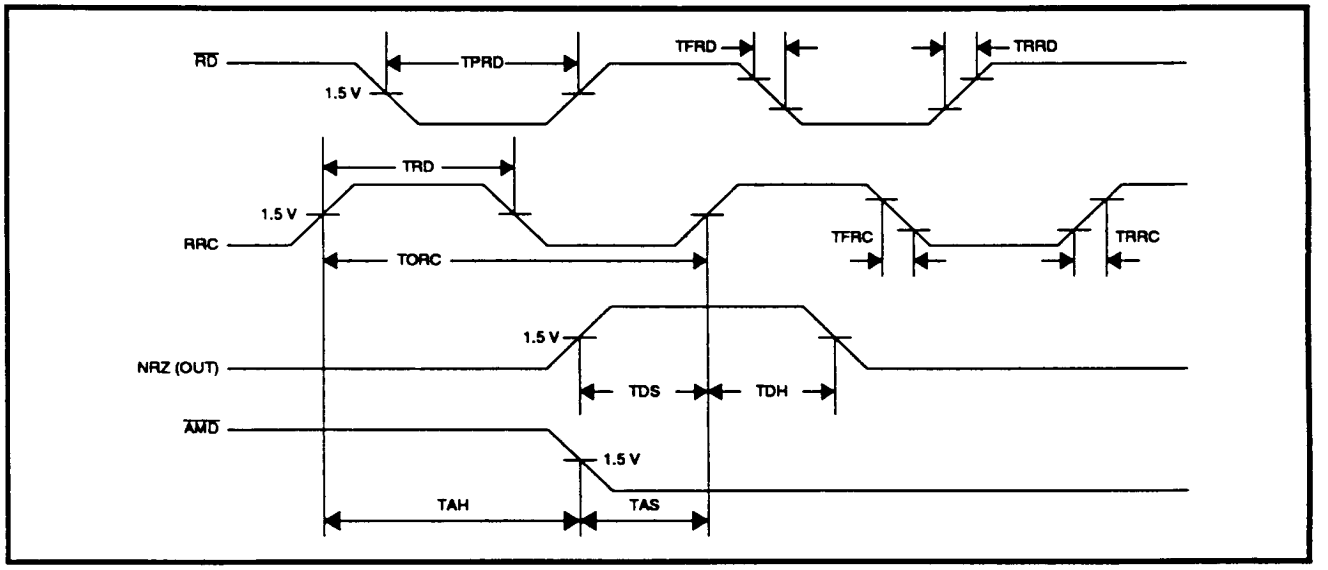



**FIGURE 3: Read Timing**

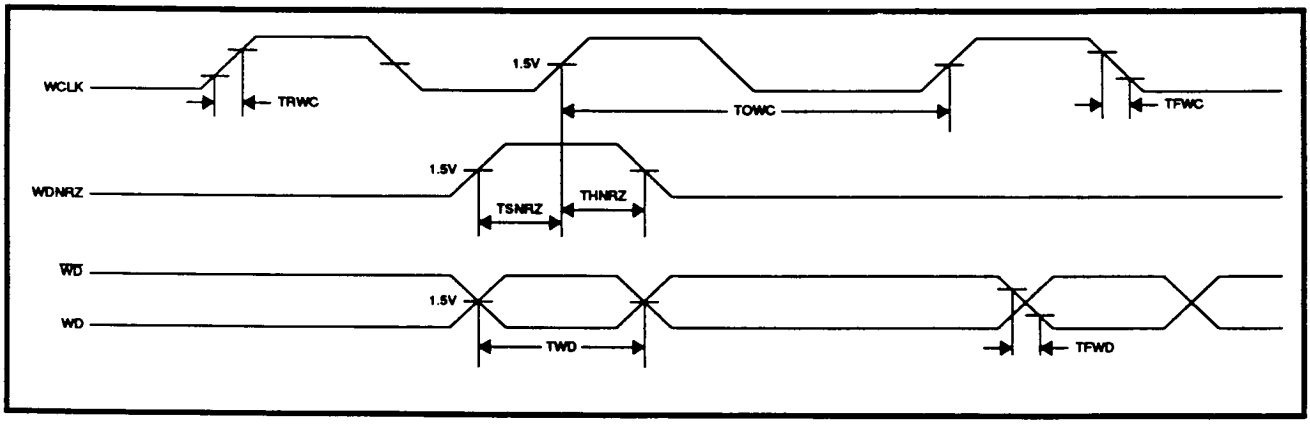



**FIGURE 4: Write Timing**

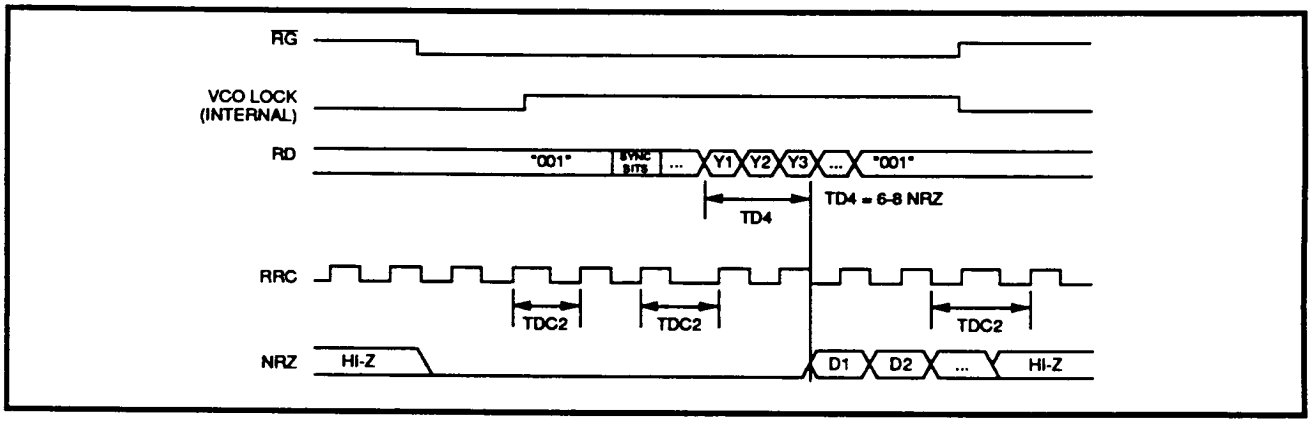



**FIGURE 5: Read Mode NRZ Data Timing**

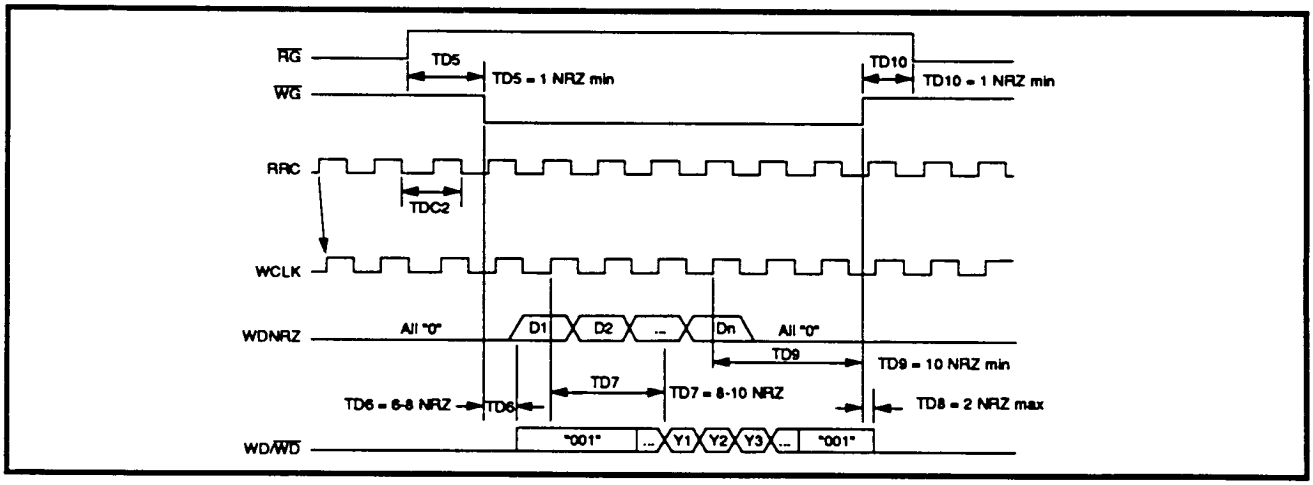



**FIGURE 6: Write Mode NRZ Data Timing**

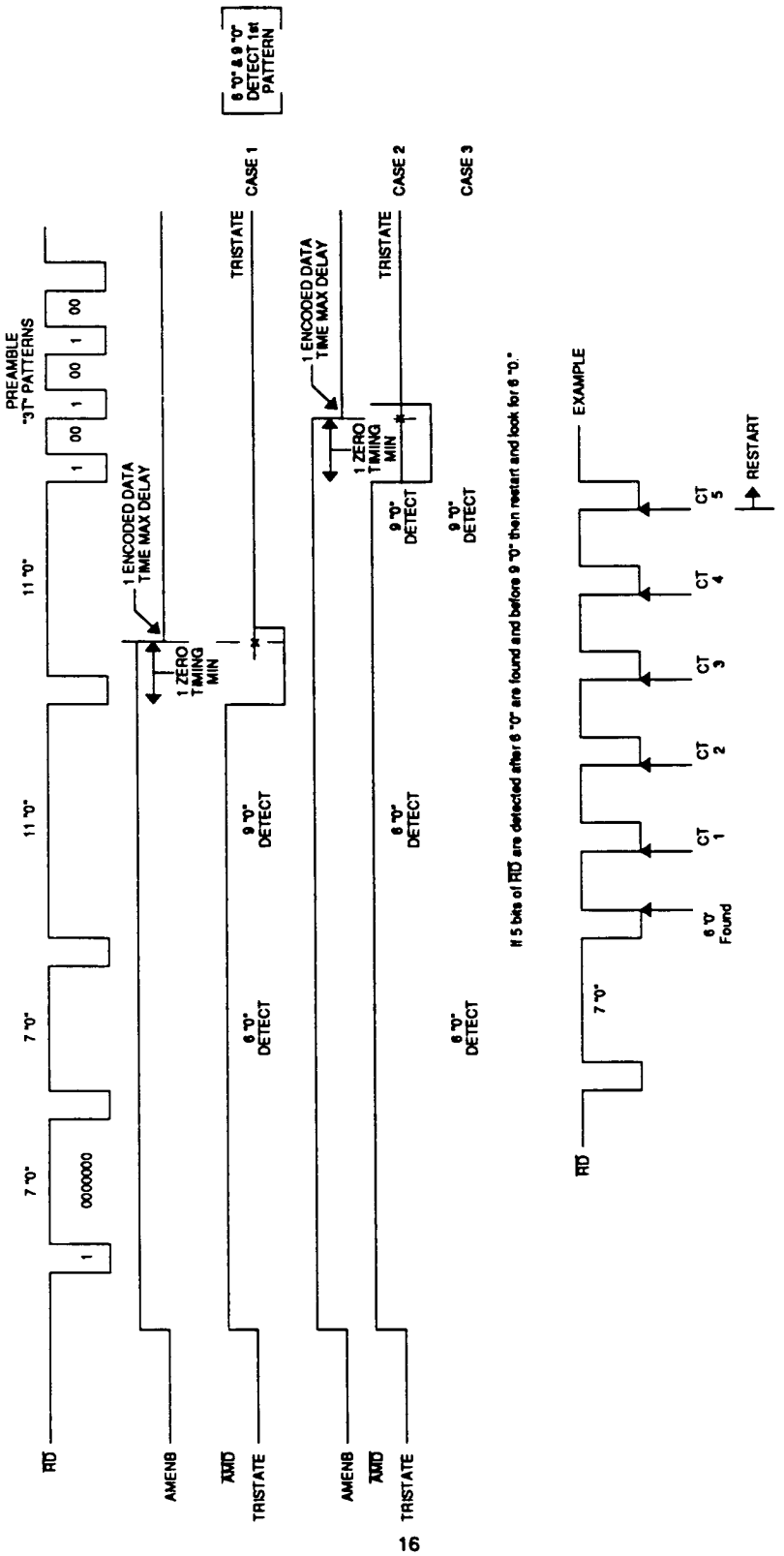



**FIGURE 6: Address Mark Search**

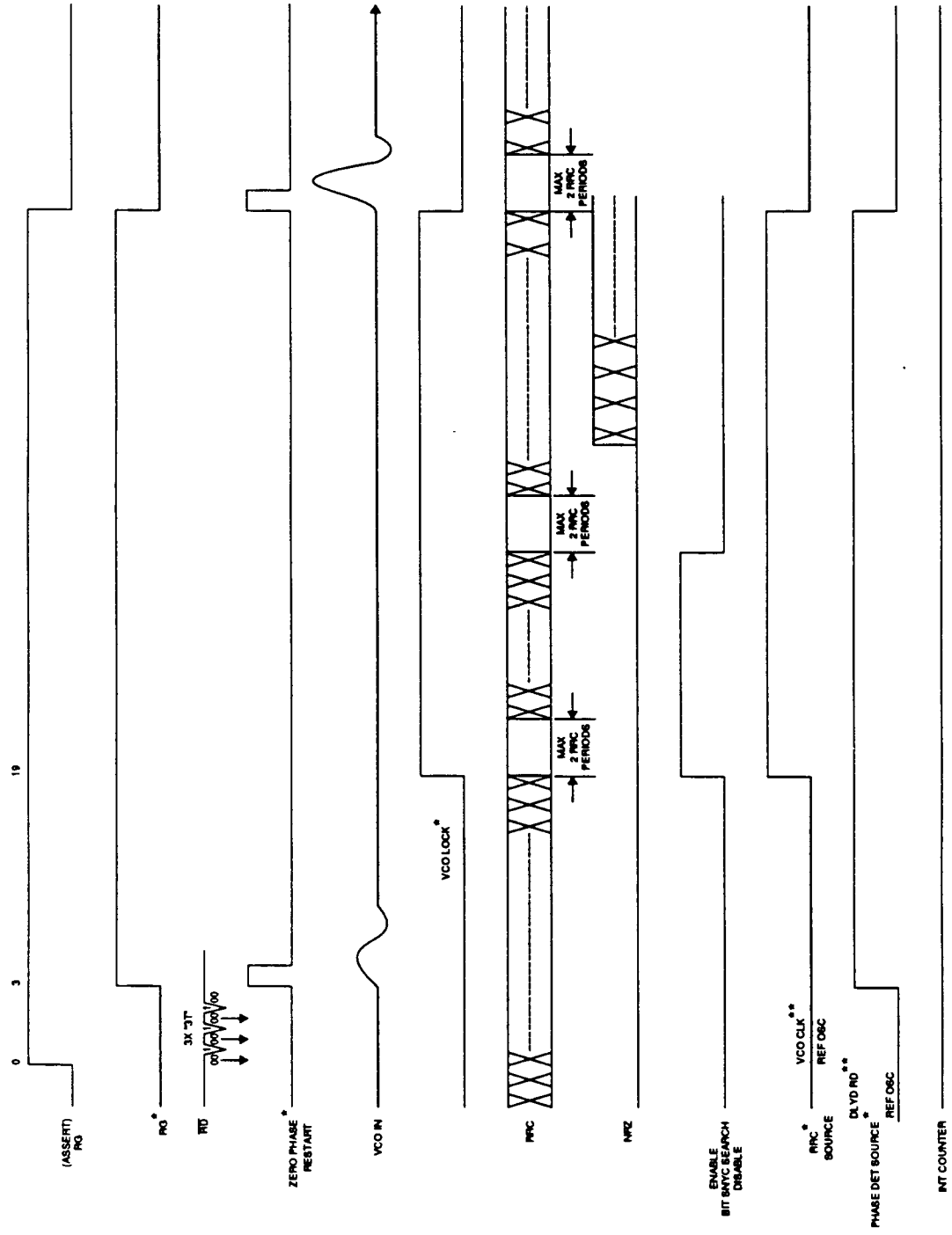



FIGURE 7: Read Mode Locking Sequence (Soft and Hard Sector)

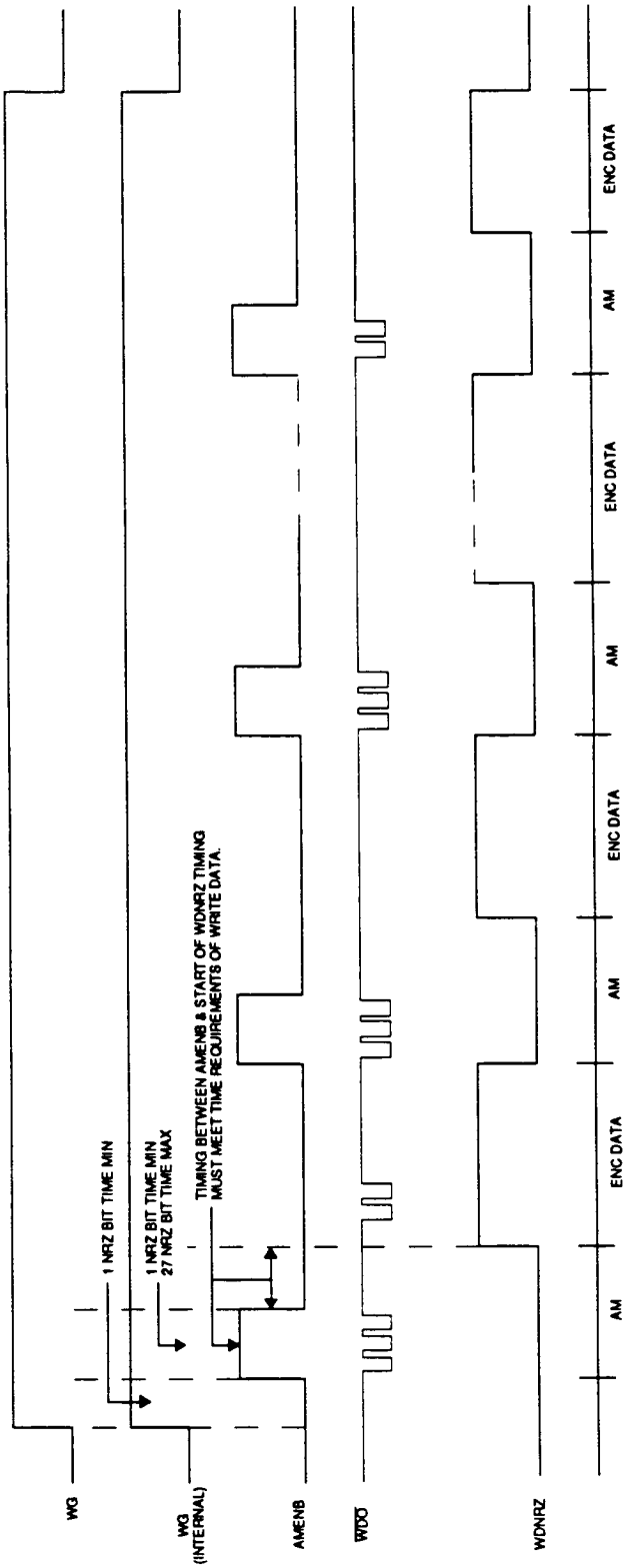



**FIGURE 8: Multiple Address Mark Write**

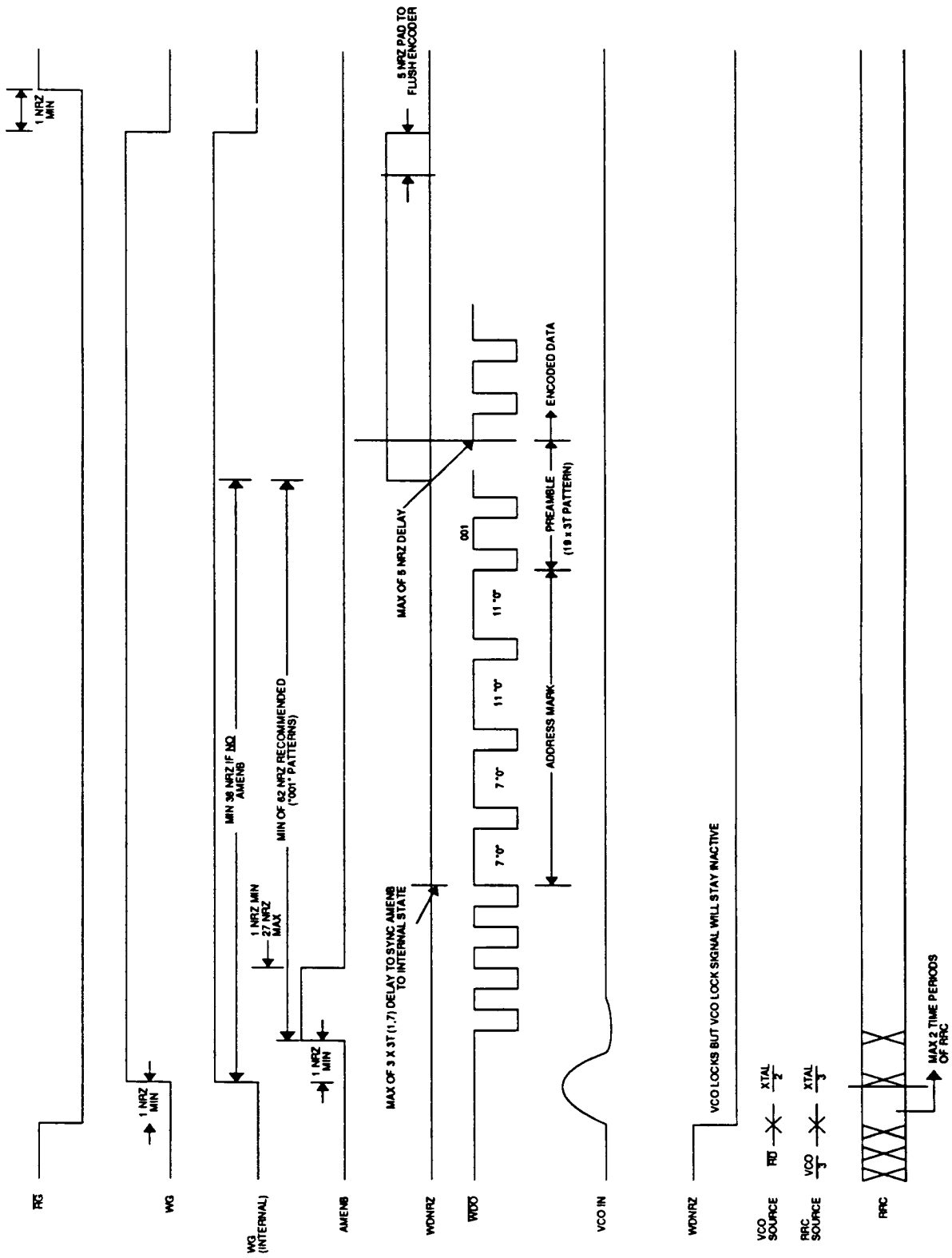
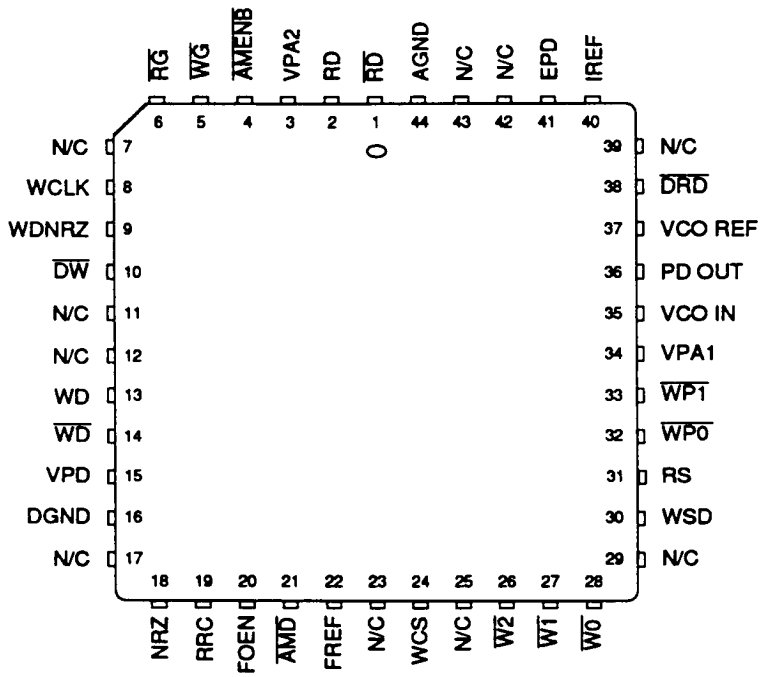



FIGURE 9: Write Data

# SSI 32D5391
# Data Sync/1, 7 RLL ENDEC
# with Write Precomp. and Window Shift

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**44-Lead PLCC**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32D5391 | | |
| 44-Lead PLCC | 32D5391-CH | 32D5391-CH |



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0693 - rev.