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256K x 32 SRAM MODULE

PUMA 68S8000X - 12/15/17/20

Issue 1.5 : December 1998

Description

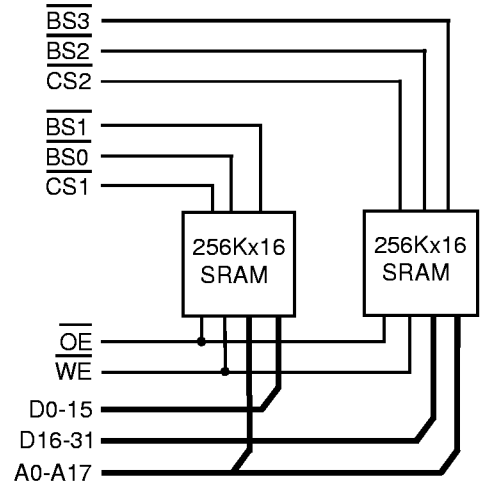
The PUMA 68S8000X is a 8Mbit CMOS High Speed Static RAM organised as 256K x 32 in a JEDEC 68 pin surface mount PLCC, available with access times of 12, 15, 17 or 20ns. The output width is user configurable as 16 or 32 bits using two Chip Selects ($\overline{CS1}$~2). 8-bit accessability is achieved using four byte select pins ($\overline{BS0}$~3)

The device features low power standby, multiple ground pins for maximum noise immunity and TTL compatible inputs and outputs. The PUMA 68S8000X offers a dramatic space saving advantage over two standard 256Kx16 devices. The PUMA 68S8000X is an pin compatible upgrade path from the PUMA 68S2000X.

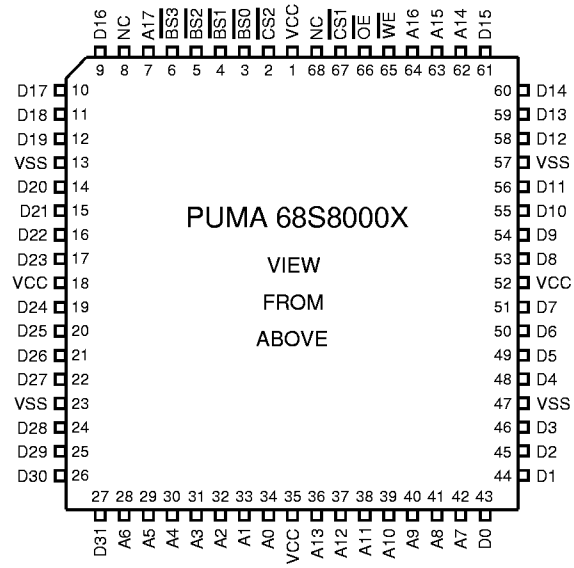
Features

- Very Fast Access Times of 12/15/17/20 ns.
- JEDEC 68 'J' leaded plastic Surface Mount Substrate.
- Upgradeable.
- User Configurable as 16 / 32 bit wide output.
- Operating Power : 2.86 W (Max)
  Standby Power (TTL) : 660 mW (Max)
  (CMOS) : 110 mW (Max)
- Individual byte enables provide byte accessibility.
- Fully Static operation.
- Multiple ground pins for maximum noise immunity.
- Single 5V±10% Power supply.

Block Diagram



Pin Definition



Pin Functions

Address Inputs	**A0 - A17**
Data Input/Output	**D0 - D31**
Chip Select	**$\overline{CS1}$~2**
Byte Select	**$\overline{BS0}$~3**
Write Enable	**$\overline{WE}$**
Output Enable	**$\overline{OE}$**
No Connect	**NC**
Power (+5V)	**V_{cc}**
Ground	**GND**

Package Details

Plastic 68 J-Leaded JEDEC PLCC

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Voltage on any pin relative to V_{SS}	V_T (2)	-0.3	-	7.0	V
Power Dissipation	P_T	-	-	2.0	W
Storage Temperature	T_{STG}	-55	-	125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -2.0V pulse of less than 10ns.

Recommended Operating Conditions

Parameter		*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
Input High Voltage		V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}	-0.3	-	0.8	V
Operating Temperature	(Commercial)	T_A	0	-	70	°C
	(Industrial)	T_{AI}	-40	-	85	°C

DC Electrical Characteristics (V_{CC}=5V±10%) T_A 0 to 70 °C

Parameter		*Symbol*	*Test Condition*	*Min*	*Typ*	*max*	*Unit*
I/P Leakage Current	Address,$\overline{OE}$,$\overline{WE}$	I_{LI}	0V ≤ V_{IN} ≤ V_{CC}	-4	-	4	µA
Output Leakage Current		I_{LO}	$\overline{CS1\sim2}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	-4	-	4	µA
Operating Supply Current	32-bit mode	I_{CC1}	Min. Cycle, $\overline{CS1\sim2}$=V_{IL}, V_{IL}≤V_{IN}≤V_{CC}-2.1V, $\overline{BS0\sim3}$=V_{IL}	-	-	520	mA
	16-bit mode	I_{CC2}	Min. Cycle, $\overline{BS0\sim3}$=V_{IL}, V_{IL}≤V_{IN}≤V_{CC}-2.1V, $\overline{CS1}$=V_{IL} or $\overline{CS2}$=V_{IL}.	-	-	310	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS1\sim2}$ = V_{IH}	-	-	120	mA
	CMOS levels	I_{SB2}	$\overline{CS1\sim2}$ ≥ V_{CC}-0.2V, 0.2≤V_{IN}≤V_{CC}-0.2V	-	-	20	mA
Output Voltage		V_{OL}	I_{OL} = 8.0mA	-	-	0.4	V
		V_{OH}	I_{OH} = -4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

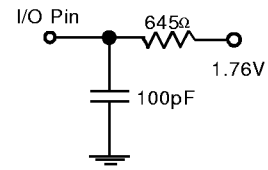
Capacitance (V_{CC}=5V±10%,T_A=25°C) Note: Capacitance calculated, not measured.

Parameter		*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance	(Address,$\overline{OE}$,$\overline{WE}$)	C_{IN1}	V_{IN} = 0V	20	pF
I/P Capacitance	(other)	C_{IN2}	V_{IN} = 0V	10	pF
I/O Capacitance	(16-bit Mode - worst case)	$C_{I/O}$	$V_{I/O}$ = 0V	24	pF

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 3ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%

Output Load



Operation Truth Table

$\overline{CS1}$	$\overline{CS2}$	$\overline{BS0}$	$\overline{BS1}$	$\overline{BS2}$	$\overline{BS3}$	$\overline{OE}$	$\overline{WE}$	SUPPLY CURRENT	MODE
L	L	L	H	H	H	X	L	I_{CC1}	Write $D_{0\sim7}$
L	L	H	L	H	H	X	L	I_{CC1}	Write $D_{8\sim15}$
L	L	H	H	L	H	X	L	I_{CC1}	Write $D_{16\sim23}$
L	L	H	H	H	L	X	L	I_{CC1}	Write $D_{24\sim31}$
L	L	L	L	H	H	X	L	I_{CC1}	Write $D_{0\sim15}$
L	L	H	H	L	L	X	L	I_{CC1}	Write $D_{16\sim31}$
L	L	L	L	L	L	X	L	I_{CC1}	Write $D_{0\sim31}$
L	L	H	H	H	H	X	L	I_{CC1}	$D_{0\sim31}$ High-Z
L	L	L	H	H	H	L	H	I_{CC1}	Read $D_{0\sim7}$
L	L	H	L	H	H	L	H	I_{CC1}	Read $D_{8\sim15}$
L	L	H	H	L	H	L	H	I_{CC1}	Read $D_{16\sim23}$
L	L	H	H	H	L	L	H	I_{CC1}	Read $D_{24\sim31}$
L	L	L	L	H	H	L	H	I_{CC1}	Read $D_{0\sim15}$
L	L	H	H	L	L	L	H	I_{CC1}	Read $D_{16\sim31}$
L	L	L	L	L	L	L	H	I_{CC1}	Read $D_{0\sim31}$
L	L	X	X	X	X	H	H	I_{CC1}	$D_{0\sim31}$ High-Z
L	H	L	L	X	X	X	L	I_{CC2}	Write $D_{0\sim15}$, $D_{16\sim31}$ Standby
L	H	L	H	X	X	X	L	I_{CC2}	Write $D_{0\sim7}$, $D_{16\sim31}$ Standby
L	H	H	L	X	X	X	L	I_{CC2}	Write $D_{8\sim15}$, $D_{16\sim31}$ Standby
L	H	H	H	X	X	X	L	I_{CC2}	$D_{0\sim15}$ High-Z, $D_{16\sim31}$ Standby
L	H	X	X	X	X	H	H	I_{CC2}	$D_{0\sim15}$ High-Z, $D_{16\sim31}$ Standby
H	L	X	X	L	L	X	L	I_{CC2}	$D_{0\sim15}$ Standby,Write $D_{16\sim31}$
H	L	X	X	L	H	X	L	I_{CC2}	$D_{0\sim15}$ Standby,Write $D_{16\sim23}$
H	L	X	X	H	L	X	L	I_{CC2}	$D_{0\sim15}$ Standby,Write $D_{24\sim31}$
H	L	X	X	H	H	X	L	I_{CC2}	$D_{0\sim15}$ Standby,$D_{16\sim31}$ High-Z
H	L	X	X	X	X	H	H	I_{CC2}	$D_{0\sim15}$ Standby,$D_{16\sim31}$ High-Z
H	H	X	X	X	X	X	X	I_{SB1}, I_{SB2}	$D_{0\sim31}$ Standby

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}

AC OPERATING CONDITIONS

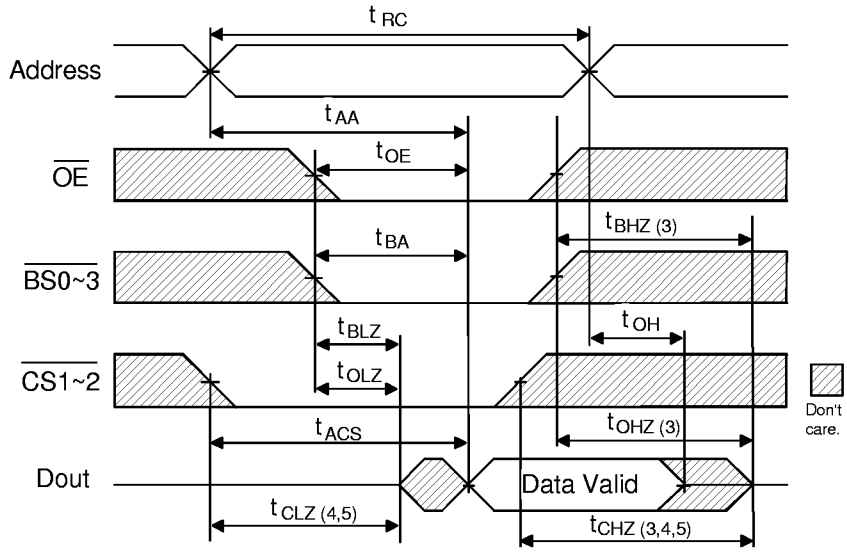
Read Cycle

		-12		-15		-17		-20		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	12	-	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	17	-	20	ns
Chip Select Access Time	t_{ACS}	-	12	-	15	-	17	-	20	ns
Byte Select Access Time	t_{BA}	-	6	-	7	-	8	-	10	ns
Output Enable to Output Valid	t_{OE}	-	6	-	7	-	8	-	10	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	3	-	ns
Byte Selection to Output in Low Z	t_{BLZ}	0	-	0	-	0	-	0	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	6	0	7	0	8	0	9	ns
Output Disable to Output in High Z	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Byte Deselection to Output in High Z	t_{BHZ}	0	6	0	7	0	8	0	9	ns

Write Cycle

		-12		-15		-17		-20		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Write Cycle Time	t_{WC}	12	-	15	-	17	-	20	-	ns
Chip Selection to End of Write	t_{CW}	8	-	10	-	12	-	15	-	ns
Byte Selection to End of Write	t_{BW}	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	12	-	15	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width ($\overline{OE}$ high)	t_{WP1}	8	-	10	-	12	-	15	-	ns
Write Pulse Width ($\overline{OE}$ low)	t_{WP2}	12	-	12	-	13	-	15	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	8	-	10	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output active from end of write	t_{OW}	3	-	3	-	3	-	3	-	ns

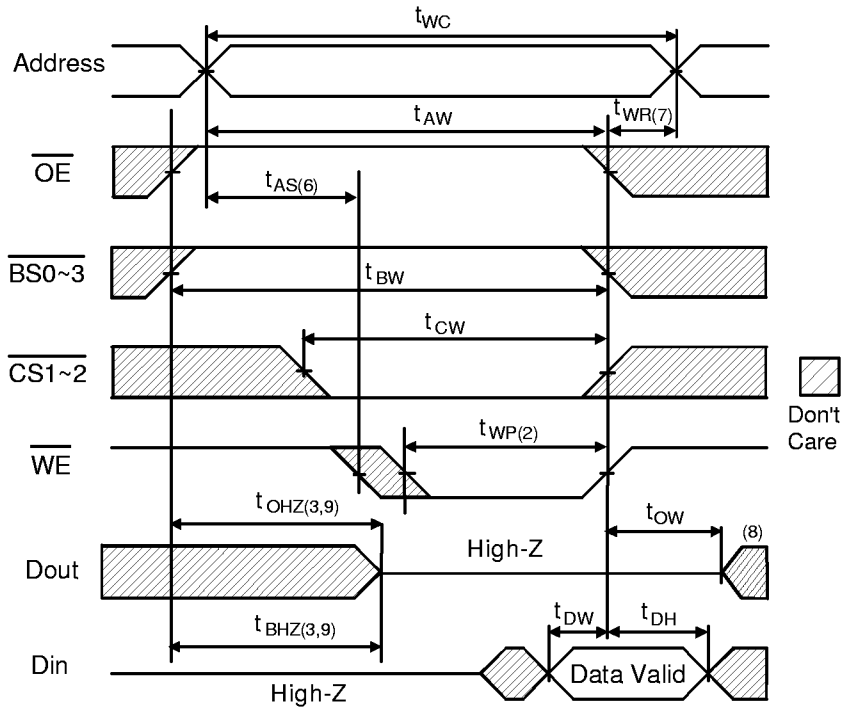
Read Cycle Timing Waveform (1,2)



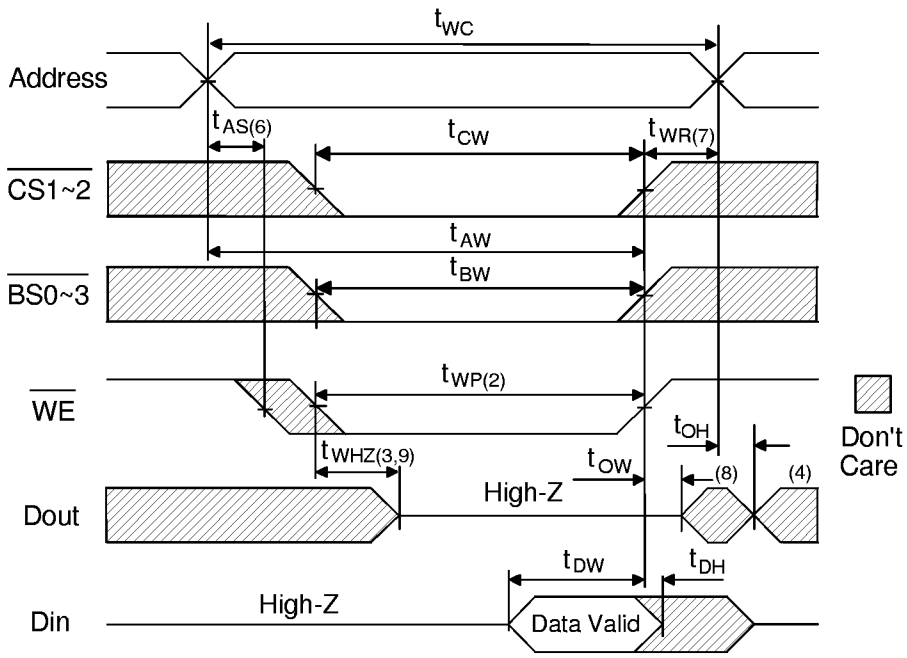
AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.
(2) All read cycle timing is referenced from the last valid address to the first transition address.
(3) t_{CHZ}, t_{BHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.
(4) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.
(5) These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform (1,4)



Write Cycle No.2 Timing Waveform [1,5]



AC Write Characteristics Notes

(1) All write cycle timing is referenced from the last valid address to the first transition address.

(2) All writes occur during the overlap of $\overline{CS1\sim2}$, $\overline{BS0\sim3}$ and $\overline{WE}$ low.

(3) If $\overline{OE}$, $\overline{CS1\sim2}$, $\overline{BS0\sim3}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.

(4) Dout is the Read data of the new address.

(5) $\overline{OE}$ is continuously low.

(6) Address is valid prior to or coincident with $\overline{CS1\sim2}$, $\overline{BS0\sim3}$ and $\overline{WE}$ low, too avoid inadvertant writes.

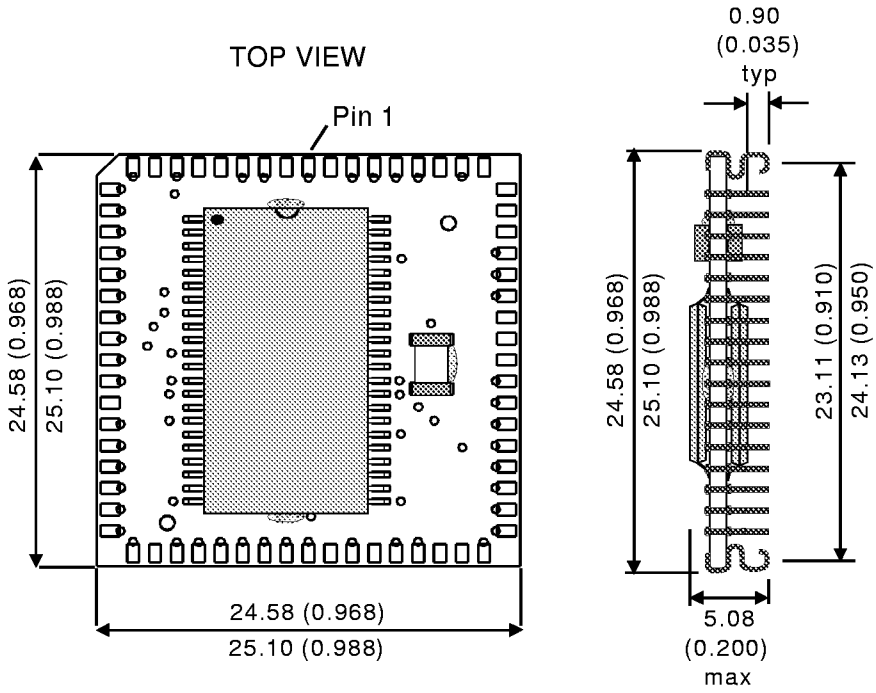
(7) $\overline{CS1\sim2}$, $\overline{BS0\sim3}$ or $\overline{WE}$ must be high during address transitions.

(8) When $\overline{CS1\sim2}$ and $\overline{BS0\sim3}$ are low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.

(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Package Information Dimensions in mm(inches)

Plastic 68 Pin JEDEC Surface mount PLCC



Ordering Information

PUMA 68S8000XLI - 12

Speed	12	=	12 ns
	15	=	15 ns
	17	=	17 ns
	20	=	20 ns
Temp. range/screening	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
Power Consumption	Blank	=	Standard
Pinout Configuration	X	=	Industry Standard
Memory Organisation	S8000	=	SRAM configurable as 256Kx32 or 512Kx16.
Package	PUMA 68	=	68 pin "J" Leaded PLCC

Soldering Recommendations.

Bake.

As specified on product packaging.

If not specified HMP Ltd. recommend a minimum bake of 6 hours duration @ 125°C, if parts have been exposed to the atmosphere for 24 hours or more.

Soldering.

Must not exceed,

VPR 215 - 219°C, 60 secs.

IR / Convection

Ramp Rate 6°C/sec max.
Temp maintained at 125°C,120 secs max.
Temp exceeding 183°C, 120 - 180 secs.
Time at max. temp. 10 - 40 secs.
Max temp. 220 +5/-0°C
Ramp down -6°C/sec max.