hmp limited
Elm Road, West Chirton, NORTH SHIELDS, Tyne & Wear
NE29 8SE, England Tel.+44 (0191) 2930500 Fax.+44 (0191) 2590997

128K x 32 SRAM MODULE

PUMA 68S4000/A - 020/025/35/45

Issue 4.4 : December 1999

Description

The PUMA68S4000/A is a 4Mbit CMOS High Speed Static RAM organised as 128K x 32 in a JEDEC 68 pin surface mount PLCC, available with access times of 20, 25, 35, and 45ns. The output width is user configurable as 8 , 16 or 32 bits using four Chip Selects ($\overline{CS1}$~4).

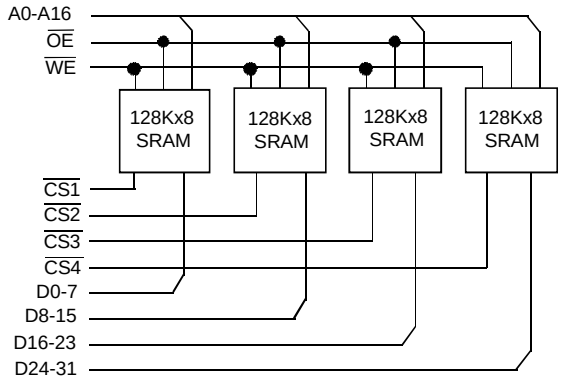
The device features multiple ground pins for maximum noise immunity and TTL compatible inputs and outputs. The PUMA 68S4000/A offers a dramatic space saving advantage over four standard 128Kx8 devices.

Features

- Fast Access Times of 20 ,25, 35 and 45 ns.
- JEDEC 68 'J' leaded plastic surface mount Substrate
- Industrial or Military Grade.
- Upgradeable footprint.
- User Configurable as 8 / 16 / 32 bit wide output.
- Operating Power (32-BIT) 4.00 W (Max)
  Low Power Standby (TTL) 1.43 W (Max)
  -L Version (CMOS) 44 mW (Max)
- Fully Static operation.
- Multiple ground pins for maximum noise immunity.
- Single 5V±10% Power supply.

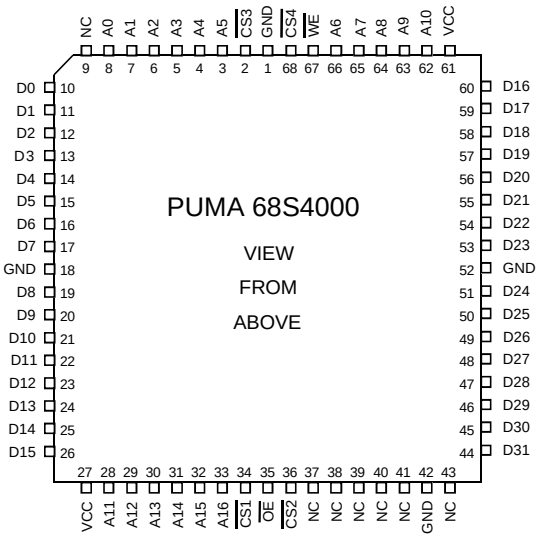
Block Diagram

(PUMA 68 S4000A page 2)



Pin Definition

(PUMA 68 S4000A page 2)



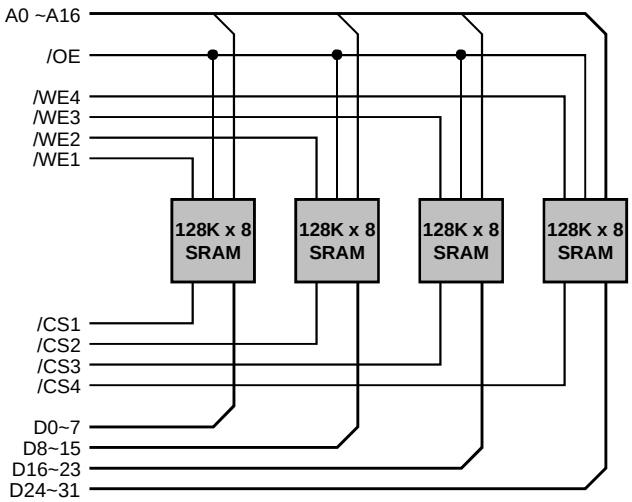
Pin Functions

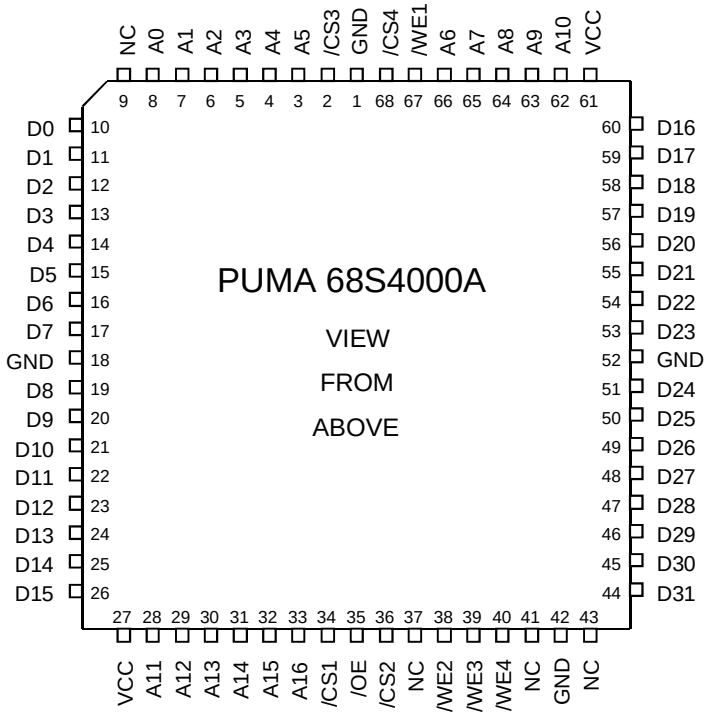
Address Inputs	**A0 - A16**
Data Input/Output	**D0 - D31**
Chip Select	**$\overline{CS1}$~4**
Write Enable	**$\overline{WE1}$~4**
Output Enable	**$\overline{OE}$**
No Connect	**NC**
Power (+5V)	**V_{cc}**
Ground	**GND**

Package Details

Plastic 68 J-Leaded JEDEC PLCC

PUMA 68 S4000A Pinout and Block Diagram.





DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Voltage on any pin relative to V_{SS}	V_T (2)	-0.5	-	7.0	V
Power Dissipation	P_T	-	-	4.0	W
Storage Temperature	T_{STG}	-65	-	150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.0V pulse of less than 10ns.

Recommended Operating Conditions

Parameter		*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
Input High Voltage		V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}	-0.3	-	0.8	V
Operating Temperature	(Commercial)	T_A	0	-	70	°C
	(Industrial)	T_{AI}	-40	-	85	°C (Suffix I)
	(Military)	T_{AM}	-55	-	125	°C (Suffix M)

DC Electrical Characteristics (V_{CC}=5V±10%, T_A = -55°C to +125°C)

Parameter		*Symbol*	*Test Condition*	*Min*	*Typ*	*max*	*Unit*
Input Leakage Current		I_{LI1}	V_{IN}=0V to V_{CC}	-20	-	20	µA
Output Leakage Current		I_{LO}	$V_{I/O}$=0V to V_{CC}	-40	-	40	µA
Operating Supply Current(2)	32 bit	I_{CC32}	$\overline{CS}$(1)=V_{IL}, $I_{I/O}$=0mA, f=f_{max}	-	-	840	mA
	16 bit	I_{CC16}	As above.	-	-	540	mA
	8 bit	I_{CC8}	As above.	-	-	400	mA
Standby Supply Current	(TTL)	I_{SB}	$\overline{CS}$(1)=V_{IH}, f=f_{max}, V_{IN}=V_{IL} or V_{IH}	-	-	260	mA
-L Version	(CMOS)	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V,f=0	-	-	8	mA
Output Voltage Low	V_{OL}	I_{OL} = 8.0mA,V_{CC}=Min		-	-	0.4	V
Output Voltage High	V_{OH}	I_{OH} = -4.0mA,V_{CC}=Min		2.4	-	-	V

Notes: (1) $\overline{CS1}$~4 inputs operate simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

(2) At f=f_{max} address and data inputs are cycling at max frequency.

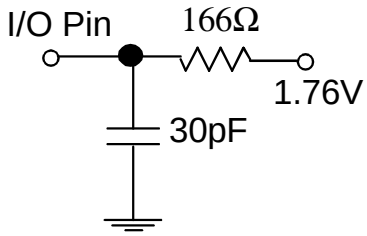
Capacitance (V_{CC}=5V±10%,T_A=25°C) Note: Capacitance calculated, not measured.

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Capacitance Address,$\overline{OE}$,$\overline{WE}$	C_{IN1}	V_{IN}=0V	-	-	34	pF
Output Capacitance 8-bit mode (worst case)	$C_{I/O}$	$V_{I/O}$=0V	-	-	42	pF

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 3ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%

Output Load



Operation Truth Table

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	$\overline{OE}$	$\overline{WE}$	*SUPPLY CURRENT*	*MODE*
L	H	H	H	X	L	I_{CC8}	Write $D_{0~7}$
H	L	H	H	X	L	I_{CC8}	Write $D_{8~15}$
H	H	L	H	X	L	I_{CC8}	Write $D_{16~23}$
H	H	H	L	X	L	I_{CC8}	Write $D_{24~31}$
L	L	H	H	X	L	I_{CC16}	Write $D_{0~15}$
H	H	L	L	X	L	I_{CC16}	Write $D_{16~31}$
L	L	L	L	X	L	I_{CC32}	Write $D_{0~31}$
L	H	H	H	L	H	I_{CC8}	Read $D_{0~7}$
H	L	H	H	L	H	I_{CC8}	Read $D_{8~15}$
H	H	L	H	L	H	I_{CC8}	Read $D_{16~23}$
H	H	H	L	L	H	I_{CC8}	Read $D_{24~31}$
L	L	H	H	L	H	I_{CC16}	Read $D_{0~15}$
H	H	L	L	L	H	I_{CC16}	Read $D_{16~31}$
L	L	L	L	L	H	I_{CC32}	Read $D_{0~31}$
X	X	X	X	H	H	$I_{CC32}/I_{CC16}/I_{CC8}$	$D_{0~31}$ High-Z
H	H	H	H	X	X	I_{SB},I_{SB1}	$D_{0~31}$ Standby

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}

Low Vcc Data Retention Characteristics - L version only

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$=V_{CC}-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR1} (1)	V_{CC} = 2.0V, $\overline{CS}$ > V_{CC}-0.2V, V_{IN} >0V	-	-	2.2	mA
Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}	-	-	ns

AC OPERATING CONDITIONS

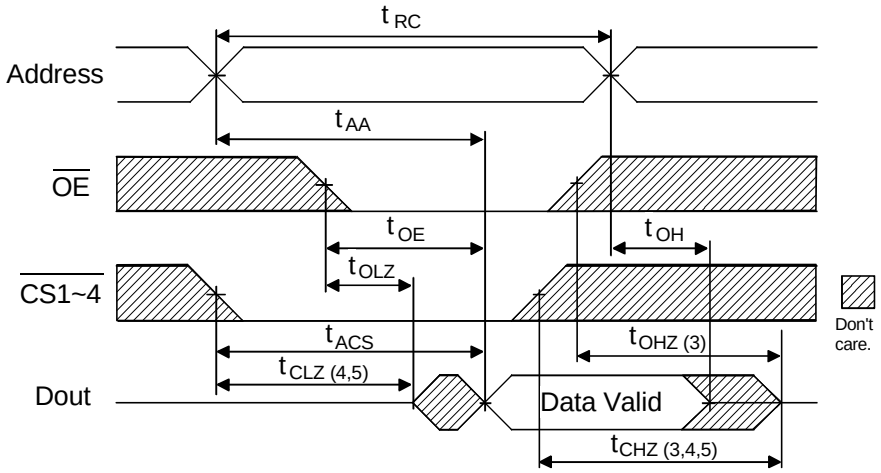
Read Cycle

		-020		-025		-35		-45		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	20	-	25	-	35	-	45	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	-	45	ns
Chip Select Access Time	t_{ACS}	-	20	-	25	-	35	-	45	ns
Output Enable to Output Valid	t_{OE}	-	10	-	12	-	15	-	17	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Deselection to O/P in High Z	t_{CHZ}	0	9	0	10	0	12	0	15	ns
Output Disable to Output in High Z	t_{OHZ}	0	8	0	10	0	12	0	15	ns

Write Cycle

		-020		-025		-35		-45		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Write Cycle Time	t_{WC}	20	-	25	-	35	-	45	-	ns
Chip Selection to End of Write	t_{CW}	15	-	20	-	25	-	35	-	ns
Address Valid to End of Write	t_{AW}	15	-	20	-	25	-	35	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	12	-	15	-	17	-	20	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	10	0	12	0	15	0	15	ns
Data to Write Time Overlap	t_{DW}	10	-	12	-	15	-	15	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output active from end of write	t_{OW}	3	-	3	-	3	-	3	-	ns

Read Cycle Timing Waveform (1,2)



AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

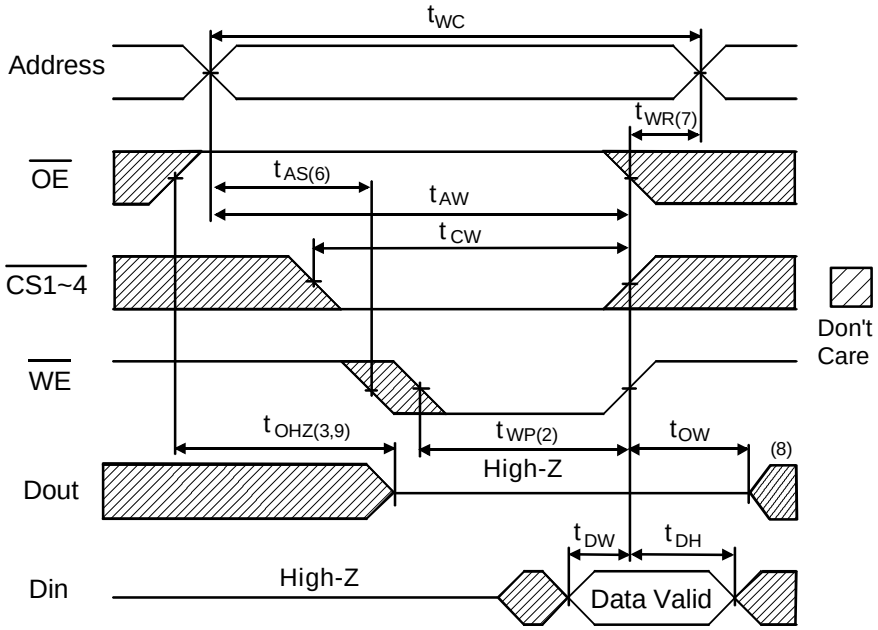
(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

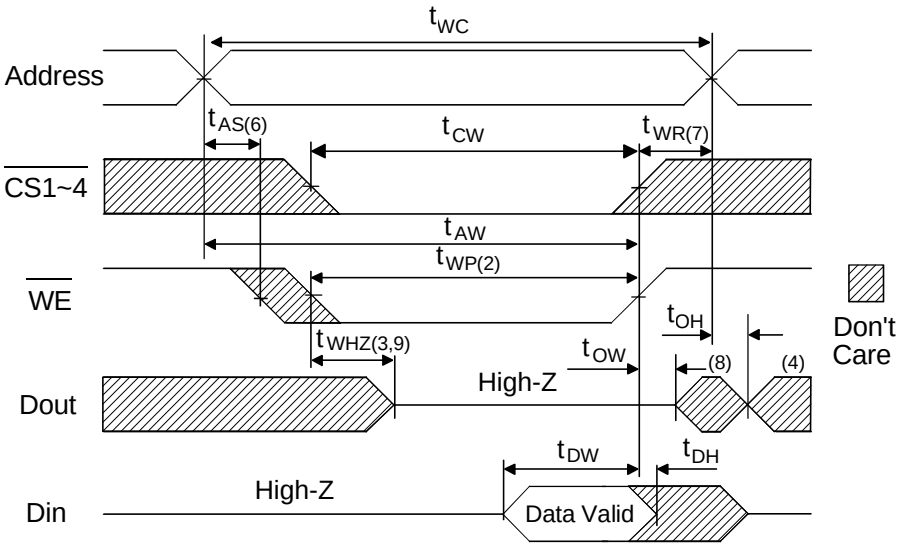
(4) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform (1,4)



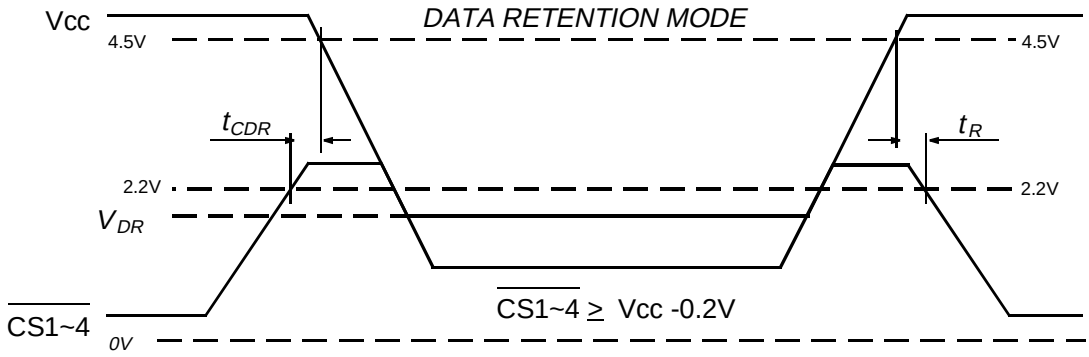
Write Cycle No.2 Timing Waveform (1,5)



AC Write Characteristics Notes

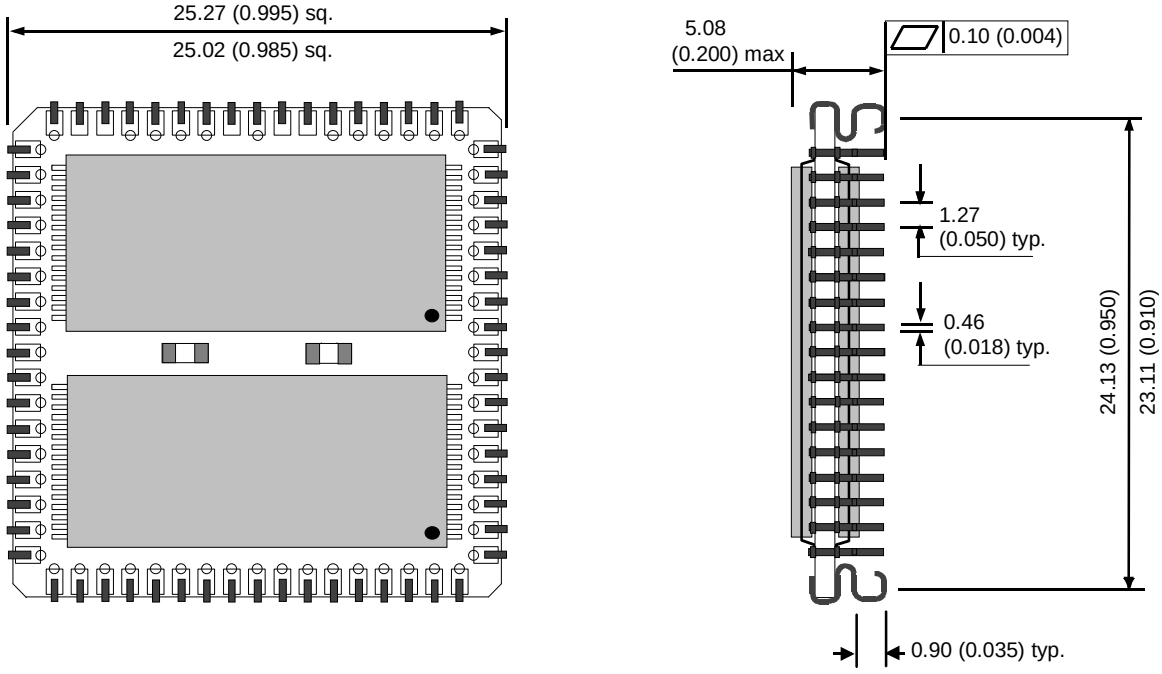
(1) All write cycle timing is referenced from the last valid address to the first transition address.
(2) All writes occur during the overlap of $\overline{CS1\sim4}$ and $\overline{WE}$ low.
(3) If $\overline{OE}$, $\overline{CS1\sim4}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.
(4) Dout is the Read data of the new address.
(5) $\overline{OE}$ is continuously low.
(6) Address is valid prior to or coincident with $\overline{CS1\sim4}$ and $\overline{WE}$ low, too avoid inadvertant writes.
(7) $\overline{CS1\sim4}$ or $\overline{WE}$ must be high during address transitions.
(8) When $\overline{CS1\sim4}$ are low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.
(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Data Retetnion Waveform



Package Information Dimensions in mm(inches)

Plastic 68 Pin JEDEC Surface mount PLCC



Ordering Information

PUMA 68S4000/AM - 020

Speed	020	=	20ns
	025	=	25ns
	35	=	35ns
	45	=	45ns
Temperature range	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
	M	=	Military Temperature
/WE Option	Blank	=	Single/WE
	A	=	/WE1~4
Memory Organisation	S4000	=	128K x 32 SRAM configurable as 256K x 16 and 512K x 8
Package	PUMA 68	=	68 pin "J" Leaded PLCC

Note :
Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantibility or fitness for aparticular purpose.
Our products are subject to a constant process of development. Data may be changed without notice.
Products are not authorised for use as critical components in life support devices without the express written approval of a company director.

Co Planarity

Specified as +/- 2 thou max.

Visual Inspection Standard

All devices inspected to ANSI/J-STD-001B Class 2 standard

Moisture Sensitivity

Devices are **moisture sensitive.**

Shelf Life in Sealed Bag 12 months at <40^{O}C and <90% relative humidity (RH).

After this bag has been opened, devices that will be subjected to infrared reflow, vapour phase reflow, or equivalent processing (peak package body temp 220^{O}C) **must be** :

A : Mounted within 72 Hours at factory conditions of <30^{O}C/60% RH

OR

B : Stored at <20% RH

If these conditions are not met or indicator card is >20% when read at 23^{O}C +/-5% devices **require baking** as specified below.

If baking is required, devices may be baked for :-

A : 24 hours at 125^{O}C +/-5% for high temperature device containers

OR

B : 192 hours at 40^{O}C +5^{O}C/-0^{O}C and <5% RH for low temperature device containers**.**

Packaging Standard

Devices packaged in dry nitrogen, JED-STD-020.

Packaged in trays as standard.

Tape and reel available for shipment quantities exceeding 200pcs upon request.

Soldering Recomendations

IR/Convection -	Ramp Rate	6^{O}C/sec max.
	Temp. exceeding 183^{O}C	150 secs. max.
	Peak Temperature	225^{O}C
	Time within 5^{O}C of peak	20 secs max.
	Ramp down	6^{O}C/sec max.
Vapour Phase -	Ramp up rate	6^{O}C/sec max.
	Peak Temperature	215 - 219^{O}C
	Time within 5^{O}C of peak	60 secs max.
	Ramp down	6^{O}C/sec max.

The above conditions must not be exceeded.

Note : The above recommendations are based on standard industry practice. Failure to comply with the above recommendations invalidates product warranty.