mosaic

Mosaic Semiconductor Inc

128Kx 32 EEPROM MODULE

PUMA 2E4000X-15/20/25

Issue 1.1 : September1993

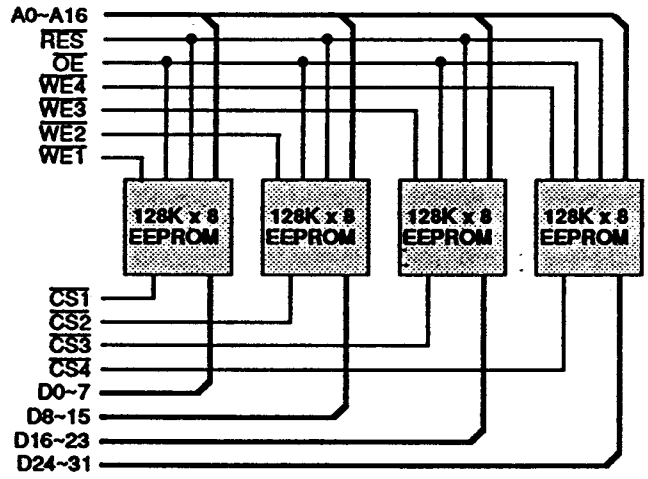
ADVANCE PRODUCT INFORMATION

4,194,304 bit MNOS High Speed EEPROM

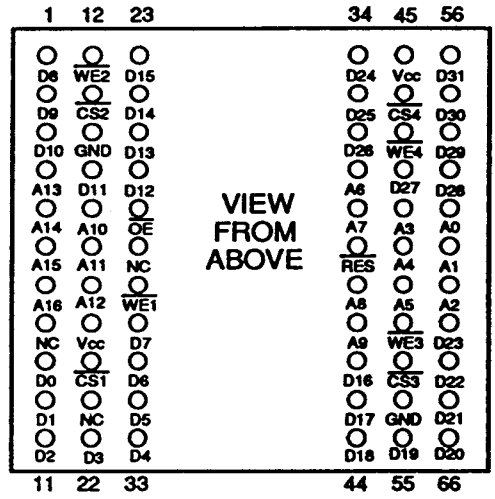
Features

Fast Access Time of 150/200/250 ns.
66 PGA Ceramic Substrate suitable for thermal ladders.
User Configurable as: 8 / 16 / 32 bit wide output.
Operating Power @ 1MHz: 160 / 253 / 440 mW (max).
Low Power Standby 11 mW (max).
Single Byte and Page Write (128 Bytes) operation.
Software Data Protection.
$\overline{DATA}$ Polling Indication of End of Write.
10^4 Write/Erase Cycles in Page Mode.
10 Year Data Retention Time.

Block Diagram



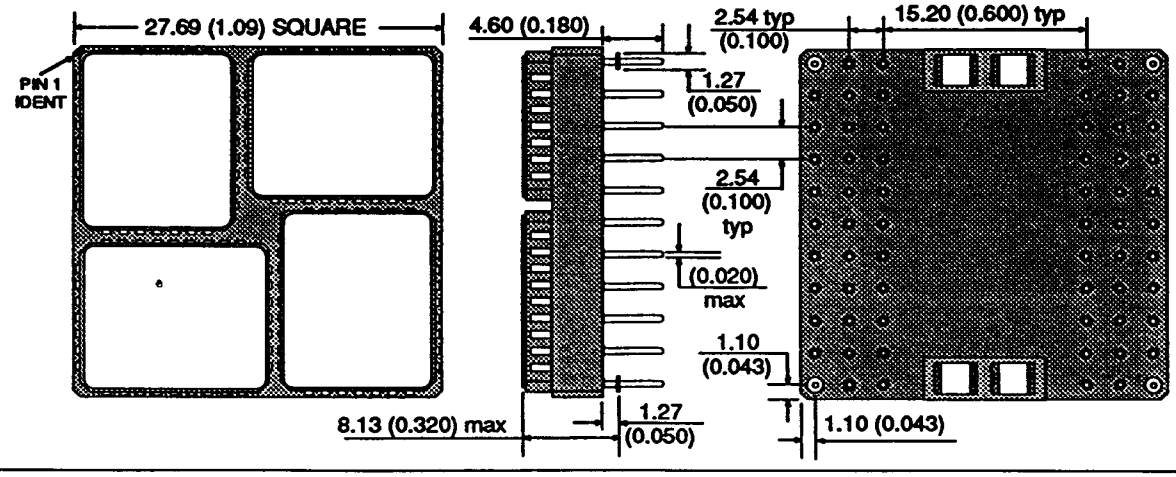
Pin Definition



Pin Functions

A0~16	Address Inputs
D0~31	Data Inputs/Outputs
$\overline{CS1}$~4	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE1}$~4	Write Enable
$\overline{RES}$	Reset
V_{cc}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches). All dimensions maximum unless otherwise stated.



Absolute Maximum Ratings (1)

Operating Temperature	T_{OPR}	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Input voltages (including N.C. pins) with Respect to GND (2)	V_{IN}	-0.5 to +7.0	V
Supply Voltage with respect to GND	V_{CC}	-0.6 to +7.0	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) May be -3.0V for pulse width of less than 50 ns.

Recommended Operating Conditions

		min	*typ*	*max*	
DC Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Input High Voltage	V_{IH}(1)	2.2	-	V_{CC}+0.3	V
Operating Temp Range	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I Suffix)
	T_{AM}	-55	-	125	°C (M, MB Suffix)

Note: (1) Except $\overline{RES}$ pin.

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter		*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current	$\overline{CS1\text{-}4}$, $\overline{WE1\text{-}4}$	I_{LI1}	V_{IN} = GND to V_{CC}	-2	2	µA
	$\overline{RES}$	I_{LI2}	V_{IN} = GND to V_{CC}	-	100	µA
	Other Inputs	I_{LI3}	V_{IN} = GND to V_{CC}	-8	8	µA
Output Leakage Current	32 bit	I_{LO}	V_{IN} = GND to V_{CC}, $\overline{CS}$(1)=V_{IH}	-2	2	µA
Operating Supply Current	32 bit	I_{CC32}	$\overline{CS}$(1)=$\overline{OE}$=V_{IL}, $\overline{WE}$(1)=V_{IH}, I_{OUT}=0mA, f=5MHz(2)	-	200	mA
	16 bit	I_{CC16}	As above	-	106	mA
	8 bit	I_{CC8}	As above	-	59	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}$(1) = V_{IH}, I_{IO} = 0mA, Other Inputs = V_{IH}	-	12	mA
	CMOS levels	I_{SB2}	$\overline{CS}$(1) = V_{CC}-0.3V, I_{IO} = 0mA, Other Inputs = V_{CC}	-	2	mA
Output Low Voltage		V_{OL}	I_{OL} = 2.1mA.	-	0.4	V
Output High Voltage		V_{OH}	I_{OH} = -400µA.	2.4	-	V

Notes (1) $\overline{CS}$ and $\overline{WE}$ above are accessed through $\overline{CS1\text{-}4}$ and $\overline{WE1\text{-}4}$ respectively. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) At an operating frequency of 1MHz, the 32 /16 / 8 bit currents will be 80 / 46 / 29 mA (max) respectively.

Capacitance (T_A=25°C, f=1MHz) Note: These parameters are calculated, not measured.

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	$\overline{CS1\text{-}4}$, $\overline{WE1\text{-}4}$	C_{IN1}	V_{IN}=0V	-	16	pF
	Other Inputs	C_{IN2}	V_{IN}=0V	-	34	pF
Output Capacitance	32 bit	C_{OUT32}	V_{OUT}=0V	-	22	pF

AC READ CHARACTERISTICS

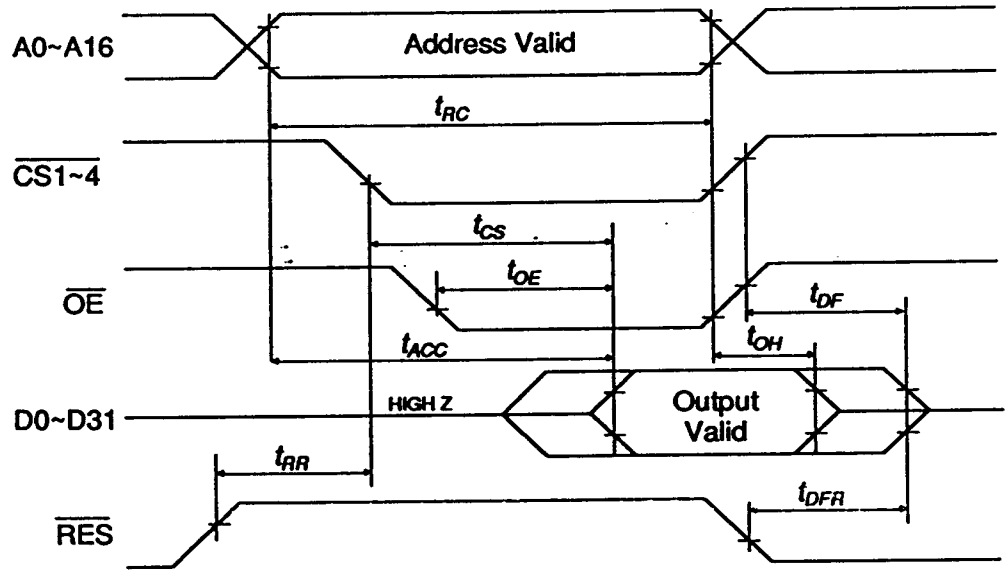
Read Cycle

Parameter	Symbol	-15 min	-15 max	-20 min	-20 max	-25 min	-25 max	Unit
Address to Output Delay	t_{ACC}	-	150	-	200	-	250	ns
Chip Select to Output Delay	t_{CS}	-	150	-	200	-	250	ns
Output Enable to Output Delay	t_{OE}	10	75	10	80	10	90	ns
Address to Output Hold	t_{OH}	0	-		-	0	-	ns
Output Enable to Output Float	t_{DF} (1)	0	50	0	55	0	60	ns
	t_{DFR} (2)	0	350	0	350	0	350	ns
Reset to Output Delay	t_{RR} (2)	0	600	0	600	0	600	ns

Notes: (1) t_{DF} is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. This parameter is guaranteed and not 100% tested.

(2) These parameters are not tested but guaranteed by design.

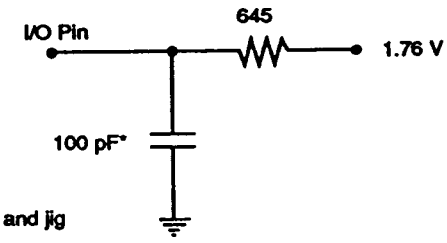
Read Cycle Timing Waveform



AC Test Conditions

* Input pulse levels: 0.0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* V_{cc}=5V±10%
* Module tested in 32 bit mode.

Output Load



* Including scope and jig

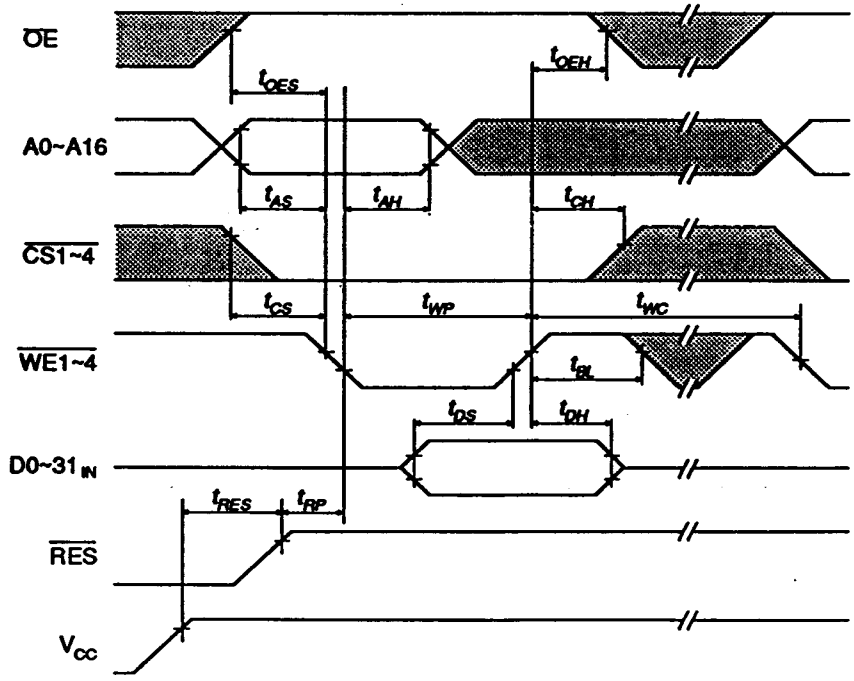
AC WRITE CHARACTERISTICS - BYTE AND PAGE

Write Cycle

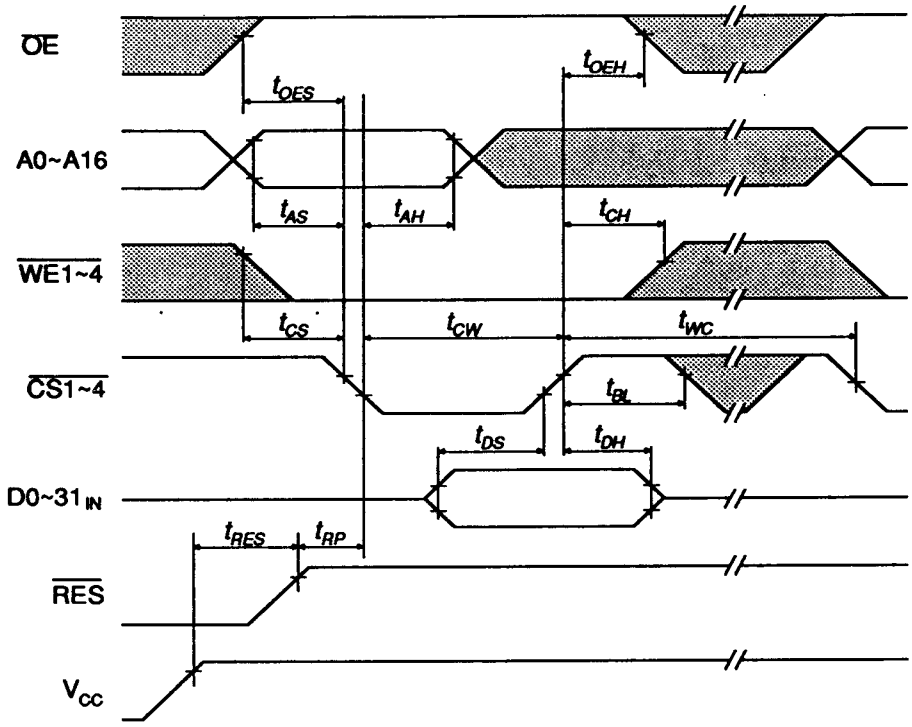
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Address Set-up Time	t_{AS}	0	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Write Pulse Width	t_{WP}	250	-	-	ns
	t_{CW}	250	-	-	ns
Address Hold Time	t_{AH}	150	-	-	ns
Data Set-up Time	t_{DS}	100	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Output Enable Set-up Time	t_{OES}	0	-	-	ns
Output Enable Hold Time	t_{OEH}	0	-	-	ns
Data Latch Time	t_{DL}	300	-	-	ns
Write Cycle Time	t_{WC}	-	-	15(1)	ms
Byte Load Window	t_{BL}	100	-	-	µs
Byte Load Cycle	t_{BLC}	0.55	-	30	µs
Reset to Write Set-up Time	t_{RP}	100	-	-	µs
V_{CC} to Reset Set-up Time	t_{RES} (1)	1	-	-	µs

Notes: (1) This parameter is not tested but guaranteed by design.
(2) Normal writing is not possible when the $\overline{RES}$ terminal becomes low during writing. The $\overline{RES}$ terminal should not be made low for at least 10ms after the last writing pulse is input.
(3) Use this device in longer cycle than this value.

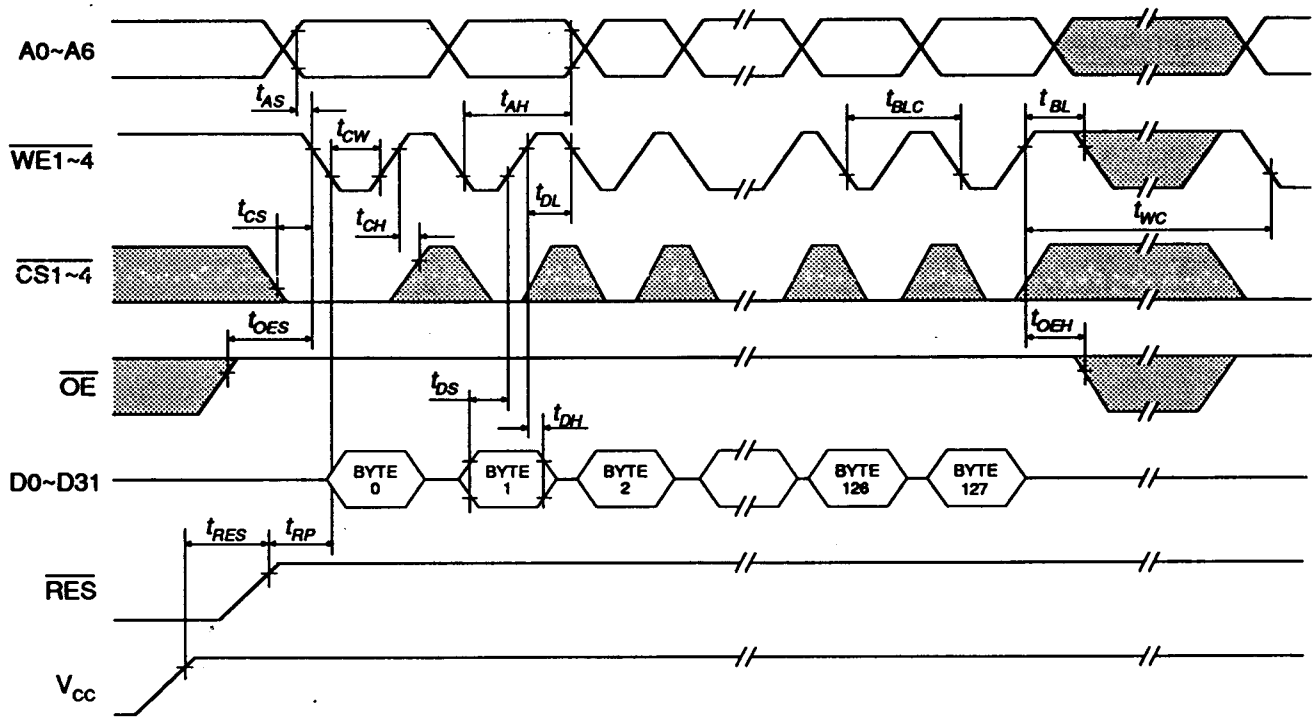
AC Write Waveform - $\overline{WE}$ Controlled



AC Write Waveform - $\overline{CS}$ Controlled

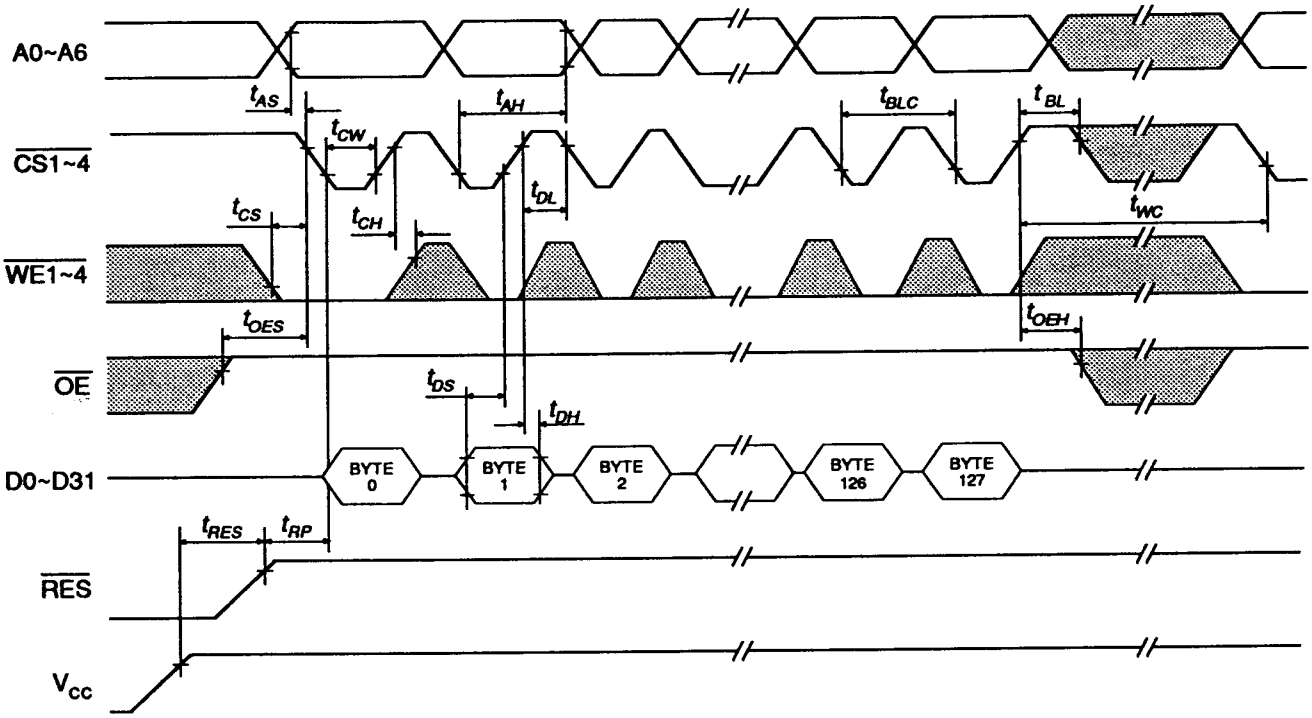


Page Mode Write Waveform - $\overline{WE}$ Controlled



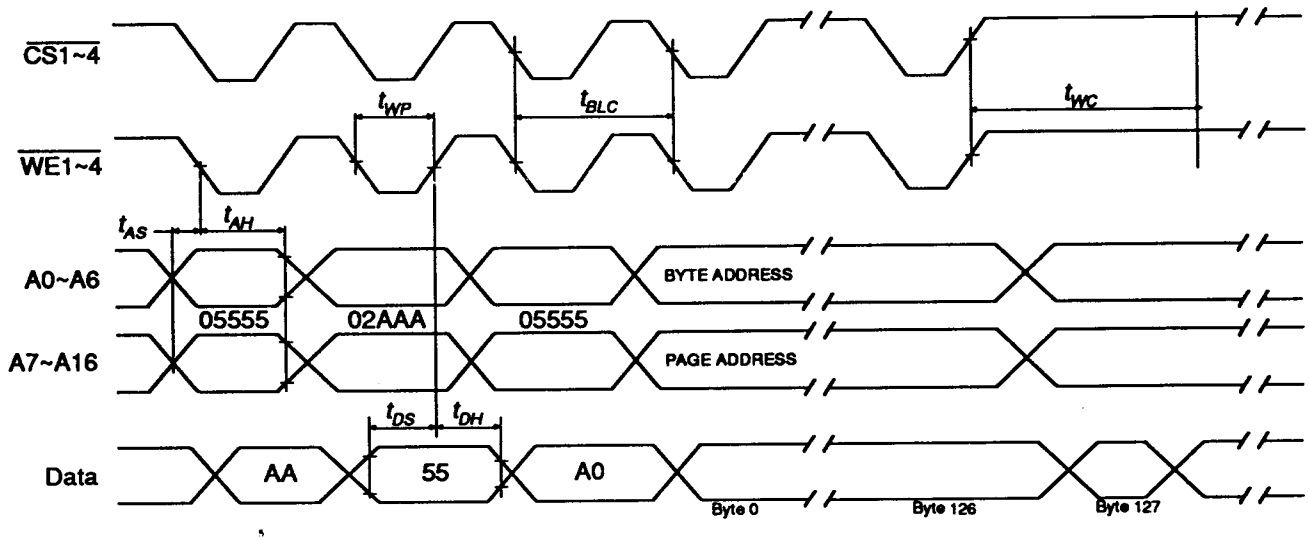
Note: A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS}$).

Page Mode Write Waveform - $\overline{CS}$ Controlled



Note: A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS}$).

Software Protected Write Waveform

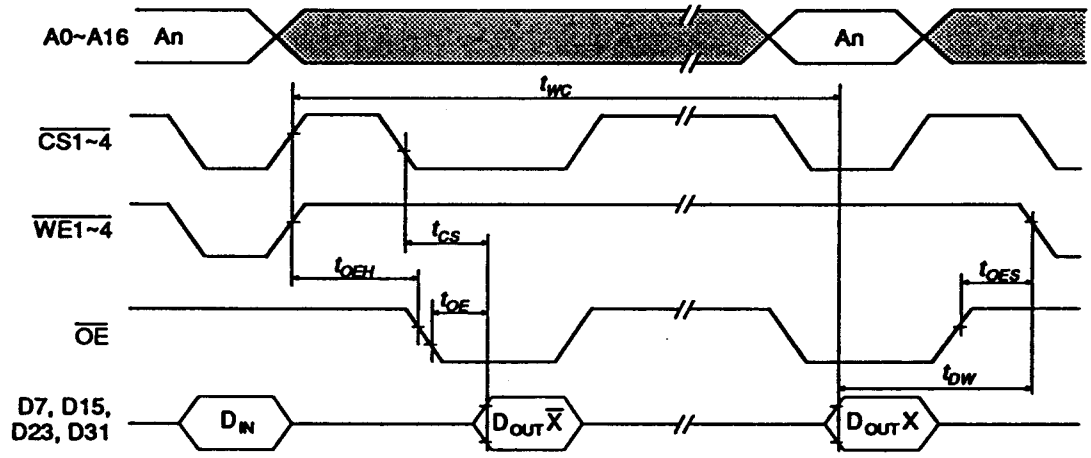


Notes: (1) A7 through A15 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS}$)
(2) The example above is for the PUMA 2E4000X module operating in 8 bit mode.

$\overline{\text{DATA}}$ Polling Characteristics

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Output Enable Hold Time	t_{OEH}	0	-	-	ns
Output Enable Set-up Time	t_{OES}	0	-	-	ns
Write Start Time	t_{DW}	150	-	-	ns
Write Cycle Time	t_{WC}	-	-	15	ms
$\overline{\text{OE}}$ to Output Delay	t_{OE}	10	-	75	ns

$\overline{\text{DATA}}$ Polling Waveform



DEVICE OPERATION

Read

The PUMA 2E4000X is accessed in the same way as a static RAM, with the data stored at the memory location determined by the address pins being placed on the output pins when $\overline{CS1\text{-}4}$ and $\overline{OE}$ are low, and $\overline{WE1\text{-}4}$ are high. Whenever $\overline{CS1\text{-}4}$ or $\overline{OE}$ are high, the outputs are in the OFF or high impedance state.

Write

A low pulse on $\overline{WE1\text{-}4}$ with $\overline{CS1\text{-}4}$ low or a low pulse on $\overline{CS1\text{-}4}$ with $\overline{WE1\text{-}4}$ low indicates a write cycle. The address is latched on the falling edge of $\overline{CS1\text{-}4}$ or $\overline{WE1\text{-}4}$, and the data is latched on the first rising edge of $\overline{CS1\text{-}4}$ or $\overline{WE1\text{-}4}$. Once a byte write has begun it will automatically time itself to completion.

Page Mode Write

This operation mode allows 1 to 128 bytes of data to be loaded into a device, which are then simultaneously written. Once the first byte has been written, each subsequent byte must have the high to low transition of $\overline{WE1\text{-}4}$ (or $\overline{CS1\text{-}4}$) within 30µs of the same transition of the previous byte. If $\overline{CS1\text{-}4}$ and $\overline{WE1\text{-}4}$ are held high for 100µs after a byte has been loaded, the loaded bytes are automatically written. A7 to A16 specify the page address (which must be valid during the above transitions) and A0 to A6 specify which bytes within the page are to be written. Note that the bytes may be loaded in any order and may be changed within the same load period.

$\overline{DATA}$ Polling

In order to detect the end of a Write Cycle, $\overline{DATA}$ Polling is provided. During a Write operation (Byte or Page) an attempt to read the last byte written will result in the complement of the written data appearing on D7 (or D15, D23 or D31, depending on the device selected). Once the Write Cycle is complete, true data appears on the outputs and the next Write Cycle may begin. Using this method of indicating the end of a Write can effectively halve the total write time.

Write Cycle Endurance

Each device used on the PUMA2E4000X is able to withstand at least 10^5 Write/Erase cycles when used in Page Mode, and at least 10^4 such cycles when used in Byte Mode.

Data Protection

Both hardware and software protection is provided as described below.

Four types of hardware protection give high security against accidental writes:

(a) If $\overline{RES}$ is kept low, no devices on the PUMA 2E4000X can be Erased or Programmed, so data can be protected while V_{CC} is switched.

(b) $\overline{OE}$ low, $\overline{CS1\text{-}4}$ or $\overline{WE1\text{-}4}$ high inhibits inadvertent Write Cycles during power-on and power-off. Write Cycle timing specifications must be observed concurrently.

(c) Pulses of less than 20ns on $\overline{WE1\text{-}4}$ do not initiate a Write Cycle.

Software controlled data protection, once enabled by the user, means that a software algorithm must be used before any write can be performed. To enable this feature the algorithm on page 9 is followed, and must be reused for each subsequent write operation. Once set the data protection remains operational until it is disabled by the using the second algorithm; power transitions will not reset this feature.

Operating Modes

The table below shows the logic inputs required to control the operating modes of each EEPROM on the PUMA 2E4000X. Note that $\overline{CS}$ and $\overline{WE}$ below are accessed by $\overline{CS1\text{-}4}$ and $\overline{WE1\text{-}4}$ respectively to allow 8, 16 and 32 bit operation.

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	*Outputs*
Standby	1	X	X	X	High Z
Read	0	0	1	V_H	D_{OUT}
Write	0	1	0	V_H	D_{IN}
Deselect	0	1	1	V_H	High Z
Write Inhibit	X	X	1	X	
	X	0	X	X	
Data Polling	0	0	1	V_H	D_{OUT} (D7)
Program	X	X	X	0	High Z

$1 = V_{IH}$
$0 = V_{IL}$
$V_H = V_{CC}$-1.0V to V_{CC}+1.0V
X = Don't care

Software Data Protection

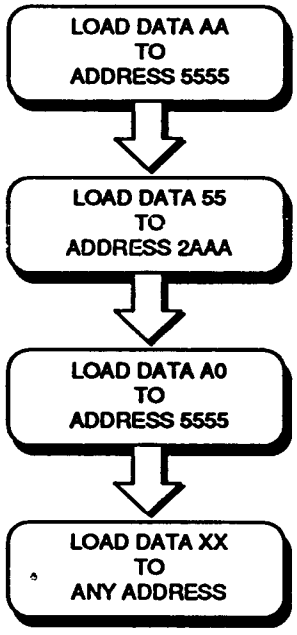
The algorithms below describe the process by which an individual 128K x 8 device on the PUMA may be software write protected and unprotected. Thus, these algorithms apply to the PUMA operating in 8 bit mode; if 16 or 32 bit modes are being used, then the relevant data would be placed on the 16 or 32 bit buses as two or four 8 bit bytes respectively e.g. 5555_H and 55555555_H. In the case of 16 bit mode, this process would be repeated twice with the appropriate devices selected.

The PUMA 2E4000X is shipped with data Protection **NOT ENABLED.** In this mode data should be protected during power-up and power-down operations through the use of external circuits.

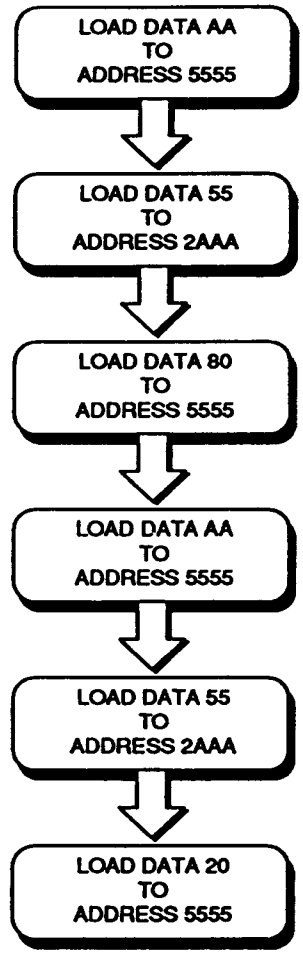
Once data protection has been enabled it is set for the life of the device unless the reset algorithm is followed. In protected mode write operations to the device(s) on the PUMA must be preceeded by a series of three write operations to three specific locations, after which 1 to 128 bytes of data may be written. Once the page load cycle is complete, the device(s) return to the data protected state.

NOTE: Once initiated, the sequence of write operations to Enable and Disable Write Protect should not be interrupted.

Enable Algorithm[1,2,3]



Disable Algorithm[1]



Notes:

(1) Data Format I/O7-I/O0 (Hex);
Once initiated, this sequence of write operations should not be interrupted.

(2) Enable Write Protect state will be initiated at end of write even if no other data is loaded.

(3) 1 to 128 bytes of data may be loaded.

Ordering Information

PUMA 2E4000XMB-20

Speed	15	= 150 ns
	20	= 200 ns
	25	= 250 ns
Temp. range/screening	Blank	= Commercial Temperature
	I	= Industrial Temperature
	M	= Military Temperature
	MB	= Processed to MIL-STD883D Method 5004, non compliant
Special Features	X	= $\overline{\text{RES}}$ function on pin 39
Organization	4000	= 128K x 32, user configurable as 256K x 16 and 512K x 8
Memory Type	E	= EEPROM
Package	PUMA 2	= 66 pin Ceramic PGA.

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