National Semiconductor

July 1988

NM1600/NM1601
65,536 x 1-Bit Static RAM

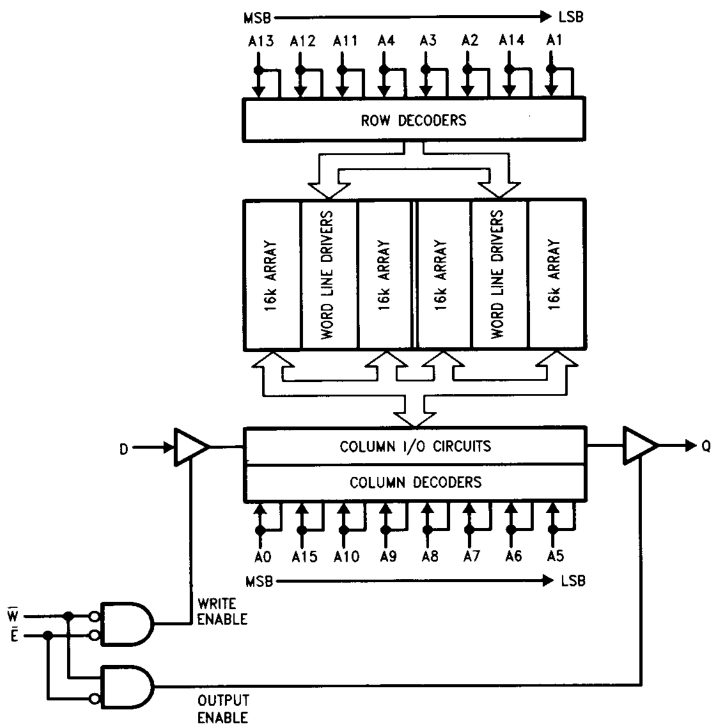
General Description

The NM1600/NM1601 is a 65,536-bit fully-static, asynchronous, random access memory organized as 65,536 words by 1-bit per word. The NM1600/NM1601 is based on an advanced, isoplanar, oxide-isolation CMOS process. The process utilizes fully-implanted CMOS technology, with sub-2 micron design rules and tantalum silicide gate electrodes for high performance. The combination of this high-performance technology, and speed-optimized circuitry results in a very high-speed memory device. The NM1601 is identical to the NM1600 with the additional feature of power down for low power battery backup.

Features

- Fast address access times: 25 ns/30 ns/35 ns (maximum)
- Enable read access faster than address access
- Minimum write cycle time, including moderate system timing skews, equal to minimum read cycle time
- No internal clocks—high speed achieved without address transition detection circuitry
- All inputs and outputs directly TTL compatible
- Separate data input and TRI-STATE® output
- Available in 22-pin DIP, PDIP or LCC
- Low power dissipation (data retention NM1601) I_{CCDR} = 50 μA Max. (2.0V ≤ V_{DR} ≤ 3.0V)
- Data retention supply voltage NM1601: 2.0V to 5.5V

Functional Block Diagram



TL/D/9676-4

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RRD-B20M88/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Input or Output Pin with Respect to V_{SS}	$-2V$ to $V_{CC} + 2V$
Storage Temperaure	$-65°C$ to $+150°C$
Operating Temperature	0°C to +70°C
Power Dissipation	1.0W
Continuous Output Current	25 mA
Average Input or Output Current (Averaged over any 1 μs time interval)	25 mA

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions $T_A = 0°C$ to $+70°C$

	Min	Max	Units
Input HIGH Voltage (V_{IH})	2.2	$V_{CC} + 0.5$	V
Input LOW Voltage (V_{IL})	−1*	0.8	V

All voltages are referenced to V_{SS} pin = 0V.

*The device will withstand undershoots to −3V of 20 ns duration.

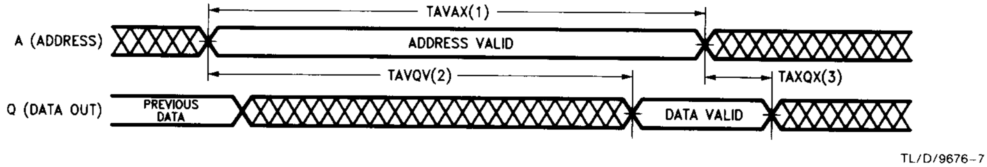
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CCMAX}$ to V_{CCMIN}

No.	Symbol		Parameter	NM1600-25/255 NM1601-25/255		NM1600-30 NM1601-30		NM1600-35 NM1601-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
READ CYCLES										
1	TAVAX	TRC	Address Valid to Address Invalid (Read Cycle Time)	25		30		35		ns
2	TAVQV	TAA	Address Valid to Output Valid (Address Access Time) (Note 5)		25		30		35	ns
3	TAXQX	TOH	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		ns
4	TELEH	TRC	Chip Enable LOW to Chip Enable HIGH (Note 6)	22		27		30		ns
5	TELQV	TACS	Chip Enable LOW to Output Valid (Chip Enable Access Time) (Note 6)		22		27		30	ns
6	TELQX	TLZ	Chip Enable LOW to Output Low Z (Chip Enable to Output Active) (Note 4)	5		5		5		ns
7	TEHQZ	THZ	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable) (Note 9)	0	10	0	12	0	15	ns
8	TELICC	TPU	Chip Enable LOW to Operating Supply Current (Note 4)	0		0		0		ns
9	TEHISB	TPD	Chip Enable HIGH to Standby Current (Note 4)		25		27		30	ns

Timing Waveforms

Read Cycle 1



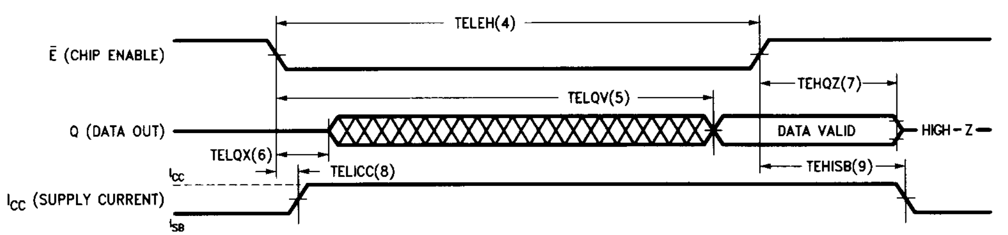
Access is under address control where $\overline{E}$ is active prior to or within 5 ns of address change. $\overline{W}$ = HIGH.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CCMAX}$ to V_{CCMIN} (Continued)

No.	Symbol		Parameter	NM1600-25/255 NM1601-25/255		NM1600-30 NM1601-30		NM1600-35 NM1601-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
WRITE CYCLE 1										
10	TAVAX	TWC	Address Valid to Address Invalid (Write Cycle Time)	25		30		35		ns
11	TWLEH	TWP	Write LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
12	TAVWH	TAW	Address Valid to Write HIGH (Address Setup to End of Write) (Note 7)	19		22		25		ns
13	TWHAX	TAH	Write HIGH to Address Don't Care (Address Hold after End of Write (Notes 7 & 12)	0		0		0		ns
14	TWLWH	TWP	Write LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
15	TAVWL	TAS	Address Valid to Write LOW (Address Setup to Beginning of Write) (Notes 7 & 8)	0		0		0		ns
16	TDVWH	TDS	Data Valid to Write HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		10		12		ns
17	TWHDX	TDH	Write HIGH to Data Don't Care (Data Hold after End of Write) (Notes 7 & 12)	0		0		0		ns
18	TWLQZ	TWZ	Write LOW to Output High Z (Write Enable to Output Disable) (Note 9)	0	9	0	12	0	12	ns
19	TWHQX	TOW	Write HIGH to Output Don't Care (Output Active after End of Write) (Note 4)	5		5		5		ns

Timing Waveforms (Continued)

Read Cycle 2



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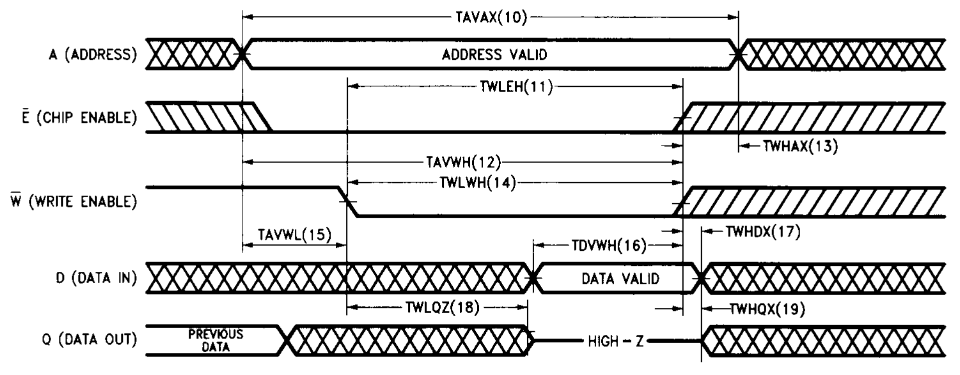
Where address is valid a minimum of 5 ns prior to Ē becoming active (LOW). W̄ = HIGH.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CCMAX}$ to V_{CCMIN} (Continued)

No.	Symbol Standard	Symbol Alternate	Parameter	NM1600-25/255 NM1601-25/255 Min	NM1600-25/255 NM1601-25/255 Max	NM1600-30 NM1601-30 Min	NM1600-30 NM1601-30 Max	NM1600-35 NM1601-35 Min	NM1600-35 NM1601-35 Max	Units
WRITE CYCLE 2										
20	TAVEL	TAS	Address Valid to Chip Enable LOW (Address Setup) (Notes 7 & 8)	0		0		0		ns
21	TELEH	TWP	Chip Enable LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
22	TEHAX	TAH	Chip Enable HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	0		0		0		ns
23	TAVEH	TAW	Address Valid to Chip Enable HIGH (Address Setup to End of Write) (Note 7)	19		22		25		ns
24	TELWH	TWP	Chip Enable LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
25	TDVEH	TDS	Data Valid to Chip Enable HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		10		12		ns
26	TEHDX	TDH	Chip Enable HIGH to Data Don't Care (Data Hold) (Notes 7 & 12)	0		0		0		ns

Timing Waveforms (Continued)

Write Cycle 1



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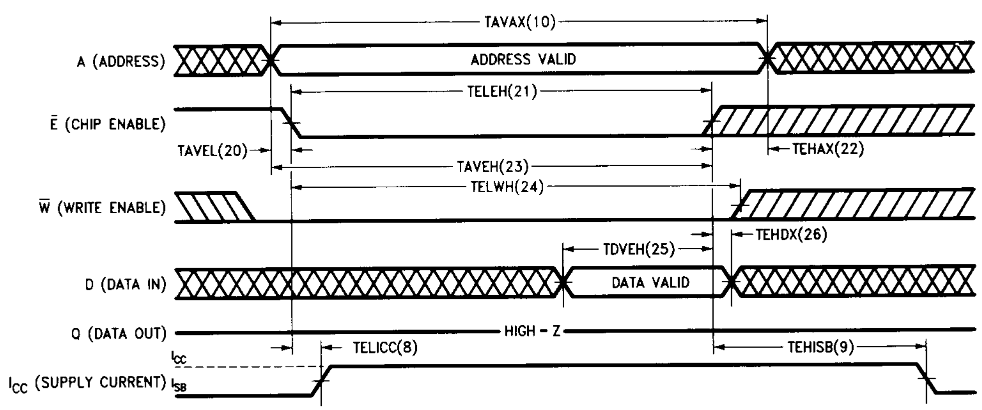
This write cycle is W̄ controlled, where Ē is active (LOW) prior to W̄ becoming active (LOW). In this write cycle the data out may become active, requiring observance of TWLQZ to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if W̄ becomes inactive (HIGH) prior to Ē becoming inactive (HIGH).

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$

Symbol	Parameter	Conditions	NM1600-25/255 NM1601-25/255 Min	NM1600-25/255 NM1601-25/255 Max	NM1600-30 NM1601-30 Min	NM1600-30 NM1601-30 Max	NM1600-35 NM1601-35 Min	NM1600-35 NM1601-35 Max	Units
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		±2		±2		±2	μA
I_{LO}	Output Leakage Current	$\overline{E} = V_{IH}$ or $\overline{W} = V_{IL}$ $V_{SS} \le V_{OUT} \le V_{CC}$		±10		±10		±10	μA
I_{CC}	Dynamic Operating Supply Current	Min Read Cycle Time Duty Cycle = 100% Output Open		90		90		80	mA
I_{SB1}	Standby Supply Current	$\overline{E} = V_{IH}$, (Note 1)		25		25		25	mA
I_{SB2}	Full Standby Supply Current — NM1600	(Note 2)		15		15		15	mA
	Full Standby Supply Current — NM1601	(Note 2)		5		5		5	mA
V_{OL}	Output LOW Voltage	$I_{OL} = 8.0$ mA		0.4		0.4		0.4	V
V_{OH1}	Output HIGH Voltage	$I_{OH1} = -4.0$ mA	2.4		2.4		2.4		V
V_{OH2}	Output HIGH Voltage	$I_{OH2} = -0.05$ mA	$V_{CC} - 0.4$		$V_{CC} - 0.4$		$V_{CC} - 0.4$		V
V_{CC}	Supply Voltage	Except Data Retention Mode	-25: 4.5	-25: 5.5	4.5	5.5	4.5	5.5	V
			-255: 4.75	-255: 5.5					

Timing Waveforms (Continued)

Write Cycle 2



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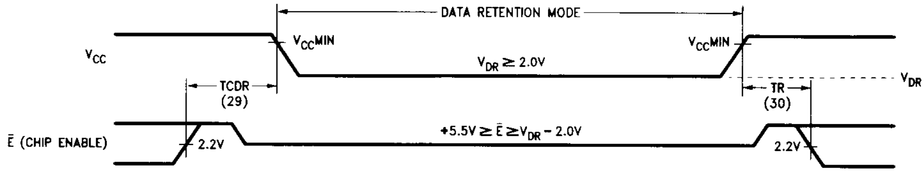
This write cycle is $\overline{E}$ controlled, where $\overline{W}$ is active (LOW) prior to, or coincident with, $\overline{E}$ becoming active (LOW). In this write cycle the data out remains in the high impedance state (TRI-STATE) at the beginning of the write cycle, precluding potential data contention in common I/O applications.

Data Retention Characteristics (NM1601 only) T_A = 0°C to +70°C, V_{CC} = 2.0V to 5.5V

No.	Symbol	Parameter	Conditions		Min	Max	Units
27	V_{DR}	V_{CC} Voltage for Data Retention	$V_{CC} - 0.2V \le \overline{E} \le +5.5V$ $V_{CC} - 0.2V \le V_{IN} \le +5.5V$ or $V_{SS} - 0.2V \le V_{IN} \le V_{SS} + 0.2V$		2.0	5.5	V
28	I_{CCDR}	Data Retention Current (Note 14)	V_{DR} = 3.0V	T_A = 0°C to +70°C		50	μA
			V_{DR} = 2.0V			35	
29	TCDR	Chip Disable to Data Retention Time (Note 4)			0		ns
30	TR	Recovery Time (Notes 4 & 13)			t_{AVAX}		ns

Data Retention Waveform



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Note 1: Standby supply current (TTL) is measured with $\overline{E}$ HIGH (chip deselected) and inputs steady state at valid V_{IL} or V_{IH} levels.

Note 2: Full standby supply current (CMOS) is measured with the enable bar input satisfying the condition: $V_{CC} - 0.2V \le \overline{E} \le V_{CC} + 0.2V$, and all other inputs, (including the data inputs) at steady state and satisfying one of two conditions: Either, $V_{CC} - 0.2V \le V_{IN} \le V_{CC} + 0.2V$ or $V_{SS} - 0.2V \le V_{IN} \le V_{SS} + 0.2V$. This condition results in a significant reduction in current in the input buffers and consequently a lower overall current level.

Note 3: Operation to specifications guaranteed 2.0 ms after V_{CC} reaches minimum operation voltage.

Note 4: This parameter is sampled, not 100% tested.

Note 5: Address Access Time (Read Cycle 1) assumes that $\overline{E}$ occurs before, or within 5 ns after addresses are valid. Timing considerations are referenced to the edges of Address Valid.

Note 6: Enable Access Time (Read Cycle 2) assumes that addresses are valid at least 5 ns prior to $\overline{E}$ transitioning LOW (active). Timing considerations are then referenced to the LOW (active) transitioning edge of $\overline{E}$.

Note 7: A write condition exists only during intervals where both $\overline{W}$ and $\overline{E}$ are LOW (active). The internal Write starts when the second of these signals becomes LOW (active). The internal Write ends when either of these signals transitions HIGH (inactive).

Note 8: Address setup to beginning of write is measured from the time when the last address input becomes valid to the time when the second of the two signals ($\overline{E}$ or $\overline{W}$) becomes LOW (active). The timing of the first signal ($\overline{W}$ or $\overline{E}$) to transition LOW (active) is a Don't Care.

Note 9: Transition to the high-impedance state is measured at a ± 500 mV change from a valid V_{OH} of V_{OL} steady state voltage with the loading specified in *Figure 2*. This parameter is sampled, not 100% tested.

Note 10: Write pulse width is measured from the time when the last of the two signals $\overline{E}$ and $\overline{W}$ becomes LOW (active) to the time of the first of $\overline{E}$ or $\overline{W}$ to transition HIGH (inactive).

Note 11: For rise or fall times greater than 3 ns, the timing relationships can no longer be specified to the time when inputs cross the 1.5V level. This is a characteristic of any CMOS device operated outisde specified switching levels of transition times.

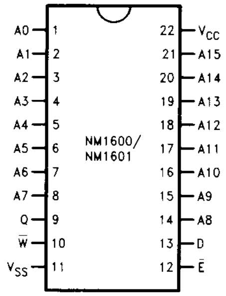
Note 12: Timing specifications of Data Setup to End of Write, Data Hold After End of Write, and Address Hold After End of Write are all referenced to the time when the first of $\overline{E}$ or $\overline{W}$ transitions HIGH (inactive). The timing of the second signal ($\overline{W}$ or $\overline{E}$) to transition HIGH (inactive) is a Don't Care.

Note 13: TAVAX = Read Cycle Timing.

Note 14: I_{CCDR} is tested with V_{IN} = 0V or 5.5V.

Connection Diagrams

22-Pin DIP (J) and PDIP (N)



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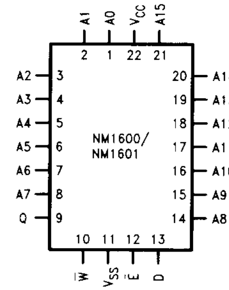
Top View

Order Number*
NM1600J25, NM1600J255, NM1600J30, NM1600J35, NM1600N25, NM1600N255, NM1600N30, NM1600N35, NM1601J25, NM1601J255, NM1601J30, NM1601J35, NM1601N25, NM1601N255, NM1601N30 or NM1601N35
See NS Package Number D22D* or N22B*

*Call factory for package outlines and dimensions.

22-Pin LCC (E)



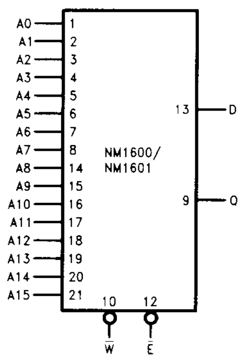
TL/D/9676-2

Top View

Order Number*
NM1600E25, NM1600E255, NM1600E30, NM1600E35, NM1601E25, NM1601E255, NM1601E30 or NM1601E35
See NS Package Number E22A*

*Call factory for package outlines and dimensions.

Logic Symbol



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Pin Names

A_0–A_{15}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
V_{CC}	Power (5.0V)
V_{SS}	Ground (0V)

AC Test Conditions (Notes 3 & 11)

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Reference Levels	1.5V
Output Load	(See *Figures 1* and *2*)

Capacitance (Note 4)

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	7	pF

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$.

Truth Table

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power Level
Standby	H	X	X	HIGH Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	HIGH Z	Active

HIGH Z = High impedance
D = Valid data bit
X = Don't care

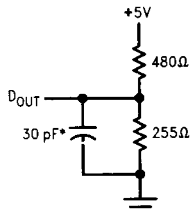

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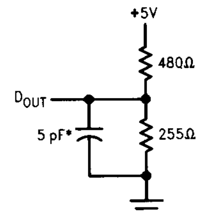
FIGURE 1. Output Load



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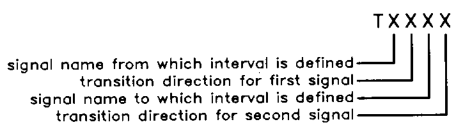
*including scope and jig.

FIGURE 2. Output Load (for TEHQZ, TELQX, TWLQZ, TWHQX)

STANDARD TIMING PARAMETER ABBREVIATIONS



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The transition definitions used in this data sheet are:

H = transition to high state.
L = transition to low state.
V = transition to valid state.
X = transition to invalid or don't care condition.
Z = transition to off (high impedance) condition.

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INVALID or Don't Care.

TL/D/9676-13

Transition from HIGH to LOW level, may occur any time during this period.

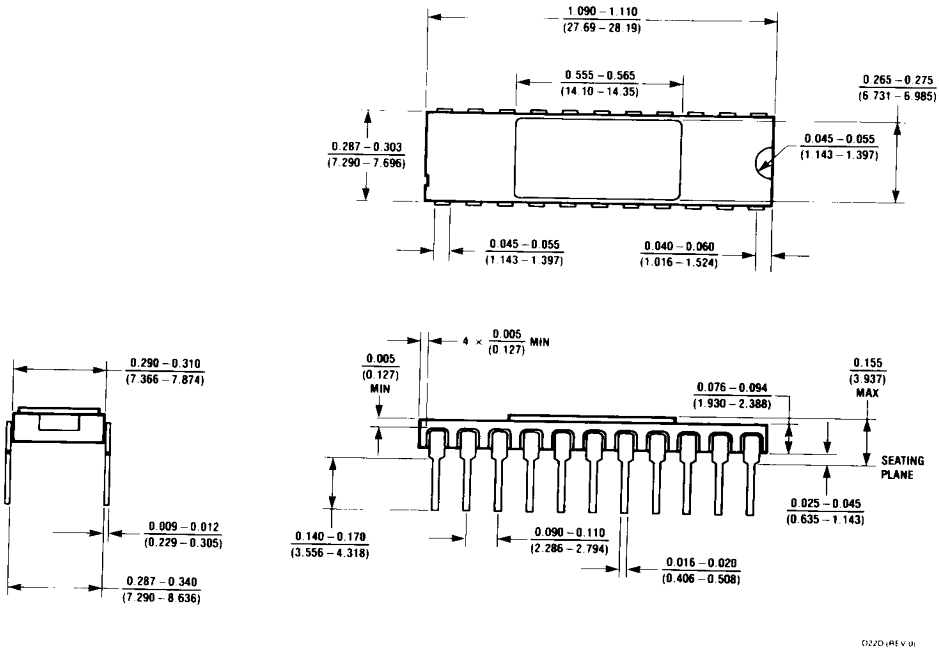
TL/D/9676-14

Transition from LOW to HIGH level, may occur any time during this period.

TIMING VALUES

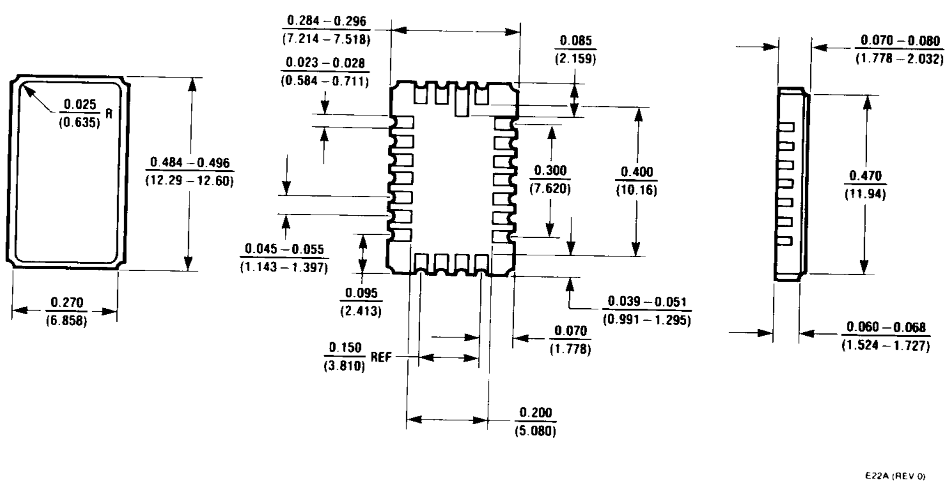
The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for each device parameter. Those timing parameters which state a minimum value do so because the system must supply at least that much time, even though most devices don't require that full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory (like access times) are specified as a maximum time because the device will never provide the data later than this stated value, and will usually provide it much sooner than this.

Physical Dimensions inches (millimeters)



22-Pin Side-Brazed Package (J)
Order Number NM1620J25, NM1620J255, NM1620J30, NM1620J35,
NM1621J25, NM1621J255, NM1621J30 or NM1621J35
NS Package Number D22D*

*Call factory for package outlines and dimensions.

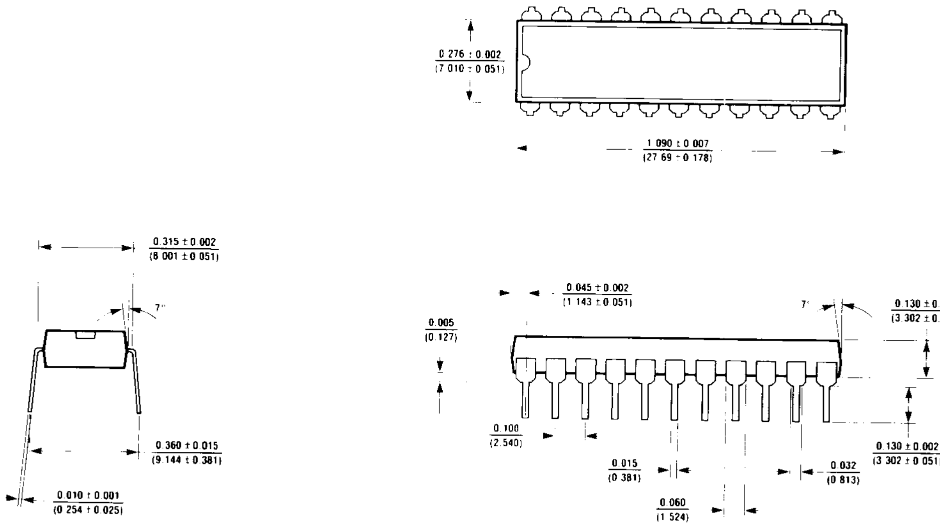


22-Pin Leadless Chip Carrier (E)
Order Number NM1620E25, NM1620E255, NM1620E30, NM1620E35,
NM1621E25, NM1621E255, NM1621E30 or NM1621E35
NS Package Number E22A*

*Call factory for package outlines and dimensions.

Physical Dimensions inches (millimeters) (Continued)

Lit. # 112227



22-Pin Plastic DIP Package (N)
Order Number NM1620N25, NM1620N255, NM1620N30, NM1620N35, NM1621N25, NM1621N255, NM1621N30 or NM1621N35
NS Package Number N22B*

*Call factory for package outlines and dimensions.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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