EC² low profile T²L COMPATIBLE 3-BIT LEADLESS CHIP CARRIER PROGRAMMABLE LOGIC DELAY LINE

- T²L input and output
- Delays stable and precise
- Leadless Chip Carrier (.240 high)
- Available in delays up to 357ns
- Available in 22 Delay steps with resolution from 1 to 50ns
- Propagation delays fully compensated
- All delays digitally programmable
- 10 T²L fan—out capacity

in a minimum-sized leadless chip carrier package compatible with Schottky T²L and DTL circuits. These modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50 °C ground fixed environment, is in excess of 2 million hours. The design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the required delay.

design notes

The "Leadless Chip Carrier Series" of Programmable Logic Delay Lines are a repackaged version of our industry-standard PTTLDL series of Programmable Logic Delay Lines to keep abreast of the ever-changing industry requirements. They have been designed to allow for final delay adjustment during or after installation in a circuit. These programmable logic delay lines incorporate required driving and pickoff circuitry and are contained

The Logic Delay Lines are digitally programmable by the presence of either a "1" or a "0" at each of the programming pins. Since the input and output terminals are fixed and the programming is accomplished only by DC voltage levels, programming may be accomplished by remote switching or permanent termination of the appropriate programming pins of the Logic Delay Line to ground; the Logic Delay Line may also be programmed automatically by computer generated data. MUX set-up time is 4ns typical. When no need exists in the application to change delay time during normal use, the desired delay is most conveniently established by use of a ground pad around each programming pin; programming is accomplished by cutting off those pins which are to remain at state "1" before insertion of the Logic Delay Line onto the printed circuit board.

EC² engineered components company

3580 Sacramento Drive, P. O. Box 8121, San Luis Obispo, CA 93403-8121
Phone: (805) 544-3800

DESIGN NOTES (continued)

The LCPDL-TTL is offered in 22 models with time delays to a maximum of 357ns and with step resolution as shown in the Part Number Table. Programming of maximum delays is accomplished in 8 delay steps in accordance with the Truth Table Examples shown on Page 3. Tolerances on minimum delay, delay change per step and deviation from programmed delay are shown in the Part Number Table on page 3.

Delay time is measured at the +1.5V level on the leading edge. Rise time for all modules is 4ns maximum, when measured from 0.75V to 2.4V. Temperature coefficient of delay is approximately −300 ppm/°C over the operating temperature range of 0 to +70° C.

The LCPDL-TTL is designed for use with positive input pulses and will reproduce these at the output without inversion. Input current is approximately −5ma with an input level of .25V. For an input level of 3.5V, input current is approximately 4ma on modules with a delay change of 1 to 5ns per step, approximately 17ma on modules with a delay change of 6 to 10ns per step and approximately 20ma on modules with a delay change of 11ns and greater per step. All modules can be driven by a standard Schottky T^{2}L gate. Output is Schottky T^{2}L toggle; programming inputs are Schottky T^{2}L single fan-in. These logic delay lines have the capability of driving up to 10 T^{2}L loads.

These "Leadless Chip Carrier Series" programmable logic delay lines are packaged in a leadless chip carrier housing molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Leads meet the solderability requirements of MIL-STD-202, Method 208. The terminations of the module provide positive standoff from the printed circuit board to permit solder reflow attachment and flush cleaning of solder-flux residue for improved reliability.

Marking consists of manufacturer's logo (EC^2), Federal Supply Code, part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW
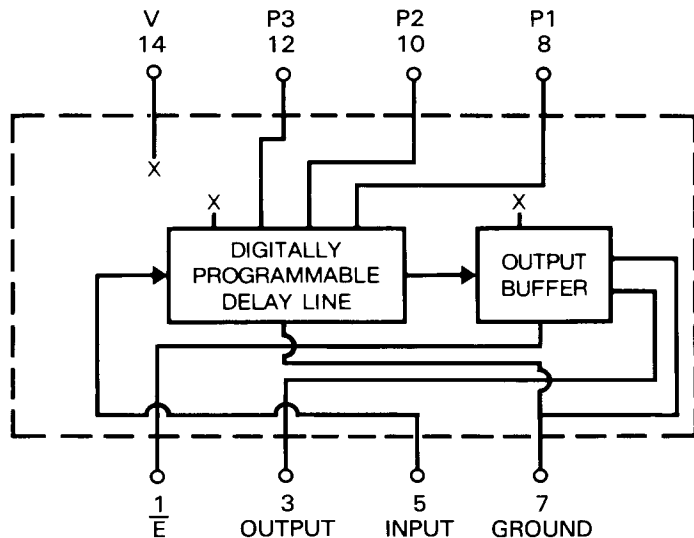
MECHANICAL DETAIL IS SHOWN BELOW
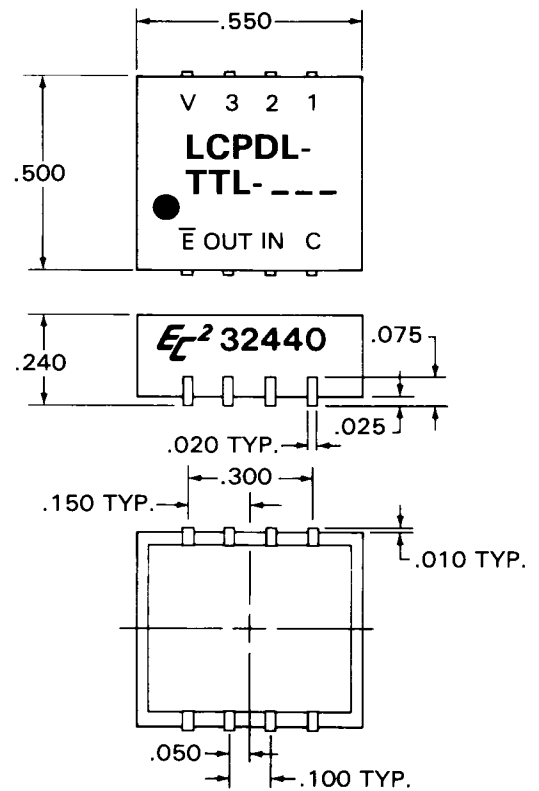
TEST CONDITIONS

1. All measurements are made at 25°C.
2. V$_{CC}$ supply voltage is maintained at 5.0V DC.
3. All units are tested using a Schottky toggle-type positive input pulse and one Schottky T^{2}L load at the output.
4. Input pulse width used is 600ns. Pulse period for all units is 5000ns.

OPERATING SPECIFICATIONS

* V$_{CC}$ supply voltage: . . . . 4.75 to 5.25V DC

V$_{CC}$ supply current: . . . . 40ma typical

Logic 1 input:
    Voltage . . . . 2V min.; 5.5V max.
    Current (−1 through −5) . . . . . . 3.5V = 4ma max.
    Current (−6 through −10) . . . . 3.5V = 17ma max.
    Current (−11 through −50) . . . . 3.5V = 20ma max.
Logic 0 input:
    Voltage . . . . .8V max.
    Current . . . . .25V = −5ma max.
Logic 1 Voltage out: . . . . 2.4V min.
Logic 0 Voltage out: . . . . .5V max.
Operating temperature range: . . . . . 0 to 70°C.
Storage temperature: . . . . −55 to +125°C.

*Delays increase or decrease approximately 2% for a respective increase or decrease of 5% in supply voltage.

PART NUMBER TABLE

φ DELAYS AND TOLERANCES (in ns)				
Part Number	*Step Zero Delay Time	Maximum Delay Time (Nom)	Delay Change Per step	* *Maximum Deviation From Programmed Delay
LCPDL-TTL-7-1	7.0 ± 1	14	1 ± .3	± .4
LCPDL-TTL-7-2	7.0 ± 1	21	2 ± .4	± .6
LCPDL-TTL-7-3	7.0 ± 1	28	3 ± .5	± .8
LCPDL-TTL-7-4	7.0 ± 1	35	4 ± .5	± .9
LCPDL-TTL-7-5	7.0 ± 1	42	5 ± .5	± 1.0
LCPDL-TTL-7-6	7.0 ± 1	49	6 ± .6	± 1.2
LCPDL-TTL-7-7	7.0 ± 1	56	7 ± .7	± 1.4
LCPDL-TTL-7-8	7.0 ± 1	63	8 ± .8	± 1.6
LCPDL-TTL-7-9	7.0 ± 1	70	9 ± .9	± 1.8
LCPDL-TTL-7-10	7.0 ± 1	77	10 ± 1.0	± 2.0
LCPDL-TTL-7-11	7.0 ± 1	84	11 ± 1.1	± 2.2
LCPDL-TTL-7-12	7.0 ± 1	91	12 ± 1.2	± 2.4
LCPDL-TTL-7-13	7.0 ± 1	98	13 ± 1.3	± 2.6
LCPDL-TTL-7-14	7.0 ± 1	105	14 ± 1.4	± 2.8
LCPDL-TTL-7-15	7.0 ± 1	112	15 ± 1.5	± 3.0
LCPDL-TTL-7-20	7.0 ± 1	147	20 ± 2.0	± 4.0
LCPDL-TTL-7-25	7.0 ± 1	182	25 ± 2.5	± 5.0
LCPDL-TTL-7-30	7.0 ± 1	217	30 ± 3.0	± 6.0
LCPDL-TTL-7-35	7.0 ± 1	252	35 ± 3.5	± 7.0
LCPDL-TTL-7-40	7.0 ± 1	287	40 ± 4.0	± 8.0
LCPDL-TTL-7-45	7.0 ± 1	322	45 ± 4.5	± 9.0
LCPDL-TTL-7-50	7.0 ± 1	357	50 ± 5.0	± 10.0

TRUTH TABLE EXAMPLES

Programming Part Pins Number	3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
LCPDL-TTL-7-1		7	1	2	3	4	5	6	7
LCPDL-TTL-7-2		7	2	4	6	8	10	12	14
LCPDL-TTL-7-3		7	3	6	9	12	15	18	21
ETC.									

* Delay at step zero is referenced to the input pin.

* * All delay times after step zero are referenced to step zero.

φ All modules can be operated with a minimum input pulse width of 40% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified delay times for specific applications.