

Integrated Device Technology, Inc.

# CMOS STATIC RAM 64K (8K x 8-BIT) RESETTABLE RAM

**IDT7165S  
IDT7165L**  
**NOT RECOMMENDED  
FOR NEW DESIGNS <sup>(1)</sup>**

### FEATURES:

- High-speed asynchronous RAM clear on Pin 1 (clears all RAM bits to 0, reset cycle time = 2 x tAA)
- High-speed address access time
  - Military: 35/45/55ns (max.)
  - Commercial: 30/35/45ns (max.)
- High-speed chip select (CS<sub>1</sub>) time
  - Military: 20/25/30 (max.)
  - Commercial: 15/20/25ns (max.)
- Low-power operation
  - IDT7165S
    - Active: 300mW (typ.)
    - Standby: 100μW (typ.)
  - IDT7165L
    - Active: 250mW (typ.)
    - Standby: 30μW (typ.)
- Battery backup operation — 2V data retention voltage (IDT7165L only)
- Produced with CEMOS™ high-performance technology
- Single 5V(+10%) power supply
- Input and output directly TTL-compatible
- Standard 28-pin, 600 mil DIP, 300 mil DIP, 28-pin SOIC, 32-pin LCC and PLCC
- Military product is compliant to MIL-STD-883, Class B

### DESCRIPTION:

The IDT7165 is a high-speed 65,536-bit static RAM, organized 8K x 8, with reset function. The RESET pin provides a single RAM clear control which clears all words in the internal RAM to zero when activated. This allows the memory bits for all locations to be cleared at power-on or system reset, or for a fast clear to be available to graphics, histogramming and other designs where a byte-by-byte RAM clear would cause noticeable system speed degradation.

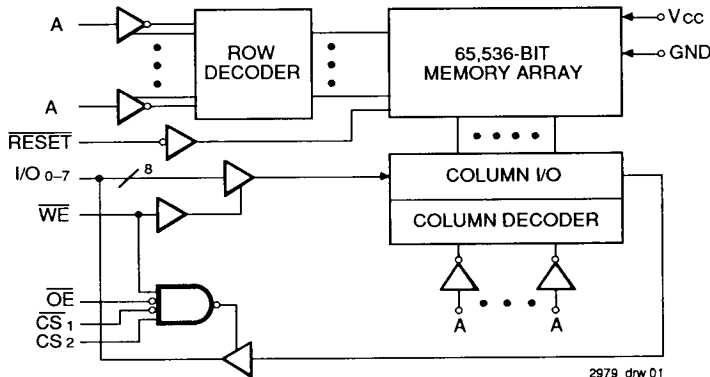
This product is fabricated using IDT's high-performance, high-reliability CEMOS technology. Address access time of 20ns and chip select (CS<sub>1</sub>) time of 15ns are available with maximum power consumption of only 770mW. This circuit also offers a reduced power standby mode. When CS<sub>2</sub> goes low, the circuit will automatically go to and remain in a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30μW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10μW operating from a 2V battery.

The IDT7165 is packaged in a 28-pin 300 or 600 mil DIP, 28-pin gull-wing SOIC, and 32-pin LCC and PLCC, providing high board level densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to the military temperature applications which require instant destruction of sensitive RAM data and demand the highest level of performance and reliability.

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### FUNCTIONAL BLOCK DIAGRAM



### NOTE:

1. Not recommended for new designs. Contact marketing.

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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

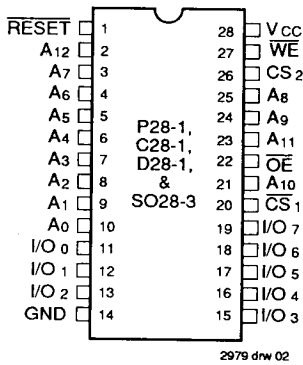
**DECEMBER 1990**

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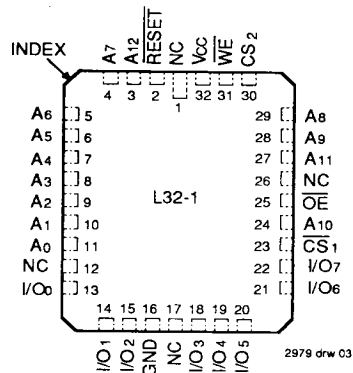
5.18 --/

DSC-1021/2  
1

**PIN CONFIGURATIONS**



2979 drw 02  
**DIP/SOIC  
TOP VIEW**



2979 drw 03  
**LCC/PLCC  
TOP VIEW**

**TRUTH TABLE** ( $V_{CC} = 0.2V, V_{HC} = V_{CC} - 0.2V$ )<sup>(1,2)</sup>

WE	CS <sub>1</sub>	CS <sub>2</sub>	OE	RESET	I/O	Function
X	X	X	X	L	—	Reset all bits to low
X	H	X	X	H	Z	Deselect chip
X	X	L	X	H	Z	Deselect power down <sup>(1)</sup>
X	V <sub>HC</sub>	X	X	H	Z	Deselect chip
X	X	V <sub>LC</sub>	X	V <sub>HC</sub>	Z	CMOS deselect power down <sup>(1)</sup>
H	L	H	H	H	Z	Output disable
H	L	H	L	H	DOUT	Read
L	L	H	X	H	DIN	Write

NOTE:  
1. CS<sub>2</sub> will power down CS<sub>1</sub>, but CS<sub>1</sub> will not power down CS<sub>2</sub>.  
2. H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = don't care.

2979 tbl 01

**PIN DESCRIPTIONS**

A <sub>0-12</sub>	Address
I/O <sub>0-7</sub>	Data Input/Output
CS <sub>1</sub> , CS <sub>2</sub>	Chip Select
RESET	Memory Reset
WE	Write Enable
OE	Output Enable
GND	Ground
V <sub>CC</sub>	Power

2979 tbl 02

**ABSOLUTE MAXIMUM RATINGS**<sup>(1)</sup>

Symbol	Rating	Com'l.	Mil.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

NOTE:  
2979 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE** ( $T_A = +25^\circ C, f = 1.0MHz$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

NOTE:  
2979 tbl 04  
1. This parameter is determined by device characterization, but is not production tested.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2979 tbi 05

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0	V
V <sub>IHR</sub>	RESET Input Voltage	2.5	—	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

NOTE:

1. V<sub>IL</sub> (min.) = -3.0V for pulse width less than 20ns.

2979 tbi 06

**DC ELECTRICAL CHARACTERISTICS<sup>(1, 2)</sup>**

(Vcc = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = Vcc - 0.2V)

Symbol	Parameter	Power	7165S30		7165S/L35		7165S/L45		7165S/L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current CS <sub>1</sub> = V <sub>IL</sub> , CS <sub>2</sub> = V <sub>IH</sub> Outputs Open, Vcc = Max., f = 0	S	110	—	110	125	110	125	110	125	mA
		L	—	—	90	—	90	110	90	110	
ICC2	Dynamic Operating Current CS <sub>1</sub> = V <sub>IL</sub> , CS <sub>2</sub> = V <sub>IH</sub> Outputs Open, Vcc = Max., f = f <sub>MAX</sub>	S	160	—	150	160	150	160	150	160	mA
		L	—	—	130	—	120	130	115	125	
ISB	Standby Power Supply Current (TTL Level) f = f <sub>MAX</sub> CS <sub>1</sub> ≥ V <sub>IH</sub> , CS <sub>2</sub> ≤ V <sub>IL</sub> , RESET ≥ V <sub>IH</sub> Outputs Open, Vcc = Max.	S	20	—	20	20	20	20	20	20	mA
		L	—	—	3	—	3	5	3	5	
ISB1	Full Standby Power Supply Current (CMOS Level) f = 0 CS <sub>2</sub> ≤ V <sub>LC</sub> and RESET ≥ V <sub>HC</sub> Vcc = Max., V <sub>IN</sub> ≥ V <sub>HC</sub> or V <sub>IN</sub> ≤ V <sub>LC</sub>	S	15	—	15	20	15	20	15	20	mA
		L	—	—	0.2	—	0.2	1.0	0.2	1.0	

NOTES:

- All values are maximum guaranteed values.
- At f = f<sub>MAX</sub> address and data are cycling at maximum frequency of read cycles f = 1/trc. f = 0 means no inputs change.

2979 tbi 07

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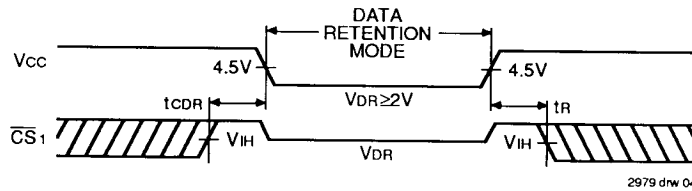
**DC ELECTRICAL CHARACTERISTICS**

Vcc = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT7165S		IDT7165L		Unit	
			Min.	Max.	Min.	Max.		
I <sub>LI</sub>	Input Leakage Current	Vcc = Max., V <sub>IN</sub> = GND to Vcc	MIL.	—	10	—	5	μA
			COM'L.	—	5	—	2	
I <sub>LO</sub>	Output Leakage Current	Vcc = Max., CS = V <sub>IH</sub> , V <sub>OUT</sub> = GND to Vcc	MIL.	—	10	—	5	μA
			COM'L.	—	5	—	2	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 10mA, Vcc = Min.	—	0.5	—	0.5	V	
			—	0.4	—	0.4		
V <sub>OH</sub>	Output High Voltage	I <sub>OL</sub> = -4mA, Vcc = Min.	2.4	—	2.4	—	V	

2979 tbi 08

### LOW V<sub>CC</sub> DATA RETENTION WAVEFORM



### DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Symbol	Parameter	Test Condition	Min.	Typ. <sup>(1)</sup> V <sub>CC</sub> @		Max. V <sub>CC</sub> @		Unit
				2.0V	3.0V	2.0V	3.0V	
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	—	2.0	—	—	—	—	V
I <sub>CCDR</sub>	Data Retention Current	CS <sub>2</sub> ≤ V <sub>LC</sub> , CS <sub>1</sub> ≥ V <sub>HC</sub> RESET ≥ V <sub>HC</sub>	MIL.	10	15	200	300	μA
			COM'L.	10	15	60	90	
t <sub>CDR</sub> <sup>(3)</sup>	Chip Deselect to Data Retention Time		0	—	—	—	—	ns
t <sub>R</sub> <sup>(3)</sup>	Operation Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	—	—	—	—	ns
I <sub>LI</sub>   <sup>(3)</sup>	Input Leakage Current		—	—	—	2	2	μA

**NOTES:**

- TA = +25°C.
- t<sub>RC</sub> = Read Cycle Time.
- This parameter is guaranteed, but not tested.

2979 tbl 08

### AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2979 tbl 09

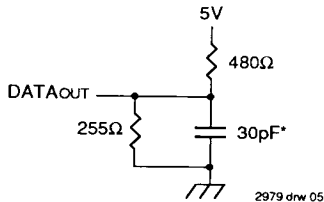


Figure 1. Output Load

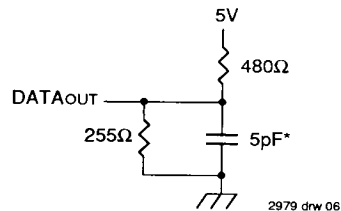


Figure 2. Output Load  
(for t<sub>CLZ1, 2</sub>, t<sub>OLZ</sub>, t<sub>CHZ1, 2</sub>, t<sub>OHZ</sub>, t<sub>OW</sub>, t<sub>WHZ</sub>)

\*Includes scope and jig.

**AC ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7165S30 <sup>(1)</sup>		7165S35 7165L35 <sup>(1)</sup>		7165S45 7165L45		7165S55 <sup>(3)</sup> 7165L55 <sup>(3)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	30	—	35	—	45	—	55	—	ns
t <sub>AA</sub>	Address Access Time	—	30	—	35	—	45	—	55	ns
t <sub>ACS1</sub>	Chip Select-1 Access Time <sup>(2)</sup>	—	15	—	20	—	25	—	30	ns
t <sub>ACS2</sub>	Chip Select-2 Access Time <sup>(2)</sup>	—	35	—	40	—	45	—	55	ns
t <sub>CLZ1</sub>	Chip Select-1 to Output in Low Z <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
t <sub>CLZ2</sub>	Chip Select-2 to Output in Low Z <sup>(4)</sup>	5	—	5	—	5	—	5	—	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	15	—	20	—	25	—	30	ns
t <sub>OLZ</sub>	Output Enable to Output in Low Z <sup>(4)</sup>	3	—	3	—	3	—	3	—	ns
t <sub>CHZ1</sub>	Chip Select-1 to Output in High Z <sup>(4)</sup>	—	13	—	15	—	20	—	25	ns
t <sub>CHZ2</sub>	Chip Select-2 to Output in High Z <sup>(4)</sup>	—	13	—	15	—	20	—	25	ns
t <sub>OHZ</sub>	Output Disable to Output in High Z <sup>(4)</sup>	—	14	—	15	—	20	—	25	ns
t <sub>OH</sub>	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t <sub>PU</sub>	Chip Select to Power Up Time <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
t <sub>PD</sub>	Chip Select to Power Down Time <sup>(4)</sup>	—	30	—	35	—	45	—	55	ns
<b>Write Cycle</b>										
t <sub>WC</sub>	Write Cycle Time	30	—	35	—	45	—	55	—	ns
t <sub>CW1</sub>	Chip Select-1 to End of Write ( $\overline{CS}_1$ )	20	—	20	—	25	—	30	—	ns
t <sub>CW2</sub>	Chip Select-2 to End of Write ( $CS_2$ )	22	—	25	—	33	—	50	—	ns
t <sub>AW</sub>	Address Valid to End of Write	22	—	25	—	33	—	50	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	23	—	25	—	25	—	50	—	ns
t <sub>WR1</sub>	Write Recovery Time ( $\overline{CS}_1$ , $\overline{WE}$ )	0	—	0	—	0	—	0	—	ns
t <sub>WR2</sub>	Write Recovery Time ( $CS_2$ )	5	—	5	—	5	—	5	—	ns
t <sub>WHZ</sub>	Write Enable to Output in High Z <sup>(4)</sup>	—	12	—	14	—	18	—	25	ns
t <sub>DW</sub>	Data to Write Time Overlap	13	—	15	—	20	—	25	—	ns
t <sub>DH1</sub>	Data Hold from Write Time ( $\overline{CS}_1$ )	3	—	3	—	3	—	3	—	ns
t <sub>DH2</sub>	Data Hold from Write Time ( $CS_2$ )	5	—	5	—	5	—	5	—	ns
t <sub>OW</sub>	Output Active from End of Write <sup>(4)</sup>	5	—	5	—	5	—	5	—	ns

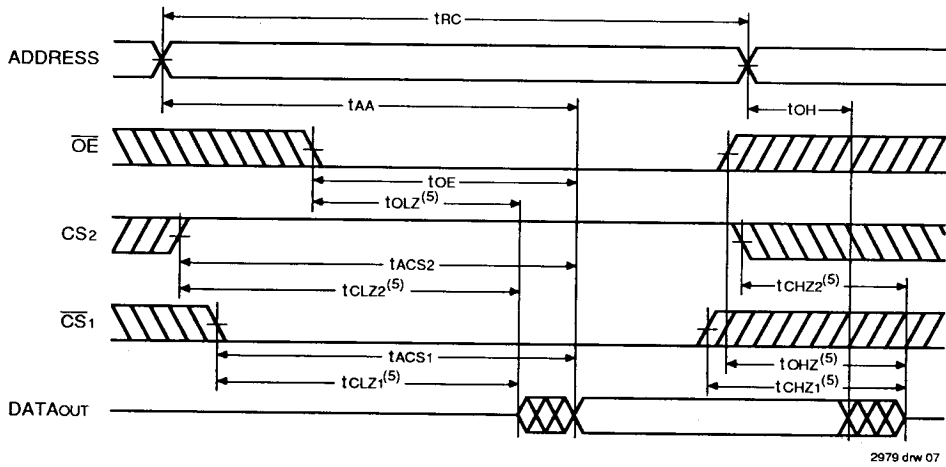
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**NOTES:**

- 0° to +70°C temperature range only.
- Both chip selects must be active for the device to be selected.
- 55°C to +125°C temperature range only.
- This parameter is guaranteed, but not tested.

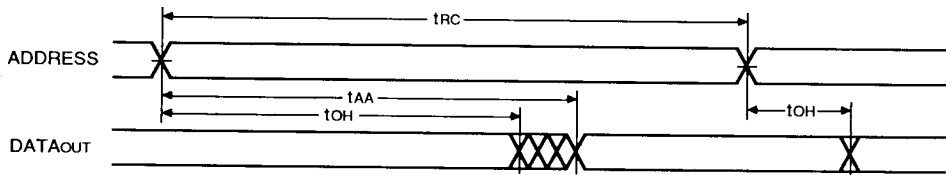
2976 tbl 08

**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>**



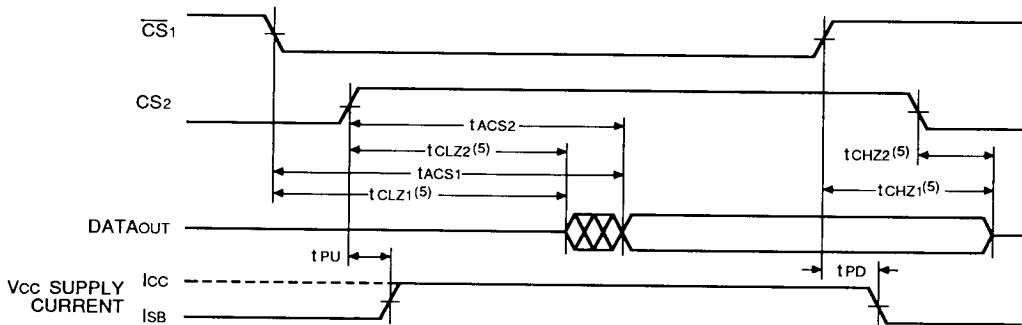
2979 drw 07

**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 2, 4)</sup>**



2979 drw 08

**TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1, 3, 4)</sup>**

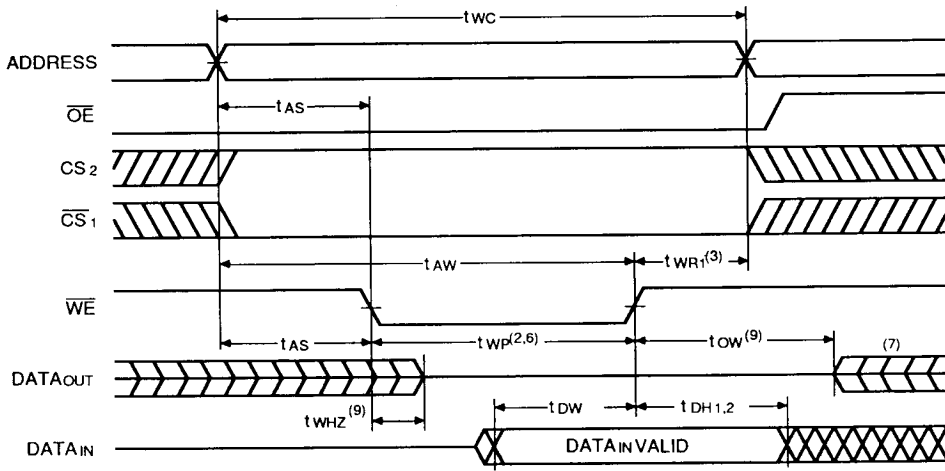


2979 drw 09

**NOTES:**

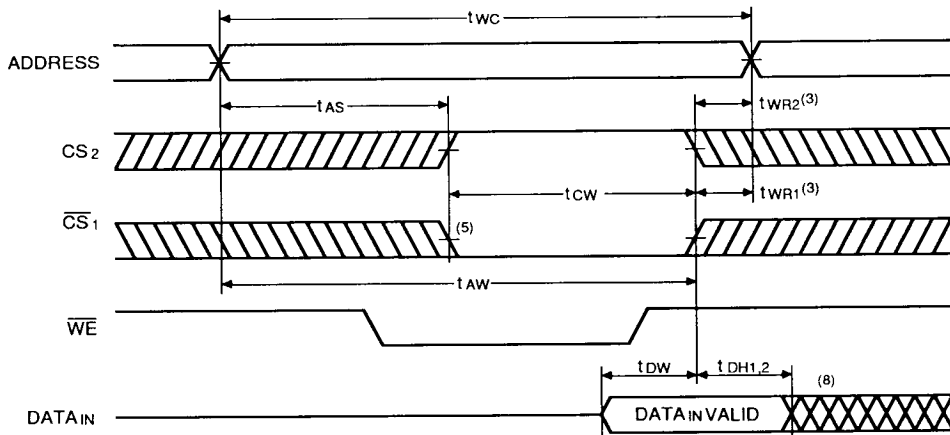
1.  $\overline{WE}$  is high for read cycle.
2. Device is continuously selected,  $\overline{CS1} = V_{IL}$ ,  $CS2 = V_{IH}$ .
3. Address valid prior to or coincident with  $\overline{CS1}$  transition low and  $CS2$  transition high.
4.  $OE = V_{IL}$ .
5. Transition is measured  $\pm 200mV$  from steady state.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1)</sup>**



2979 drw 10

**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED TIMING)<sup>(1)</sup>**



2979 drw 11

**NOTES:**

1.  $\overline{WE}$ ,  $\overline{CS1}$  or  $CS2$  must be inactive during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{WE}$ , a low  $\overline{CS1}$  and a high  $CS2$ .
3.  $t_{WR1,2}$  is measured from the earlier of  $\overline{CS1}$  or  $\overline{WE}$  going high or  $CS2$  going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the  $\overline{CS1}$  low transition or  $CS2$  high transition occurs simultaneously with or after the  $\overline{WE}$  low transition, the outputs remain in a high impedance state.
6. If  $\overline{OE}$  is low during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{WHZ} + t_{DW}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is high during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .
7.  $DATA_{OUT}$  is the same phase of write data of this write cycle.
8. If  $\overline{CS1}$  is low and  $CS2$  is high during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured  $\pm 200mV$  from steady state.

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**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 10\%$ , All Temperature Ranges)

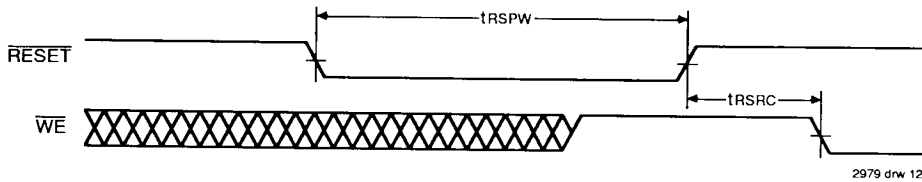
Symbol	Parameter	7165S30 <sup>(1)</sup>		7165S35 7165L35 <sup>(1)</sup>		7165S45 7165L45		7165S55 <sup>(3)</sup> 7165L55 <sup>(3)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
trSPW	Reset Pulse Width <sup>(2)</sup>	55	—	65	—	80	—	100	—	ns
trSRC	Reset High to $\overline{WE}$ Low	5	—	5	—	10	—	10	—	ns

**NOTES:**

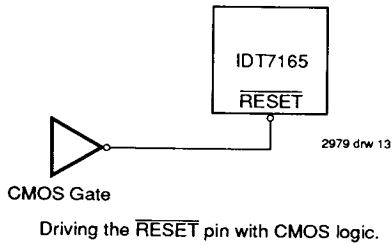
- 0° to +70°C temperature range only.
- Recommended duty cycle = 10% maximum.
- 55°C to +125°C temperature range only.

2976 tbt 09

**RESET TIMING**

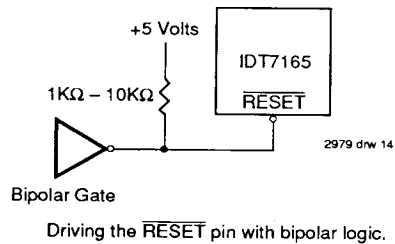


2979 drw 12



2979 drw 13

Driving the  $\overline{RESET}$  pin with CMOS logic.



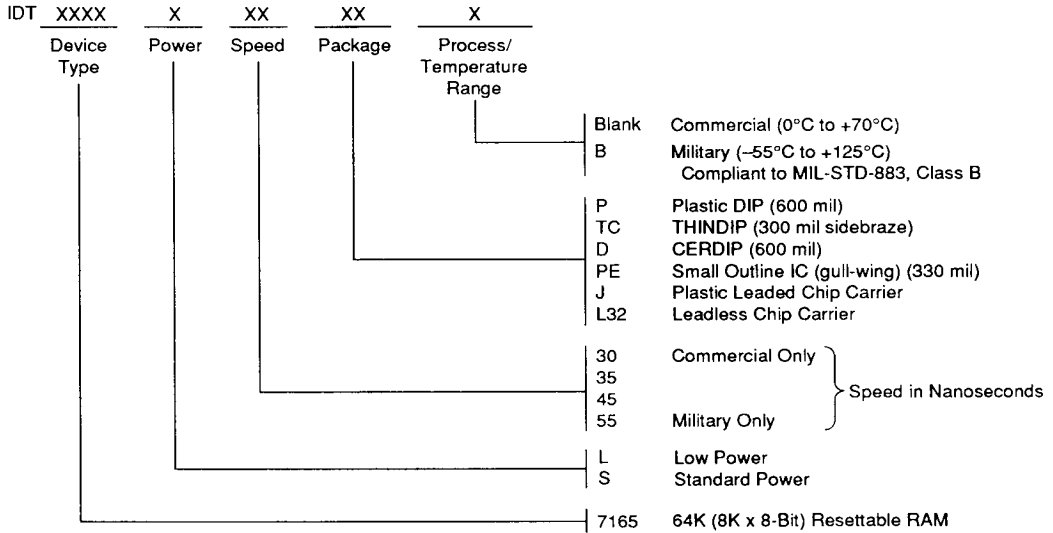
2979 drw 14

Driving the  $\overline{RESET}$  pin with bipolar logic.

Figure 3.



**ORDERING INFORMATION**



2979 drw 15

