HYUNDAI SEMICONDUCTOR HYM581000

1M×8-Bit CMOS DRAM MODULE

M431201B-APR91

T-46-23-17

DESCRIPTION

The HYM581000 is a 1M words by 8 bits dynamic RAM module and consists of eight HY531000J Fast Page mode CMOS DRAM in 20/26 pin SOJ package mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the 1M DRAMs.

HYM581000M is a socket type and HYM581000P is a leaded type single-in-line module, these are suitable for easy interchange and addition of 1M bytes memory.

FEATURES

- Fast Page Mode operation
- Fast access time

	t_{RAC}	t_{CAC}	t_{PC}
HYM581000-60	60	20	40
HYM581000-70	70	20	40
HYM581000-80	80	20	45
HYM581000-10	100	25	55

- Single power supply of 5V± 10%
- $\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh
- Low power operating
  3.74W max (HYM581000-60)
  3.30W max (HYM581000-70)
  2.86W max (HYM581000-80)
  2.42W max (HYM581000-10)
- TTL compatible inputs and outputs
- 512 refresh cycles / 8ms

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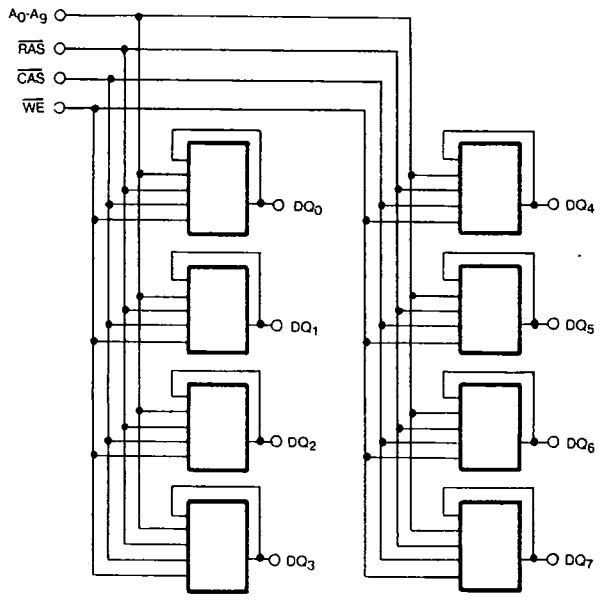
BLOCK DIAGRAM

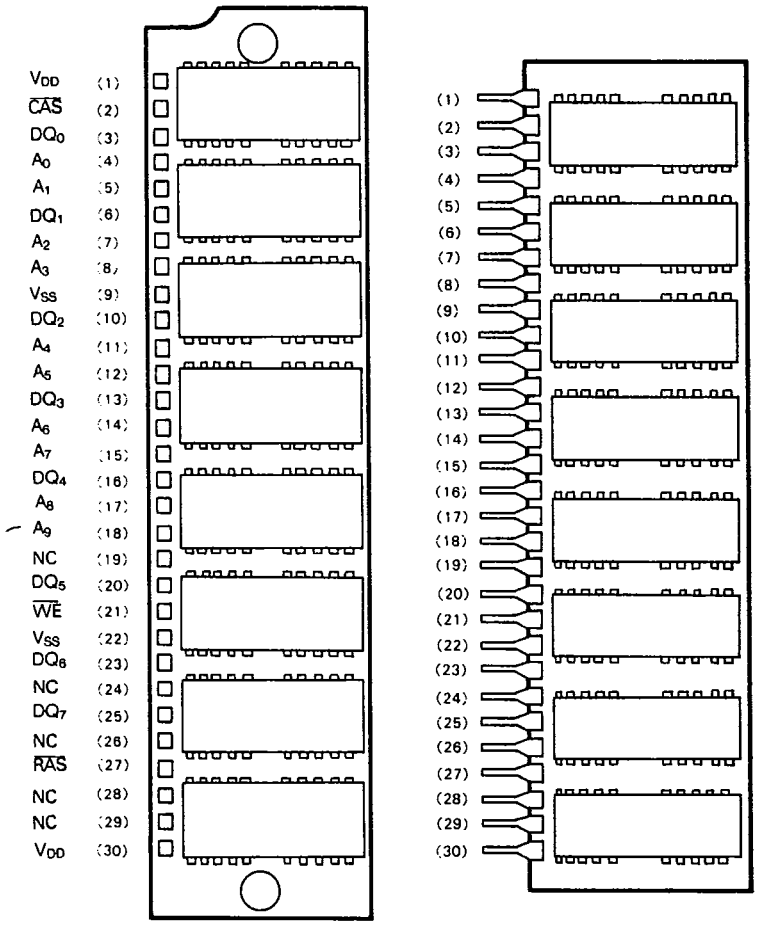


PIN NAMES

A_0–A_9	ADDRESS INPUT
DQ_0–DQ_7	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS

HYM581000M **HYM581000P**



NOTES :
1. HYM581000P's pin configuration is the same as HYM581000M's.
2. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ0-DQ7).
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out(DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	4.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM581000		UNIT	NOTE
				MIN.	MAX		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			80	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60		680	mA	1, 2
			−70		600		
			−80		520		
			−10		440		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}			16	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60		680	mA	2
			−70		600		
			−80		520		
			−10		440		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60		520	mA	1, 2
			−70		440		
			−80		360		
			−10		280		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs ≥ V_{SS}			8	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60		680	mA	2
			−70		600		
			−80		520		
			−10		440		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in fast page mode.

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AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM581000								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120		130		150		180		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		70		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	10		10		10		15		ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		50		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		15		20		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	60	25	75	ns	2
11	t_{RAC}	Access Time From $\overline{RAS}$		60		70		80		100	ns	3,4,5
12	t_{AA}	Access Time From Column Address		30		35		40		50	ns	5,7
13	t_{CAC}	Access Time From $\overline{CAS}$		20		20		20		25	ns	5,6
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		25		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	8
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	8
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		5		ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	0	20	ns	9
21	t_{WP}	Write Command Pulse Width	15		15		15		20		ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
23	t_{AR}	Column Address Hold Time From $\overline{RAS}$	50		55		60		75		ns	
24	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	50		55		60		75		ns	
25	t_{WCS}	Write Command Set-up Time	0		0		0		0		ns	10
26	t_{WCH}	Write Command Hold Time	15		15		15		20		ns	
27	t_{DS}	Data-In Set-up Time	0		0		0		0		ns	11
28	t_{DH}	Data-In Hold Time	15		15		15		20		ns	11
29	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	50		55		60		75		ns	
30	t_{CPA}	Access Time From $\overline{CAS}$ Precharge		35		35		40		50	ns	5,12
31	t_{PC}	Fast page mode Cycle time	40		40		45		55		ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		20		25		ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		20		25		ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		5		ns	

#	SYMBOL	PARAMETER	HYM581000								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15		15		15		20		ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	3	50	ns	13,14
38	t_{CLZ}	$\overline{CAS}$ to output in Low-z	0		0		0		0		ns	5
39	t_{REF}	Refresh Interval(512 Cycle)		8		8		8		8	ms	15
40	t_{RASP}	Fast page Mode $\overline{RAS}$ Pulse Width	60		70		80		100		ns	
41	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40		40		40		50		ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then the access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max). If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max).
4. Assume $t_{RCD} \leq t_{RCD}$(max). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max).
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max).
7. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \geq t_{RAD}$(max).
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{OFF} and t_{OH} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
10. t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as a electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max).
14. AC measurements assume t_T = 5ns.
15. An initial pause of 200us is required after power-up and followed at least 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

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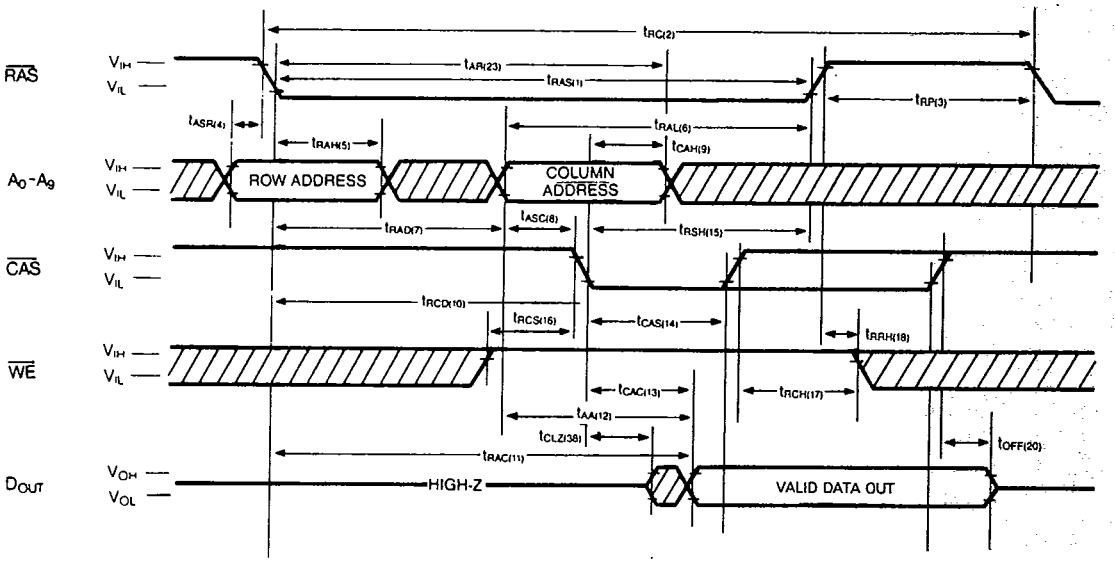
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

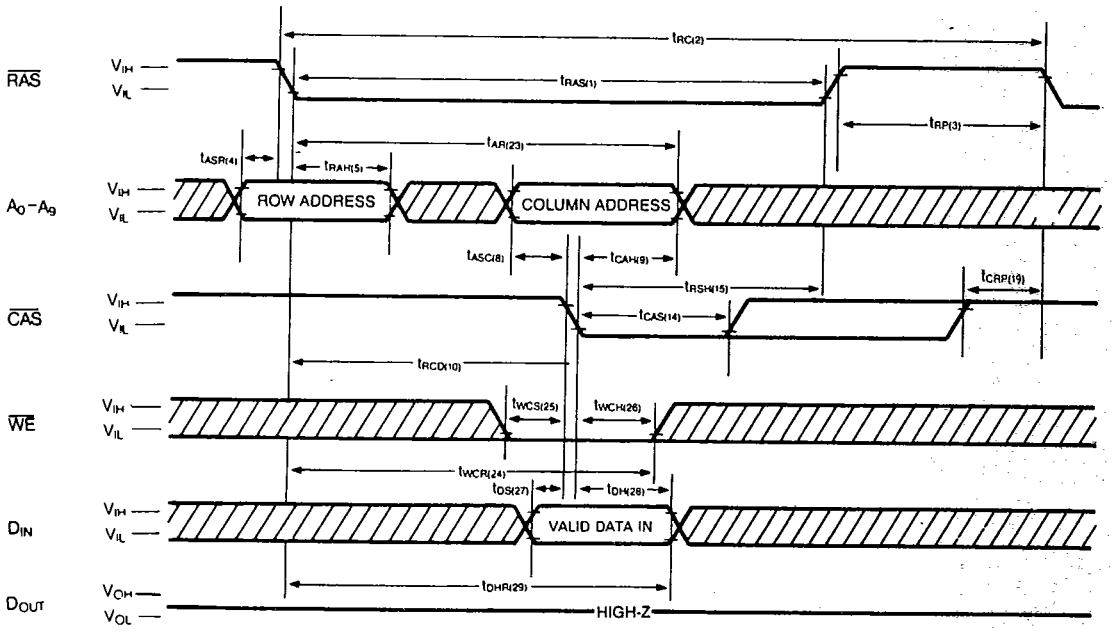
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0−A_9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)		55	pF
C_{DQ}	I/O Capacitance(DQ_0−DQ_7)		15	pF

TIMING DIAGRAM

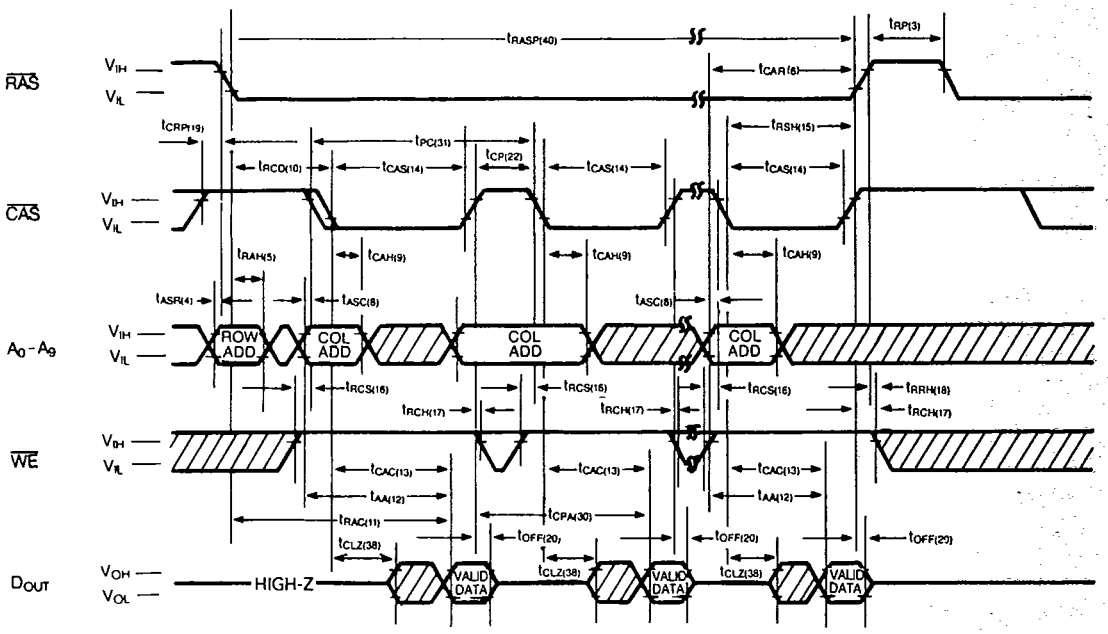
READ CYCLE



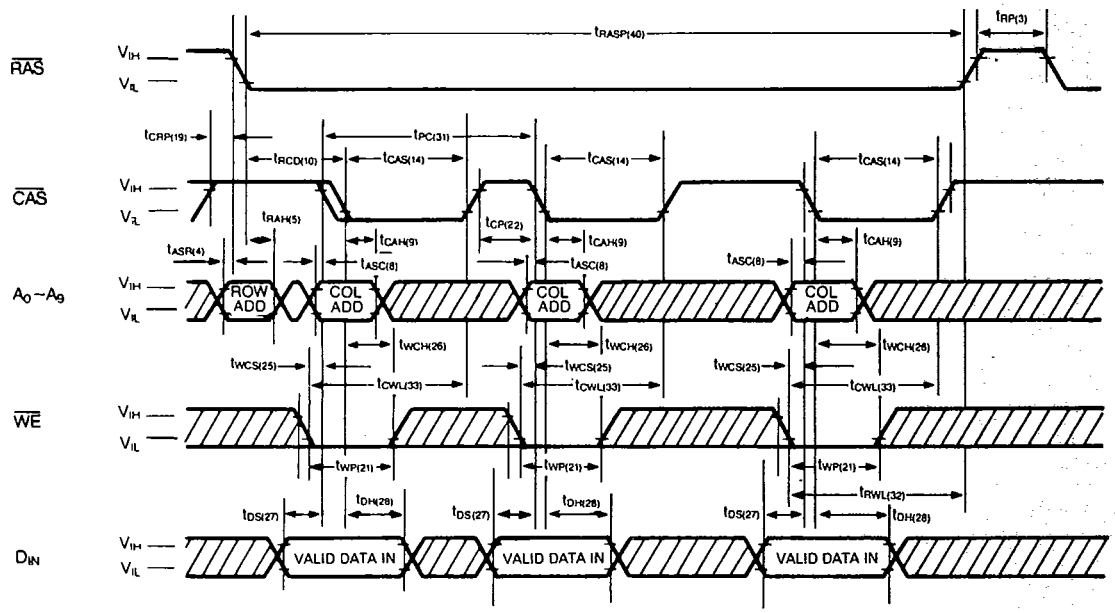
EARLY WRITE CYCLE



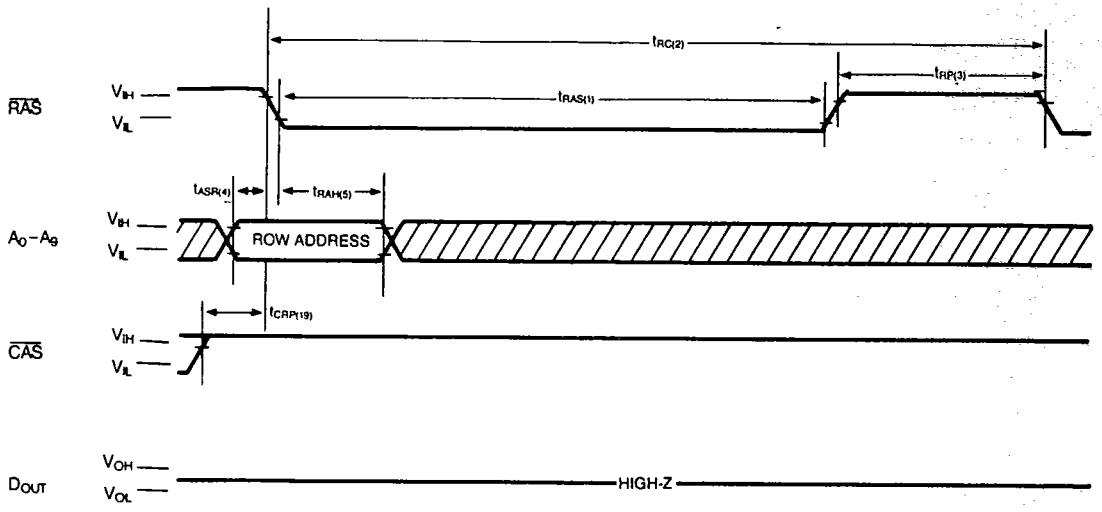
FAST PAGE MODE READ CYCLE



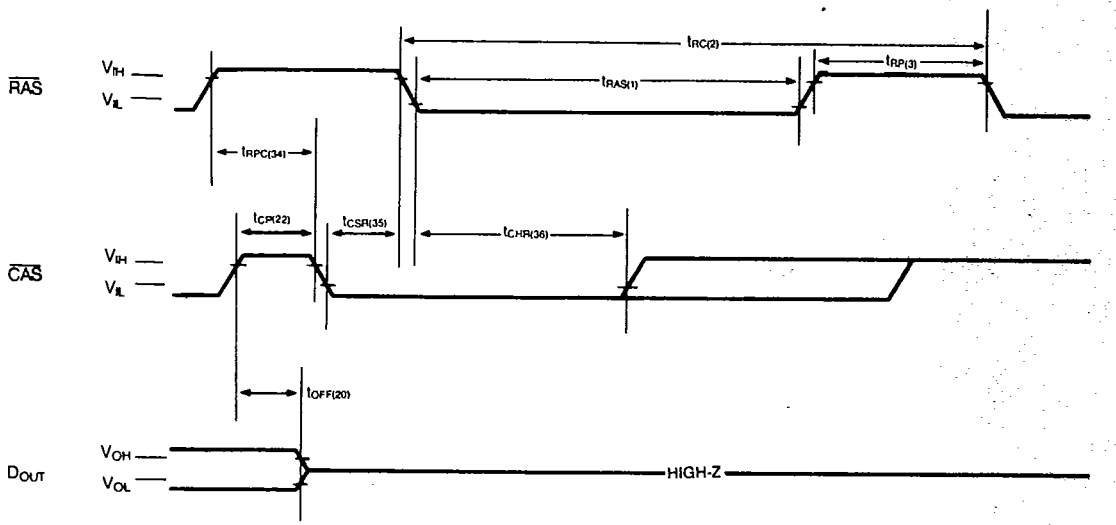
FAST PAGE MODE EARLY WRITE CYCLE



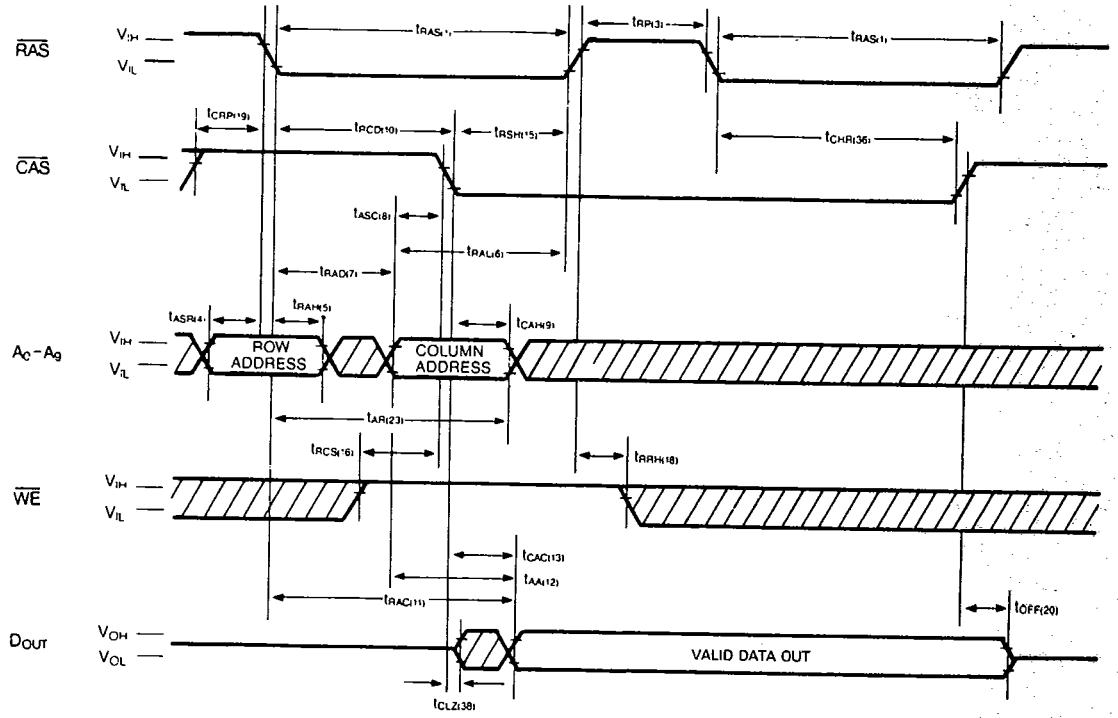
$\overline{RAS}$-ONLY REFRESH CYCLE



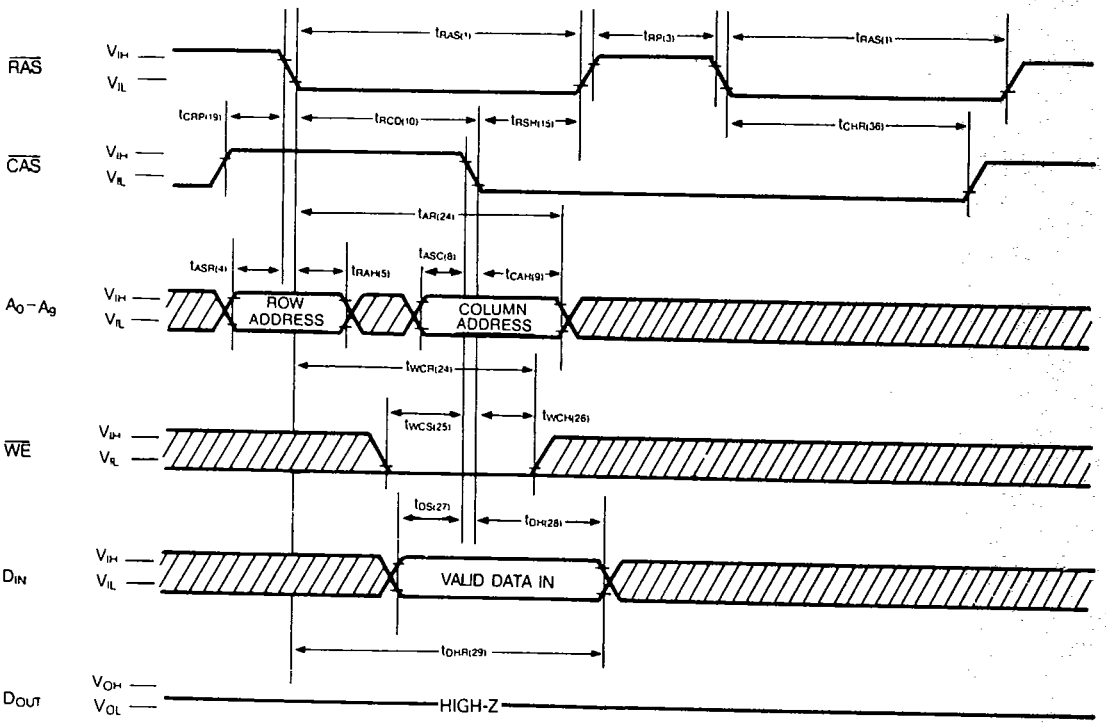
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE