Description

The Edge670 is a monolithic ATE pin electronics comparator manufactured in a high-performance complementary bipolar process. In automatic test equipment, the Edge670 offers a window comparator suitable for very fast, bidirectional channels in Memory, VLSI, and Mixed-Signal test systems.

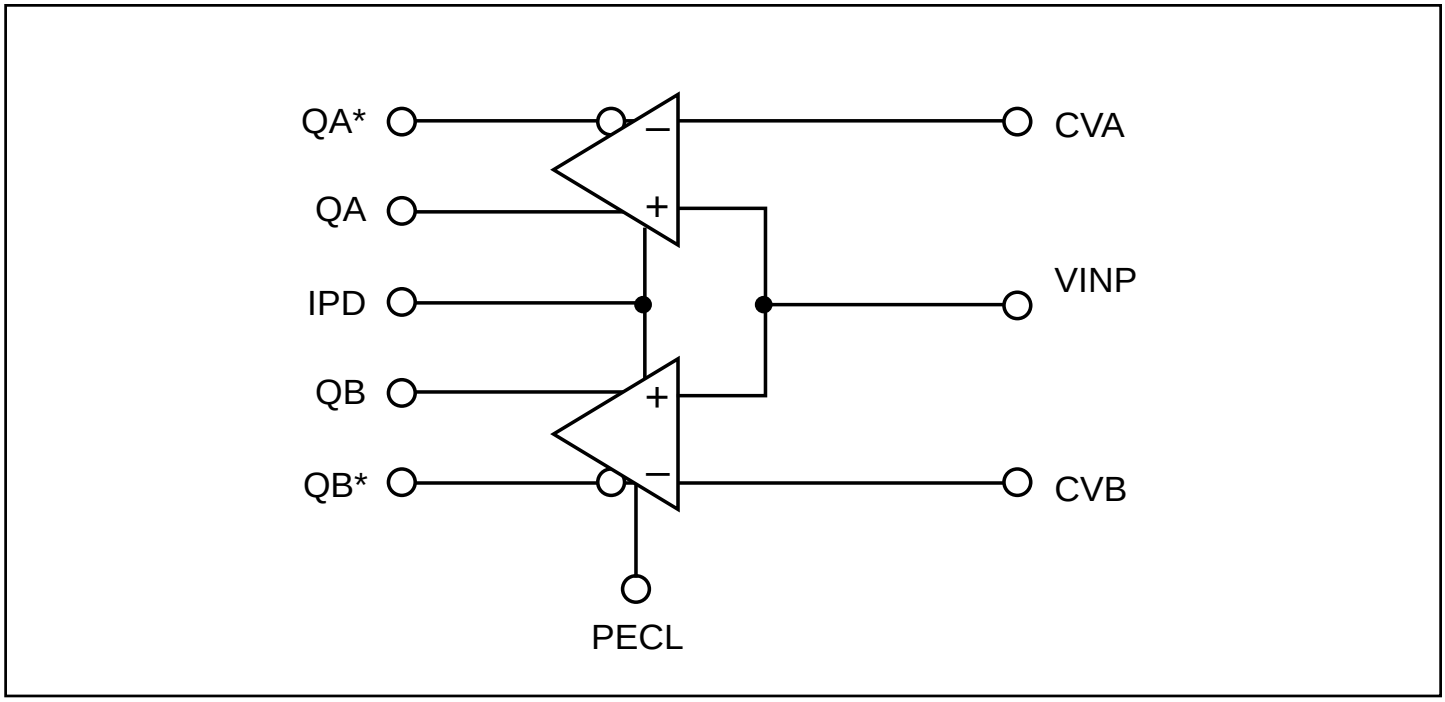
The 670 is capable of tracking very fast edges and passing sub-ns pulses over an 11V common mode range while maintaining excellent timing accuracy. The differential digital outputs are adjustable to accommodate ECL levels, PECL levels, or custom levels to interface directly with a CMOS ASIC.

The Edge670 is pin compatible with the Edge672, except no load is present.

Features

- 11V Common Mode Range
- Input Tracking > 6 V/ns with < ±25 ps dispersion
- Low Leakage (<1 µA)
- Input Power Down Mode (for extremely low leakage operation (<250 nA))
- Small footprint (32 pin TQFP)

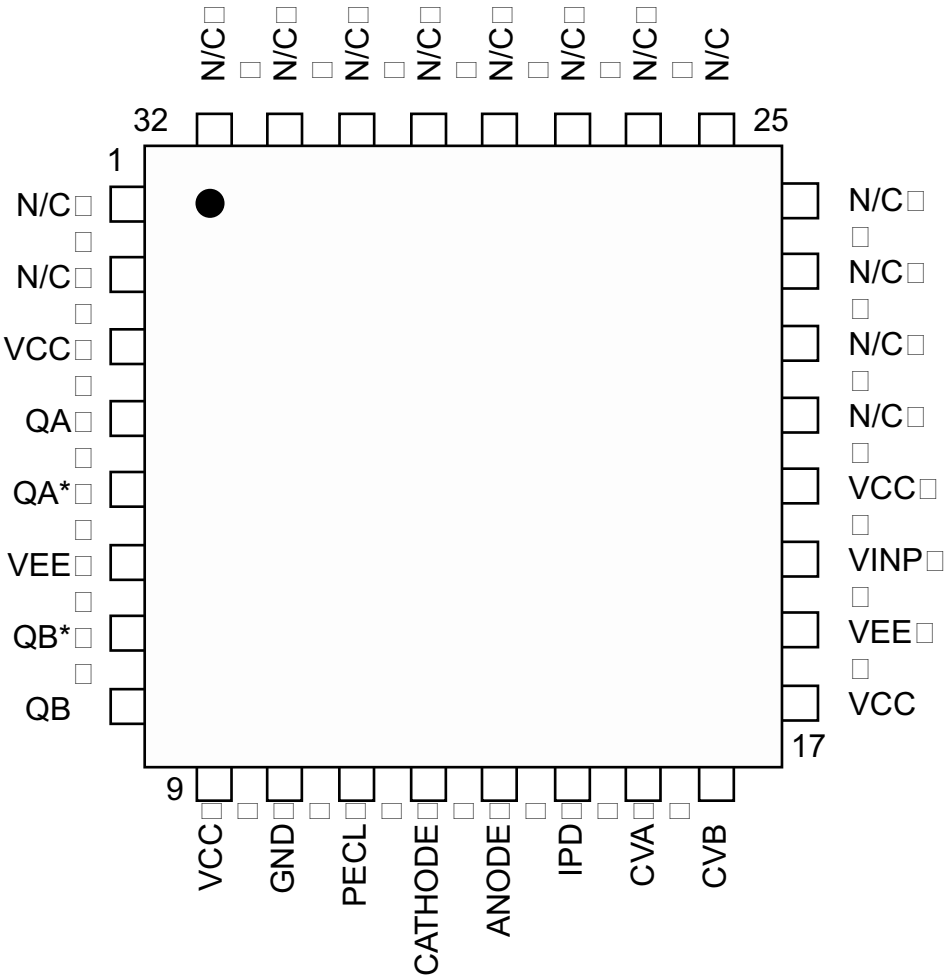
Functional Block Diagram



PIN Description

Pin Name	Pin #	Description
Comparator		
19	VINP	Analog voltage input for the window comparator. The VINP connects to both of the non-inverting (+) inputs of the comparators.
4, 5 8, 7	QA / QA* QB / QB*	Differential output pins from the window comparator.
15, 16	CVA, CVB	Analog input pins used to set the high and low levels for the window comparator.
14	IPD	TTL compatible input which activates the input power down mode of the window comparator.
Power		
6, 18	VEE	Negative power supply.
VCC	3, 9, 17, 20	Positive power supply.
GND	10	Device ground.
PECL	11	Analog power supply which sets the comparator output levels.
Test Pins		
12 13	CATHODE ANODE	Cathode and anode ends of a series string of diodes used to monitor the die temperature.

PIN Description *(continued)*



Window Comparator

Introduction

The Edge670 has two comparators connected on-chip as a window comparator to determine whether the DUT is in a high, low, or indeterminate state.

Power Supply Sequencing

The following sequence should be used when powering up the Edge670.

1. VEE
2. VCC
3. Analog Inputs (VINP, CVA, CVB)

Functionality

The VINP pin is tied to the positive inputs of both comparators (see Figure 1).

Input Condition	Output Condition
VINP > CVA	QA = High; QA* = Low
VINP < CVA	QA = Low; QA* = High
VINP > CVB	QB = High; QB* = Low
VINP < CVB	QB = Low; QB* = High

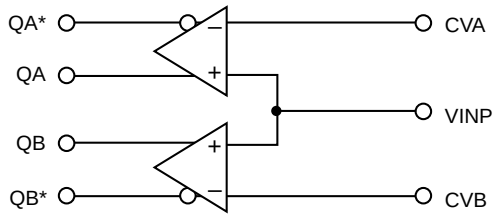


Figure 1. Comparator Functionality

Thresholds

CVA and CVB are the two comparator threshold levels. These inputs are high impedance voltage controlled inputs that determine at which VINP input voltage the comparator will change states.

Hysteresis

Hysteresis is a measure of the change in threshold voltage as a function of the comparator output state (see Figure 2). Typically, hysteresis is used to prevent multiple comparator output transitions due to slow input slew rates in a noisy environment. These slower inputs remain in the transition region for longer periods of time, allowing any noise present to cause repeated threshold crossings.

The Edge670 is designed with 4 mV of hysteresis. This hysteresis is non-adjustable and requires no external support. The amount of hysteresis was chosen to allow stable and reliable transitions in most system environments, without noticeably affecting the comparator performance.

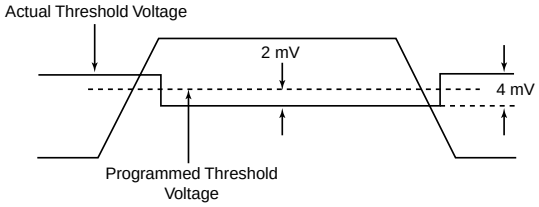


Figure 2. Hysteresis

The effects of hysteresis are visible in two categories - offset voltage and propagation delay. The amount of hysteresis must be large enough to overcome the system noise floor, yet small enough not to increase offset voltage effects significantly.

Input Protection

The VINP pin has an internal 50Ω series resistor and two over-voltage diodes capable of shunting up to 100 mA (see Figure 3) and, therefore, requires no external protection circuitry. The over-voltage input range that the comparator can withstand is determined by the power supply rails and the following equations:

$$VEE - .7 - (100\ mA * 50\Omega) < VINP < VCC + .7 + (100\ mA * 50\Omega)$$

or

$$VEE - 5.7V < VINP < VCC + 5.7V.$$

Circuit Description *(continued)*

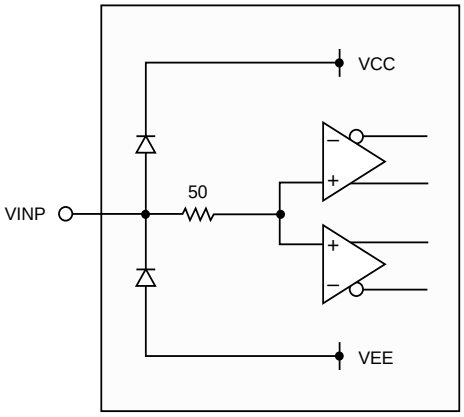


Figure 3. Input Protection

For a wider protected input range, an additional external series resistor may be added.

Comparator PECL Output Capability

PECL is a variable analog voltage power supply that determines the common mode voltage of the comparator digital outputs. With PECL connected to ground, the Edge670 generates standard differential ECL outputs. However, the outputs will track the PECL input, and remaining one diode drop below it as PECL is varied between ground and +5V. By setting PECL appropriately, a fully differential comparator output may interface directly to a CMOS ASIC without any translators.

Input Power Down

The Edge670 comparator has a mechanism where it can drastically reduce the input bias current flowing into the VINP pin, while still maintaining a functional comparator. In this mode, however, the comparator slows down significantly and can no longer track fast edges, in particular, fast falling edges.

The IPD pin is a TTL compatible input which controls the two modes. With IPD = low, the comparator is in its normal high speed mode, supporting maximum AC performance.

With IPD = high, the comparator is in Power Down Mode. The input bias current decreases to < 100 nA. The comparator still functions, but can track edges only up to 25 mV/ns.

Thermal Monitor

The Edge670 includes an on-chip thermal monitor accessible through the CATHODE and ANODE. These nodes connect to five diodes in series (see Figure 4) and may be used to accurately measure the junction temperature at any time.

An external bias current of 100 µA is injected through the string, and the measured voltage corresponds to a specific junction temperature with the following equation:

$$Tj[°C] = \{(ANODE - CATHODE)/5 - .7\} / (-.00208).$$

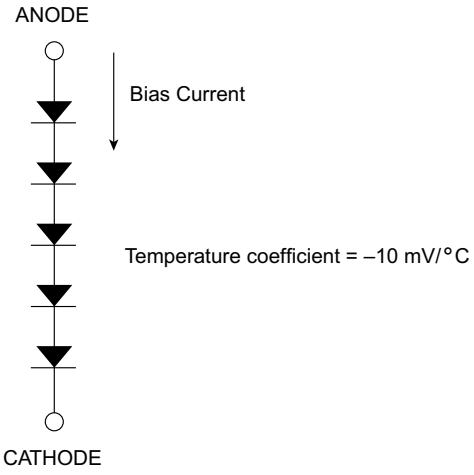


Figure 4. Thermal Diode String

Circuit Description *(continued)*

Delay Dispersion

Given a constant temperature and voltage environment (within the bounds of the recommended operating conditions), the propagation delay dispersion (TSD) indicates how much variation in propagation delay time can be expected for one comparator over a wide range of input conditions. Thus, the propagation delay of a comparator can be described as:

$$Tpd \pm TSD$$

where TPD is the nominal delay that will vary with temperature and voltage, and part to part. In many ATE applications, Tpd is calibrated or compensated for on a channel-by-channel basis. TSD includes factors that normally may be difficult to calibrate, and therefore directly impact overall system timing accuracy.

Propagation delay dispersion is defined as the maximum deviation of the propagation delay taken at the eight measurement points (see Figure 10) for 1V and 3V input signals described below. The parameters of interest are:

- Slew rate
- Edge direction
- Overdrive
- Common mode voltage.

Low dispersion numbers indicate the accuracy of a system under a variety of input conditions, and are an important figure of merit for any comparator.

While not production tested, the Edg670 is designed specifically to exhibit low dispersion. The typical Edge670 will show less than 25 ps Tpd dispersion.

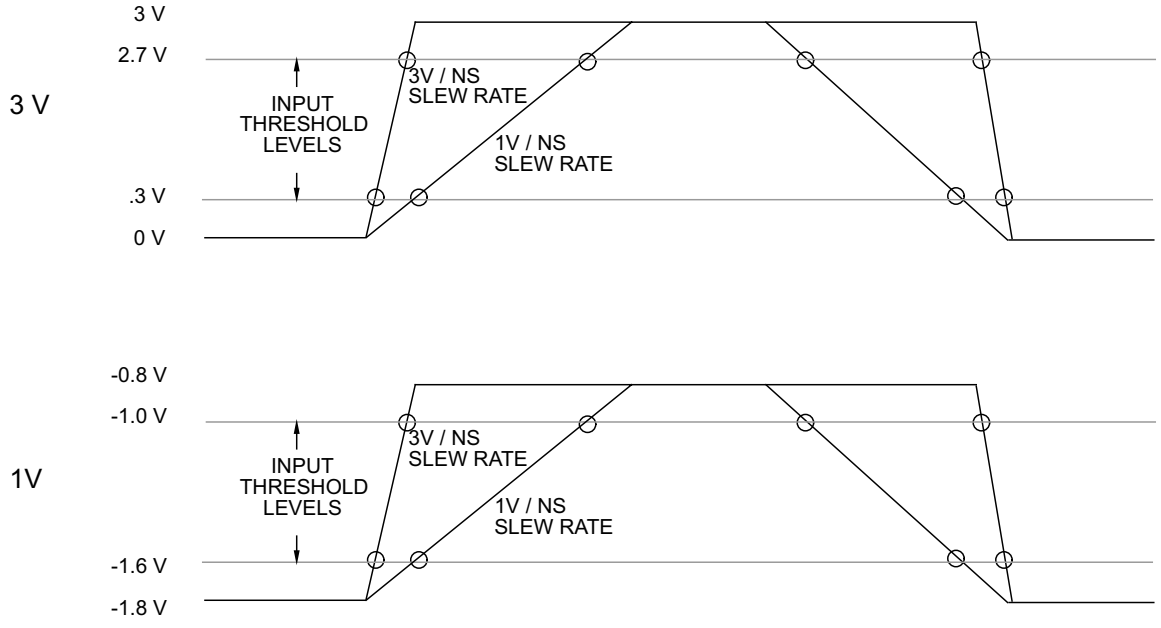
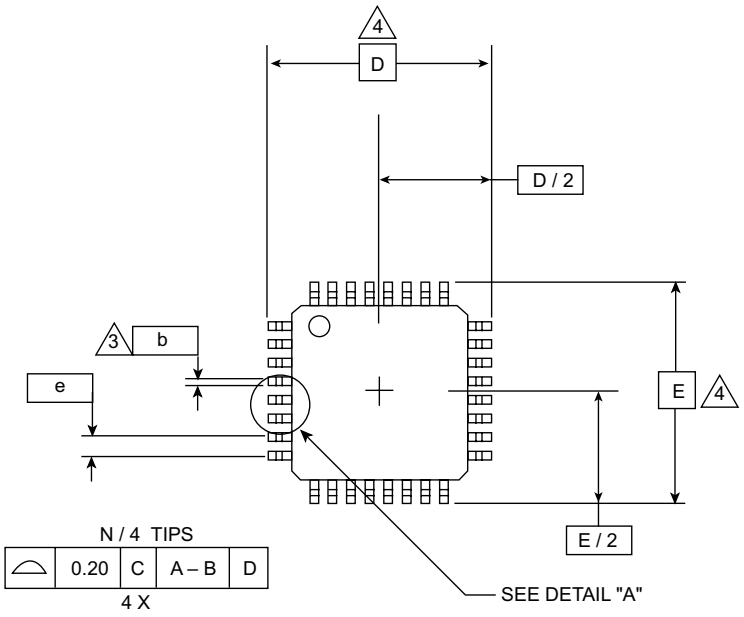


Figure 10. Dispersion Measurement Conditions

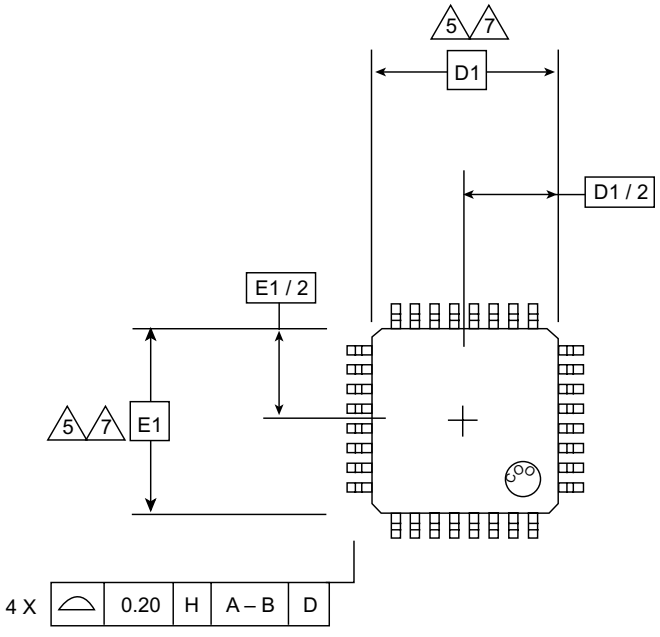
Package Information

32-Pin TQFP
7mm x 7 mm

TOP VIEW

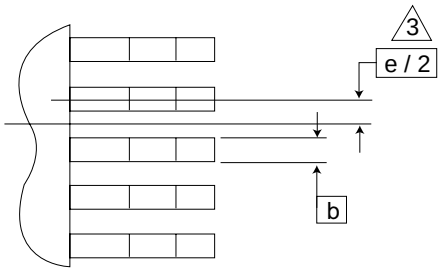


BOTTOM VIEW

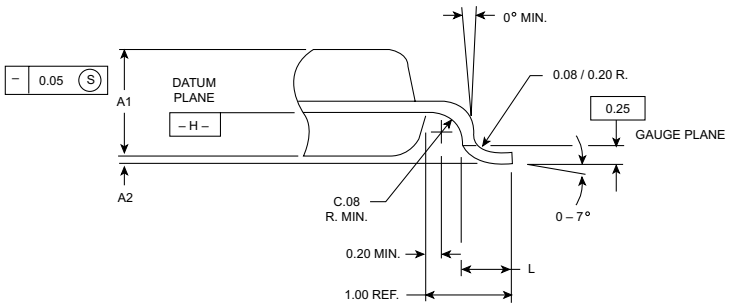


Package Information *(continued)*

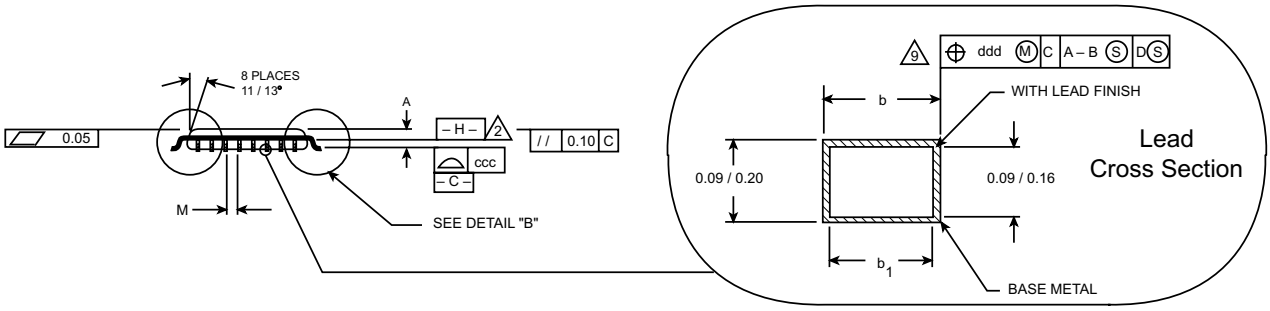
DETAIL "A"



DETAIL "B"



SECTION C–C



Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at centerline between leads where leads exit plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion.
6. "N" is the total # of terminals.
7. These dimensions to be determined at the datum plane -H-.
8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.30 millimeters.
12. This outline conforms to JEDEC publication 95, registration MO-136, variations AC, AE, and AF.

JEDEC VARIATION

AC				
Sym	**Min**	**Nom**	**Max**	**Note**
A			1.60	
A1	0.05	0.10	0.15	
A2	1.35	1.40	1.45	
D		9.00 BSC		4
D1		7.00 BSC		7, 8
E		9.00 BSC		4
E1		7.00 BSC		7, 8
L	0.45	0.60	0.75	
M	0.15			
N		32		
e		0.80 BSC		
b	0.30	0.37	0.45	9
b1	0.30	0.35	0.40	
ccc			0.10	
ddd			0.20	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC	8.5	11.5	12.0	V
Negative Power Supply	VEE	-8.5	-5.2	-4.5	V
Total Analog Supply	VCC - VEE	13.0	16.7	17.0	V
Comparator Output Positive Supply	PECL	0	3.3	5.0	V

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Positive Supply (Relative to GND)	VCC	0		+13.0	V
Negative Supply (Relative to GND)	VEE	-9.0		0	V
Total Power Supply	VCC - VEE			+20.0	V
Comparator Output Positive Supply	PECL	0		+6.0	V
Digital Output Currents	QA, QA*, QB, QB*	0		50	mA
Comparator Input to Threshold	VINP - CVA VINP - CVB	-13 -13		+13 +13	V V
Analog Voltages	CVA, CVB	VEE		VCC	V
Ambient Operating Temperature	TA	-55		+145	ºC
Storage Temperature	TS	-65		+150	ºC
Junction Temperature	TJ			+150	ºC
Process Temperature (<30 hours)				+160	ºC

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Threshold Voltage	CVA, CVB	VEE + 2.9		VCC - 2.9	V
Input Voltage Range	VINP	VEE + 2.9		VCC - 2.9	V
Input Differential Voltage	VINP - CVA, B	-11		+11	V
Threshold Input Current		-50		+50	µA
IPD Pin Input Current		-150		+10	µA
VINP Input Current (Note 1) Normal Operation IPD = 0 IPD Mode IPD = 1	 IBIAS IBIAS	 -1 -250		 +1 +250	 µA nA
Offset Voltage	VOS	-50		+50	mV
Common Mode Rejection Ratio	CMRR		60		dB
Power Supply Rejection Ratio	PSRR		60		dB
Comparator Hysteresis			4		mV
Digital Output Swing	|QA - QA*| |QB - QB*|	600 600	700 700	1,000 1,000	mV mV
Power Supply					
Positive Supply Current	ICC	30	44	60	mA
Negative Supply Current	IEE	40	60	80	mA
PECL Supply Current (Note 2)	IDD	55	16	95	mA

DC test conditions (unless otherwise specified): "Recommended Operating Conditions".

Note 1: Tested at +7V and –1V.
Note 2: Assumes no digital output current

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay (Notes 1, 2)	Tpd	1.0	2.0	4.0	ns
Propagation Delay Dispersion (Note 2)					
800 mV		-100	<±25	+100	ps
3V		-100	<±25	+100	ps
5V		-100	<±25	+100	ps
Input Slew Rate Tracking (Note 2)					
IPD = 0		5.0	6.0		V/ns
IPD = 1		25			mV/ns
Input Capacitance	Cin		1.5		pF
Output Rise and Fall Times (20% to 80%)	Tr, Tf		250		ps
Minimum Pulse Width (Note 2)				1.5	ns

DC test conditions (unless otherwise specified): "Recommended Operating Conditions".

Note 1: Assumes normal operating mode of IPD = 0.
Note 2: Guaranteed by characterization. This parameter is not production tested

Ordering Information

Model Number	Package
E670CTF	32 pin 7 mm x 7 mm TQFP (670 Die (Comparator Only))
EVM670CTF	Edge670 Evaluation Board

Contact Information

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Revision History

Current Revision: July 20, 2001
Previous Revision: March 5, 2001

Page #	Section Name	Previous Revision	Current Revision
4	Circuit Description		*Add:* Power Supply Sequencing Section

Current Revision: March 5, 2001
Previous Revision: August 12, 2000

Page #	Section Name	Previous Revision	Current Revision
5	Circuit Description		Update Figure 3