

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA
BD805*
BD807
BD809
**PLASTIC HIGH POWER
SILICON NPN TRANSISTOR**

... designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current— $h_{FE} = 30$ (Min) @ $I_C = 2.0$ Adc
- BD 805, 807, 809 are complementary with BD 806, 808, 810

**10 AMPERE
POWER TRANSISTOR**
NPN SILICON
**45, 60, 80 VOLTS
90 WATTS**
MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD805 BD807 BD809	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD805 BD807 BD809	55 70 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	°C

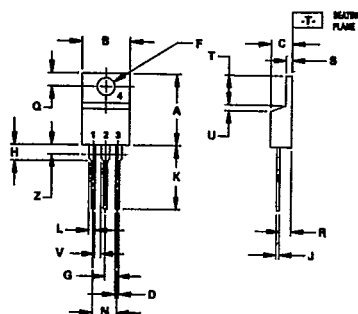
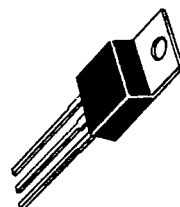
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.2$ Adc, $I_B = 0$)	BV_{CEO}	BD805 BD807 BD809	45 60 80	—	Vdc
Collector Cutoff Current ($V_{CB} = 55$ Vdc, $I_E = 0$) ($V_{CB} = 70$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD805 BD807 BD809	—	1.0 1.0 1.0	mA
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	2.0	mA
DC current Gain ($I_C = 2$ A, $V_{CE} = 2$ V) ($I_C = 4$ A, $V_{CE} = 2$ V)	h_{FE}		30 15	—	
Collector-Emitter Saturation Voltage* ($I_C = 4$ Adc, $I_B = 0.4$ Adc)	$V_{CE(sat)}$		—	1.1	Vdc
Base-Emitter On Voltage* ($I_C = 4$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	1.6	Vdc
Current Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		15	—	MHz

* Pulse Test. Pulse Width ≤ 100 μ s. Duty Cycle $\leq 20\%$.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION, INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.68	10.28	0.380	0.405
C	4.97	4.82	0.190	0.190
D	0.54	0.88	0.025	0.035
F	3.81	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.80	0.110	0.150
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.38	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

CASE 221A-04
TO-220AB

FIGURE 1 — ACTIVE REGION DC
SAFE OPERATING AREA

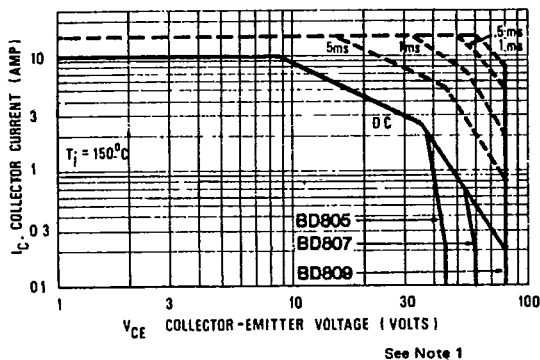


FIGURE 2 — POWER-TEMPERATURE
DERATING CURVE

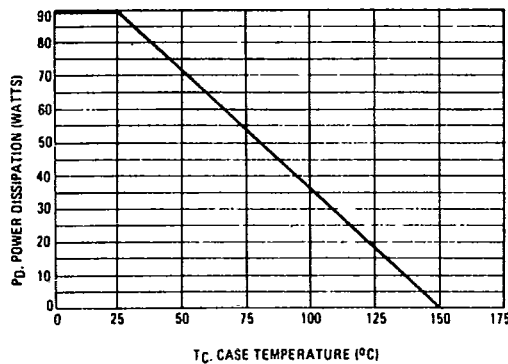


FIGURE 3 — "ON" VOLTAGES

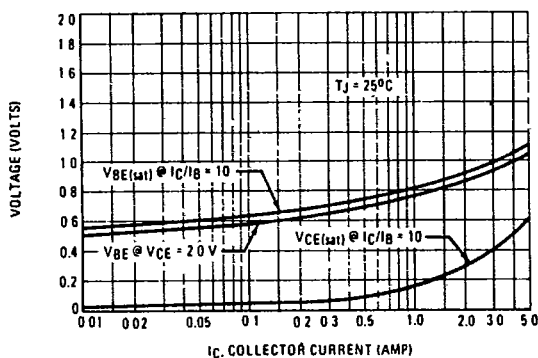


FIGURE 4 — CURRENT GAIN

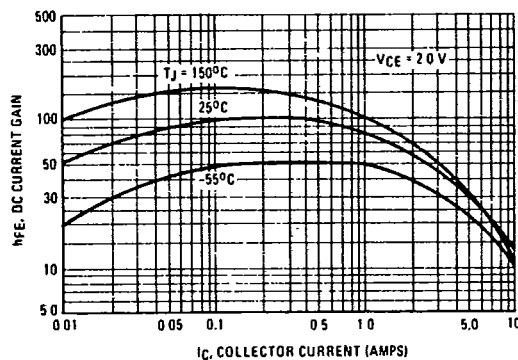
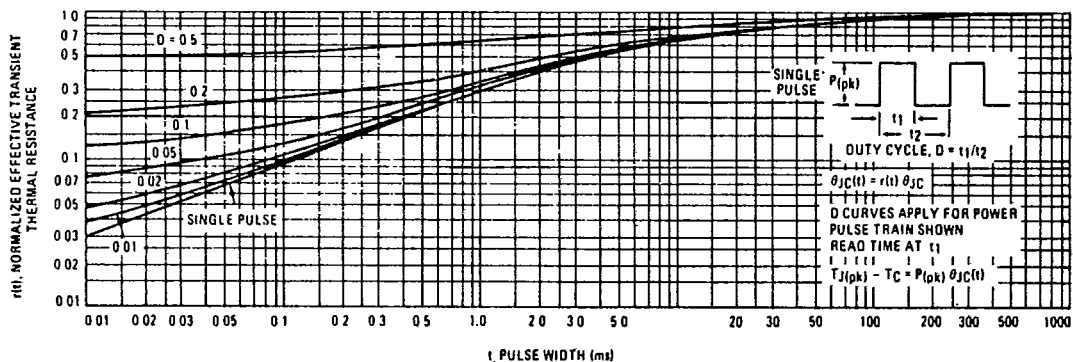


FIGURE 5 — THERMAL RESPONSE



Note 1:

There are two limitations on the power handling ability of a transistor, average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_J(pk) = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)