Am27HB010

1 Megabit (131,072 x 8-Bit) Burst Mode CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High speed**
  - 50 ns random access
  - 15 ns burst access
- **No burst boundary**
- **No burst limit**
- **Pin compatible with Am27C010**
- **Supports all "Burst" microprocessors**
  - Am29000 compatible
- **Single + 5 V power supply**
- **± 10% power supply tolerance available**
- **High speed Flashrite™ programming**
  - Typically less than 30 seconds

GENERAL DESCRIPTION

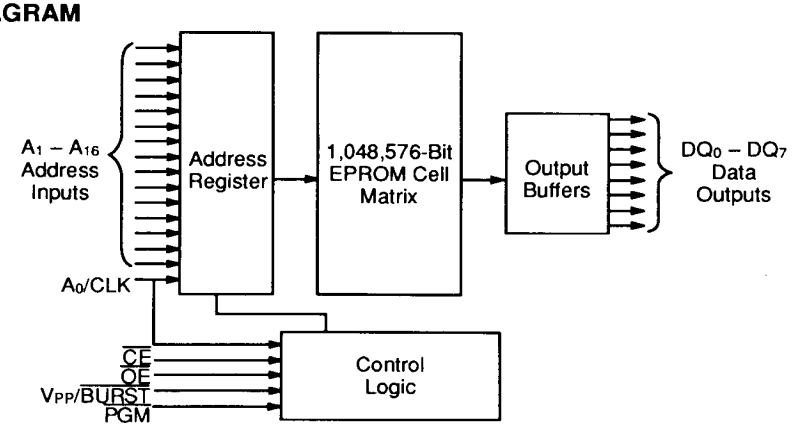
The Am27HB010 is a 1 megabit ultraviolet erasable programmable read-only memory. It is organized as 128K words by 8 bits per word. Two modes are available to access the data. Random access mode is selected by placing V_{IH} on the $V_{PP}/\overline{BURST}$ pin and this allows full random access to the data. Burst access is selected by placing V_{IL} on the $V_{PP}/\overline{BURST}$ pin which allows high speed access to sequential data. Burst mode may be entered without regard to page or word boundaries and may be sustained all the way up to the physical device boundary (128K bytes) if required.

The Am27HB010 is ideal for use with the fastest processors due to the high speed random access time. This device also achieves maximum performance with all of today's "burstable" processors due to the extremely fast burst mode access time. Designers may take full advantage of high speed digital signal processors and microprocessors by allowing code to be executed at full speed directly out of EPROM.

The Am27HB010 is programmed using AMD's Flashrite™ programming algorithm which allows the entire chip to be programmed typically in less than 30 seconds.

This device is available in 32-pin windowed DIP as well as surface mount packages and is offered in commercial, industrial and extended temperature ranges.

BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

Family Part No.	Am27HB010			
Vcc ±10%	-50	-55	-70	90
Max Access Time (ns)	50	55	70	90
Burst Access (ns)	15	15	20	30
$\overline{CE}$ ($\overline{E}$) Access (ns)	50	55	70	90
$\overline{OE}$ ($\overline{G}$) Access (ns)	15	15	20	30

Publication # 14970 Rev. C Amendment /0
Issue Date: January 1992

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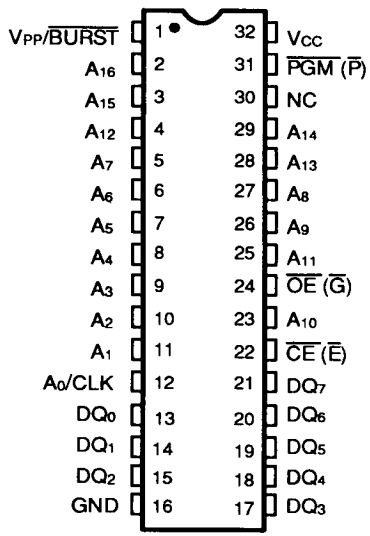
CONNECTION DIAGRAMS
Top View

DIP



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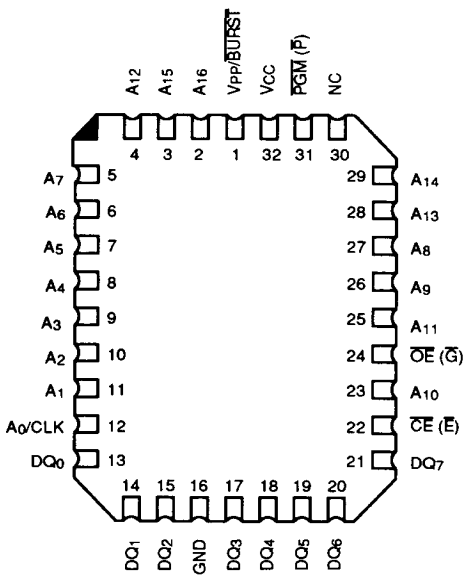
LCC*



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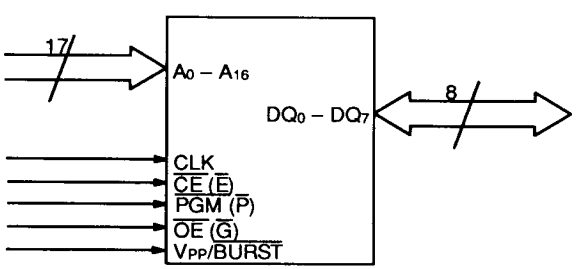
Note:
JEDEC nomenclature is in parenthesis

*Also available in a 32-pin PLCC.

PIN DESCRIPTION

A_0–A_{16}	Address Inputs
$\overline{CE}$ ($\overline{E}$)	Chip Enable Input
DQ_0–DQ_7	Data Input/Outputs
$\overline{OE}$ ($\overline{G}$)	Output Enable Input
CLK	Clock
$\overline{PGM}$ ($\overline{P}$)	Program Enable Input
V_{CC}	V_{CC} Supply Voltage
$V_{PP}/\overline{BURST}$	Program Supply Voltage & Burst Enable
GND	Ground
NC	No Internal Connection

LOGIC SYMBOL



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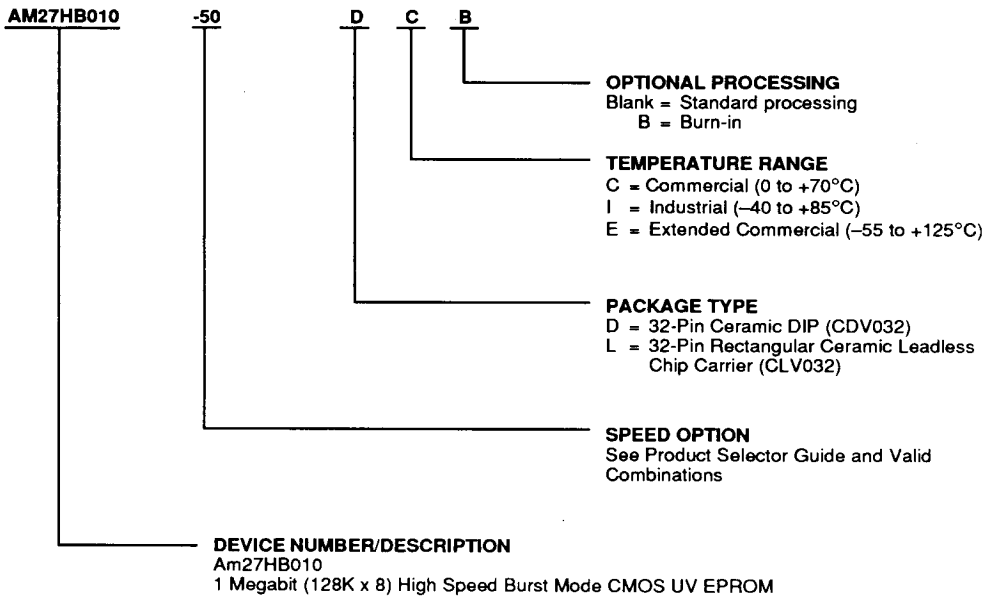
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27HB010-50	DC, DCB, LC, LCB
AM27HB010-55	
AM27HB010-70	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27HB010-90	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

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ORDERING INFORMATION
OTP Products (Preliminary)

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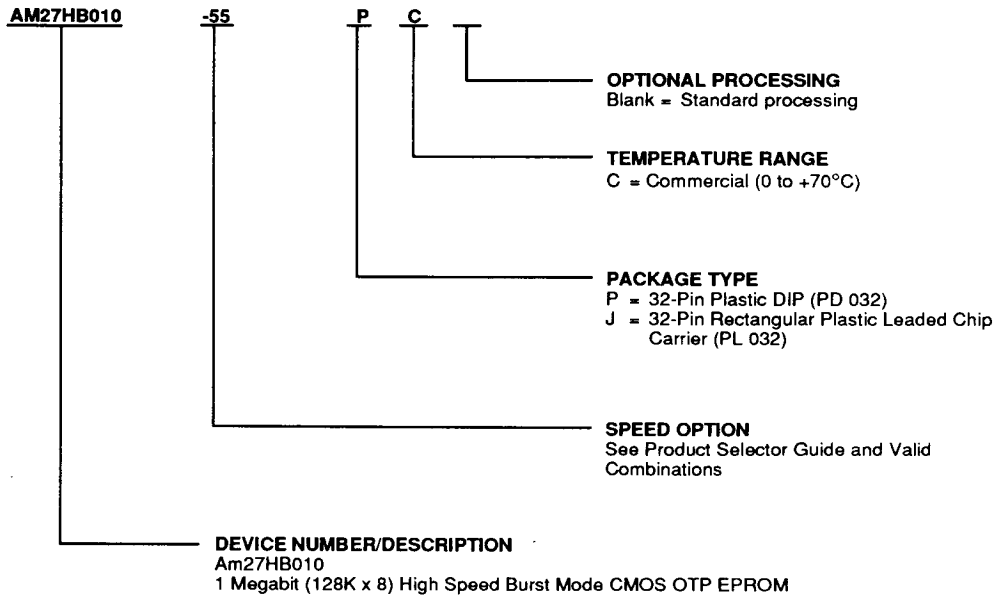

Valid Combinations	
AM27HB010-55	PC, JC
AM27HB010-70	
AM27HB010-90	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

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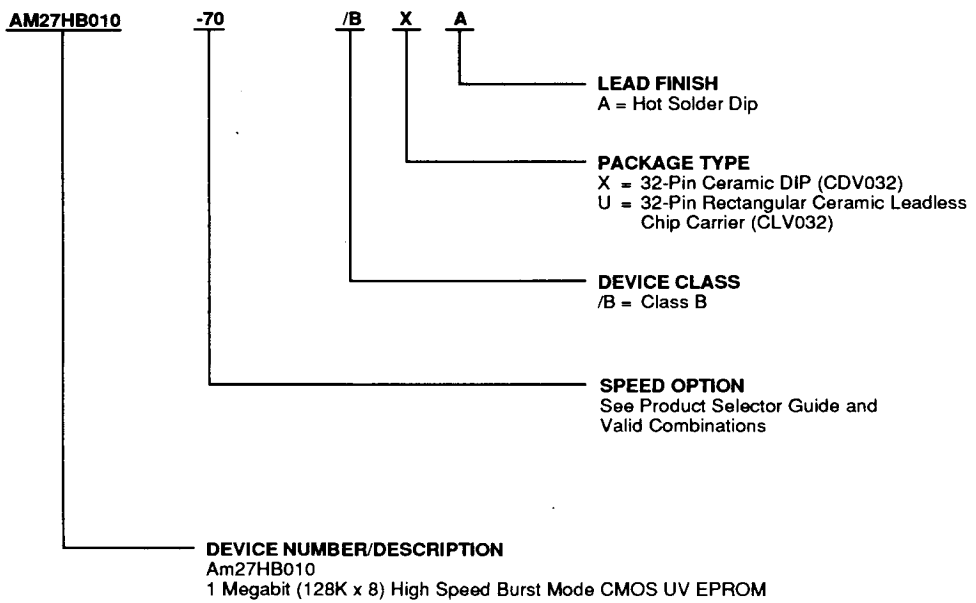
ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27HB010-70	/BXA, /BUA
AM27HB010-90	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

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FUNCTIONAL DESCRIPTION

Erasing the Am27HB010

In order to clear all locations of their programmed contents, it is necessary to expose the Am27HB010 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27HB010. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The Am27HB010 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27HB010, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27HB010 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27HB010

Upon delivery, or after each erasure, the Am27HB010 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27HB010 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, and $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}, and $\overline{OE}$ is at V_{IH}. For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm reduces programming time by using initial 100 μs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.25 V.

Program Inhibit

Programming of multiple Am27HB010s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27HB010 may be common. A TTL low-level program pulse applied to an Am27HB010 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, $\overline{PGM}$ is LOW, and $\overline{OE}$ HIGH will program that Am27HB010. A high-level $\overline{CE}$ input inhibits the other Am27HB010 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V to 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27HB010.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27HB010. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code, and byte 1 (A_0 = V_{IH}), the device identifier code. For the Am27HB010, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Random Read Mode

The Am27HB010 has three control functions that must be logically satisfied in order to obtain random access data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. V_{PP}/$\overline{BURST}$ must be at V_{IH}. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Initial Burst Access

The Am27HB010 will enter the burst-mode when both V_{PP}/$\overline{BURST}$ and $\overline{CE}$ are at logic '0'. The last pin to switch from V_{IH} to V_{IL} (either V_{PP}/$\overline{BURST}$ or $\overline{CE}$), will determine the exact entry into the burst-mode. At this time the addresses (A_0–A_{16}) are latched internally to the device for the remainder of the burst access. There are no boundary address conditions for entering the burst-mode. The access time for the initial access is measured from when the addresses ($A_1 - A_{16}$) are stable. The delay in A_0 will have no effect on access speed as long as the conditions listed in Switching Characteristics are met.

Burst Read Mode

After the initial access, sequential bytes of data may be accessed by toggling the A_0/CLK signal. Data will be available in the specified burst access time. There are no minimum or maximum amounts of data required for a burst. The device will perform a one byte burst or continue to the physical end of the device, 128K if required.

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The device will also wrap around and go to the very beginning of the memory once the physical boundary of the device is reached. To exit burst mode, $V_{PP}/\overline{BURST}$ is toggled from V_{IL} to V_{IH}.

Burst Suspend Mode

Burst mode may be suspended by removing CE while V_{PP}/BURST is still at V_{IL}. To resume burst mode, V_{PP}/BURST remains at V_{IL} while CE is re-asserted. Data will then be available within the burst access time.

It should be noted that A_0 has to be low while going into Burst Suspend Mode.

Standby Mode

The Am27HB010 has a TTL standby mode which reduces the maximum V_{CC} current to 20% of the active current. It is placed in standby mode when $\overline{CE}$ and $V_{PP}/\overline{BURST}$ is at V_{IH}. The amount of current drawn in standby mode depends on the frequency and the number of address pins switching. The Am27HB010 is specified with 50% of the address lines toggling at 10 MHz. A reduction of the frequency or quantity of address lines toggling will significantly reduce the actual standby current. The V_{CC} DC current can further be decreased to 1 mA by placing all inputs at steady CMOS logic levels.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0/CLK	A_9	$V_{PP}/\overline{BURST}$	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{IH}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	Hi-Z
Standby		V_{IH}	X	X	X	X	V_{IH}	Hi-Z
BURST Enable		V_{IL}	V_{IL}	X	X	X	V_{IL}	D_{OUT}
BURST Suspend (Note 7)		V_{IH}	V_{IH}	X	X	X	V_{IL}	Hi-Z
BURST Suspend (Note 7)		V_{IH}	V_{IL}	X	X	X	V_{IL}	D_{OUT}
BURST Read		V_{IL}	V_{IL}	X	L-H	X	V_{IL}	D_{OUT}
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto Select (Notes 3 & 5)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{IH}	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{IH}	0EH

Notes:

1. $V_H = 12.0\ V \pm 0.5\ V$
2. X = Either V_{IL} or V_{IH} (cannot exceed $V_{CC} + 0.5\ V$)
3. $A_1 - A_8 = A_{10} - A_{16} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.
5. The Am27HB010 uses the same Flashrite algorithm during program as the Am27C010.
6. $V_{IL} < 0.8\ V$; $V_{IH} > 2.0\ V$
7. BURST suspend is entered only when $\overline{CE}$ toggles from V_{IL} to V_{IH} during Burst Mode operation.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP product	–65 to +125°C
All other products	–65 to +150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	–0.6 to V_{CC} +0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. This is a stress rating only; functional operation of the device at these limits or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum ratings for extended periods may affect device reliability.

Notes:

1. During transitions, the input may overshoot GND to –2.0 V for periods of up to 10 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods of up to 10 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 10 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (T_C)	–55 to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55 to +125°C
Supply Read Voltages:	
V_{CC} for Am27HB010-XX	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

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DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 4, 5 & 8) (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA (C Devices) I_{OL} = 10 mA (I Devices) I_{OL} = 8 mA (E/M Devices)			0.45	V
V_{IH}	Input HIGH Voltage (Note 9)			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage (Note 9)			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 0.5 V		1.0		µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to + V_{CC}			10	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		100	mA
			E/M Devices		120	
I_{CC2}	Vcc Standby Current (TTL)	$\overline{CE}$ = V_{IH}, $V_{PP}/\overline{BURST}$ = V_{IH}	C/I Devices		25	mA
			E/M Devices		35	
I_{CC3}	Vcc Standby Current (CMOS)	$\overline{CE}$ = V_{CC} – 0.3 V to V_{CC} + 0.5 V $V_{PP}/\overline{BURST}$ = V_{CC} – 0.3 V to V_{CC} + 0.5 V			1.0	mA
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	PL 032		CDV032		CLV032		Unit
			Typ.	Max.	Typ.	Max.	Typ.	Max.	
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	6	12	6	12	6	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{IN} = 0 V	12	20	12	20	12	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	15	10	15	8	15	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled, not 100% tested.
4. **Caution**: The Am27HB010 must not be removed from (or inserted into) a socket when V_{PP} or V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP1}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the inputs may overshoot to –2.0 V for periods less than 10 ns.
   Maximum DC voltage on output pins may overshoot to V_{CC} + 2.0 V for periods less than 10 ns.
9. Tested under static DC conditions.

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SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27HB010				Unit
JEDEC	Standard				-50	-55	-70	-90	
t_{AVQV}	t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$, $C_L = C_{L1}$		50	55	70	90	ns
	t_{BACC}	Burst Access Time	$\overline{CE} = \overline{OE} = V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$		15	15	20	30	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$, $C_L = C_{L1}$		50	55	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$, $C_L = C_{L1}$		15	15	20	30	ns
t_{GHQZ}	t_{DF} (Note 2)	Output Enable to Output Float	$\overline{CE} = V_{IL}$, $C_L = C_{L2}$		10	10	15	25	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurs first		Min.	0	0	0	0	ns
				Max.	–	–	–	–	
	t_{SET}	Address Setup to BURST or $\overline{CE}$ Enable	$\overline{CE} = V_{IL}$, $C_L = C_{L1}$		10	10	15	25	ns
	t_{HOLD1}	Address A_0 Hold to BURST or $\overline{CE}$ Enable	$\overline{CE} = V_{IL}$, $C_L = C_{L1}$		0	0	0	0	ns
	t_{HOLD2}	Addresses A_1–A_{16} Hold to $\overline{BURST}$ or $\overline{CE}$ Enable	$\overline{CE} = \overline{OE} = V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$		7	7	7	7	ns
	$t_{BCLKLOW}$	Minimum Low Time for for A_0 to Start BURST	$\overline{CE} = \overline{OE} = V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$		10	10	15	25	ns
	t_{BSUSPS}	BURST Suspend Setup Time	$V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$		10	10	15	25	ns
	t_{BSUSPH}	BURST Suspend Hold Time	$V_{PP}/\overline{BURST} = V_{IL}$ $C_L = C_{L1}$		10	10	15	25	ns
	t_{BRES}	BURST Resume Setup Time	$V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$		10	10	15	25	ns
	$t_{BTERMCLK}$	BURST Terminate Setup to A_0/CLOCK Time	$V_{PP}/\overline{BURST} = V_{IH}$, $C_L = C_{L1}$		10	10	15	25	ns
	t_{BCLK}	Minimum CLOCK HIGH Time (Note 7)	$\overline{CE} = \overline{OE} = V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$		6	6	8	13	ns
	t_{BCLKB}	Minimum CLOCK LOW Time (Note 7)	$\overline{CE} = \overline{OE} = V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$		6	6	8	13	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution**: The Am27HB010 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and $C = C_L$
   Input Rise and Fall Times: 3 ns for -50; 5 ns for -60; 7 ns for -90
   Input Pulse Levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs
5. Transient Input Low Voltages to –2.0 V with 10 ns duration at the 50% amplitude point are permitted.
6. To guarantee Initial Burst Access, $t_{SET} + t_{BCLKLOW} + t_{HOLD} \geq t_{ACC}$.
7. Burst clocks should have 50% duty cycle. Clock skews are allowed as long as minimum t_{BCLK} and t_{BCLKB} specifications are met and $t_{BACC} = t_{BCLK} + t_{BCLKB}$.

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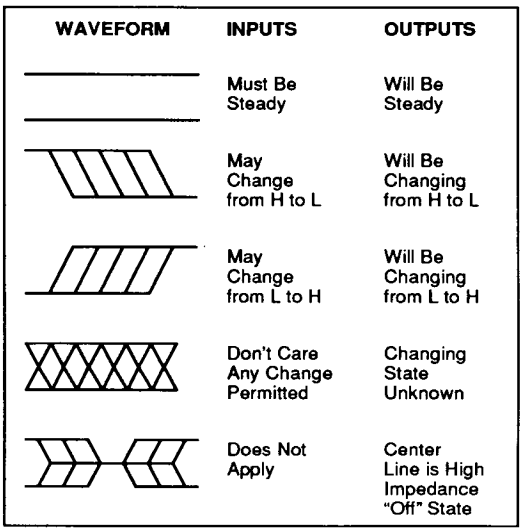
KEY TO SWITCHING WAVEFORMS



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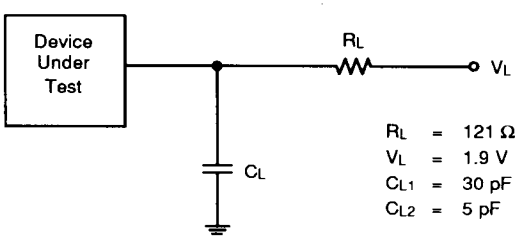
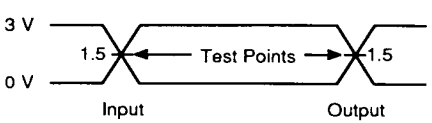
SWITCHING TEST CIRCUIT



14970-005B

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 for a logic "0". Input pulse rise and fall times are < 3 ns for –50; < 5 ns for –60; and < 7 for –90.

14970-006B

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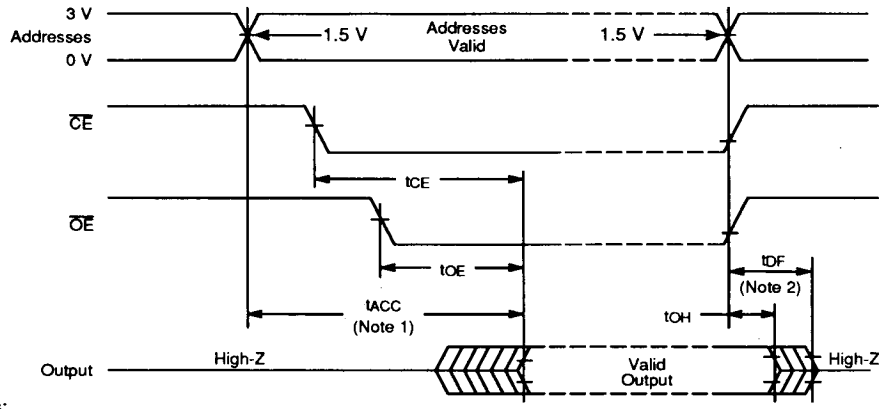
SWITCHING WAVEFORMS (Read Timings—Random Access Mode)

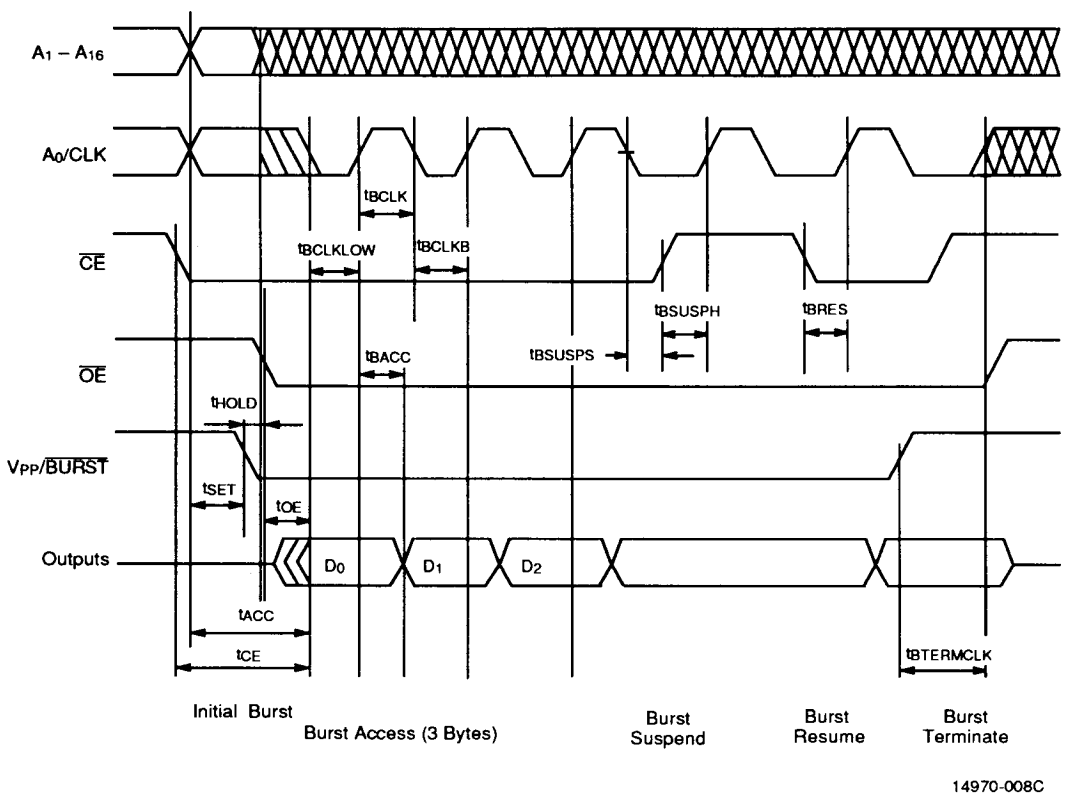


Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

14970-007B

SWITCHING WAVEFORMS (Burst Mode)



14970-008C

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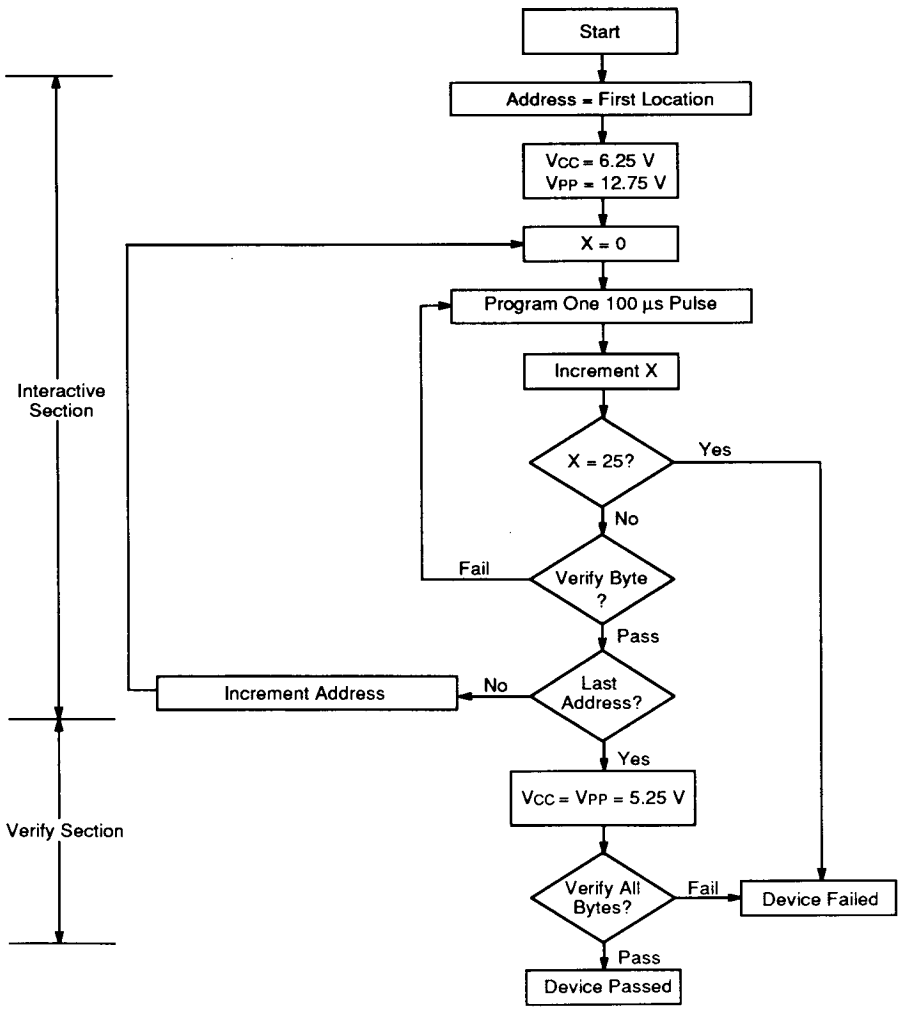
PROGRAMMING FLOW CHART



14970-009B

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DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 12 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –4 mA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC3}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
V_{CC1}	Supply Voltage		6.00	6.50	V
V_{PP}	Programming Voltage		12.5	13.0	V

SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		75	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27HB010, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

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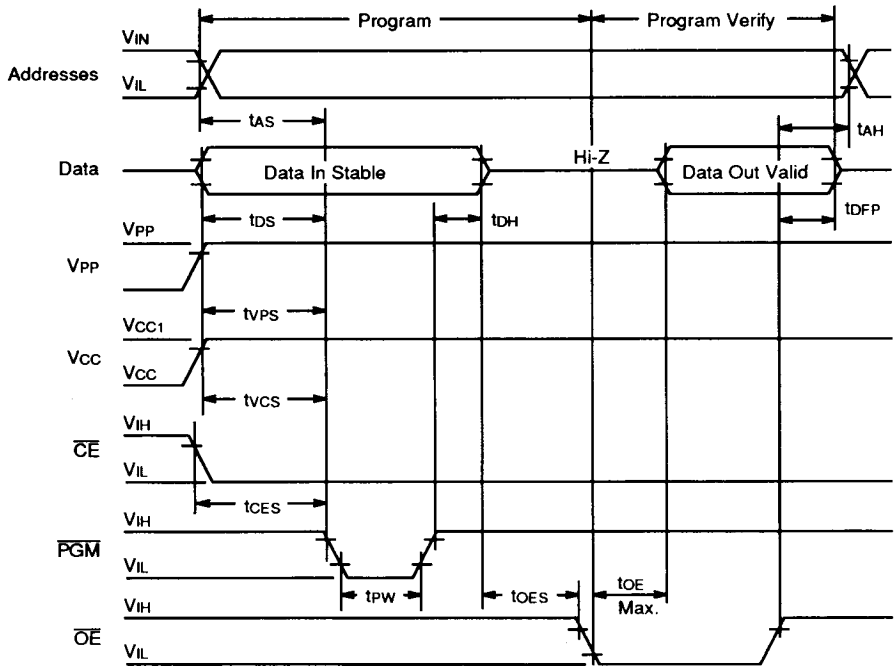
PROGRAMMING ALGORITHM WAVEFORM (Notes 1 & 2)



14970-010B

Notes:

1. The input timing reference level is 0.8 for a V_{IL} and 2 V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

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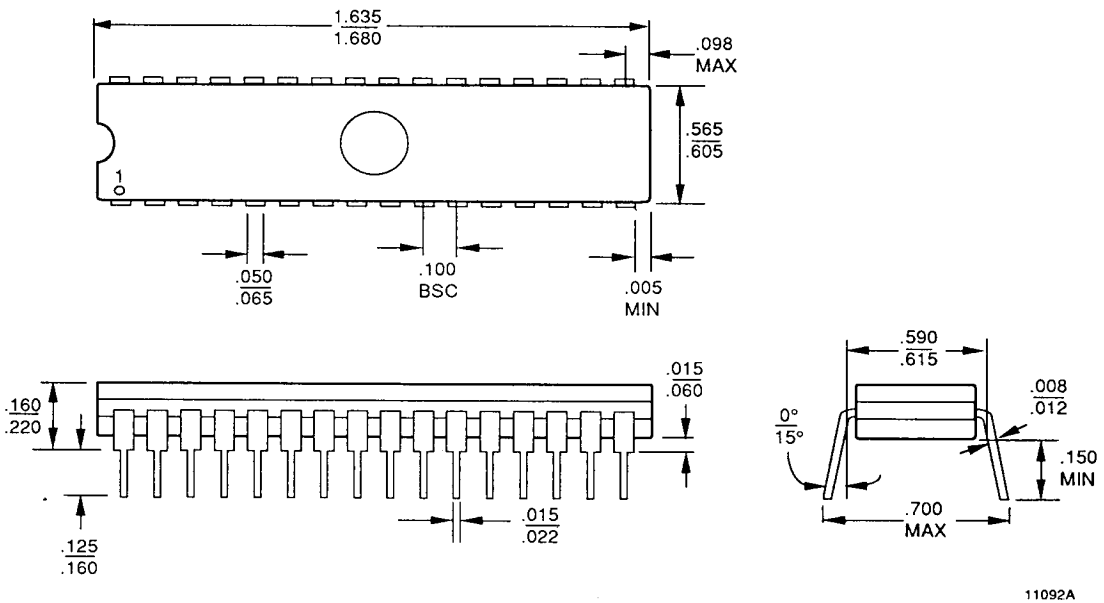
PHYSICAL DIMENSIONS
CDV 032
Ceramic Dip with View



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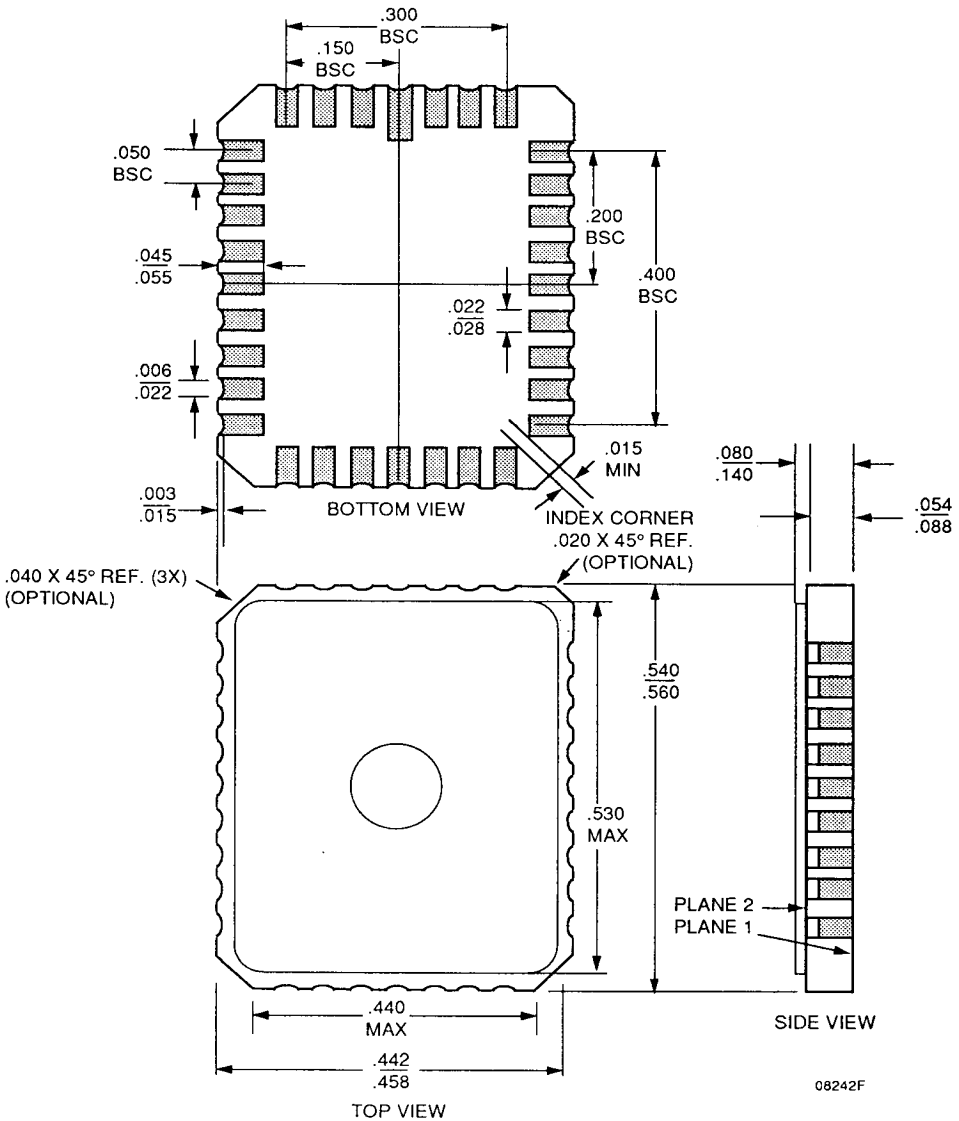
CLV 032
Ceramic Leadless Chip Carrier with View



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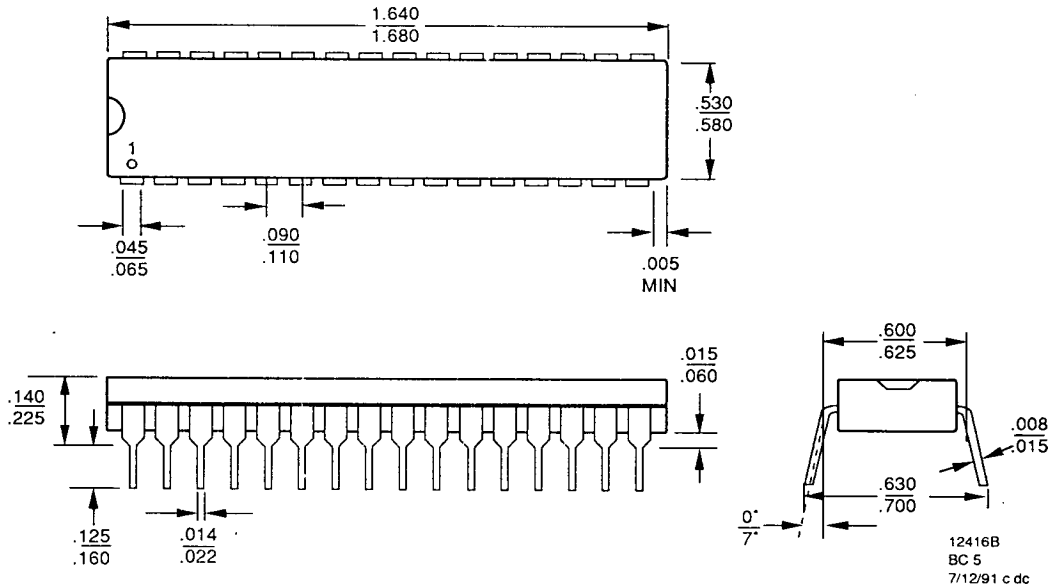
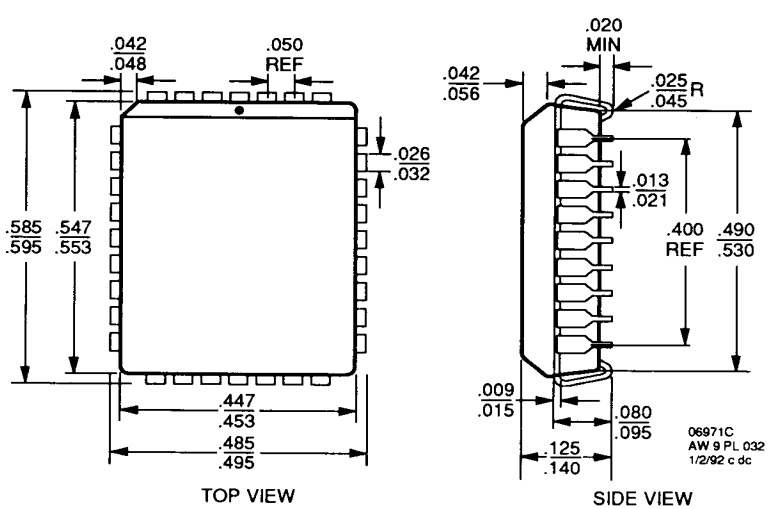
PD 032
Plastic Dip



PL 032
Plastic Leaded Chip Carrier



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