Am27C4096

4 Megabit (262,144 x 16-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 90 ns
- **Low power consumption**
  - — 100 µA maximum CMOS standby current
- **JEDEC-approved pinout**
  - — Plug in upgrade of 1 Mbit and 2 Mbit EPROMs
  - — 40-pin DIP/PDIP
  - — 44-pin LCC/PLCC

- **Single + 5 V power supply**
- **± 10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - — Typical programming time of 32 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**

GENERAL DESCRIPTION

The Am27C4096 is a 4 Mbit ultraviolet erasable programmable read-only memory. It is organized as 256K words by 16 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. The Am27C4096 is ideal for use in 16-bit microprocessor systems. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 90 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C4096 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$)

controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMDs CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 125 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C4096 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming times of 32 seconds.
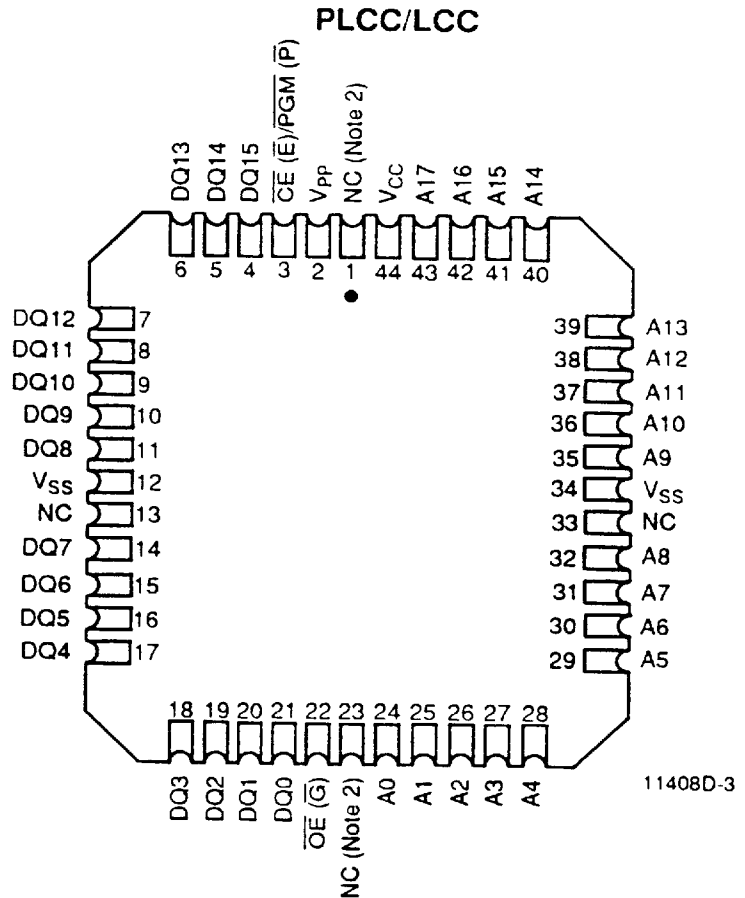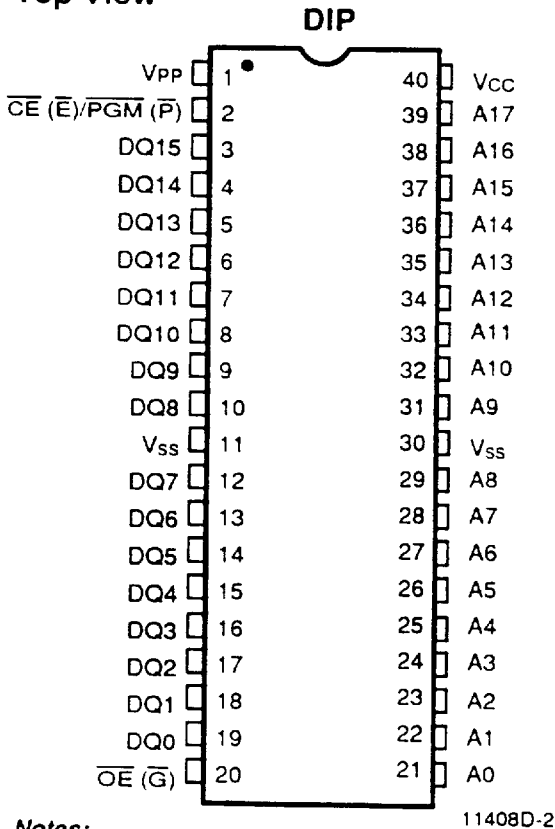
BLOCK DIAGRAM

11408D-1

0257528 0033007 205
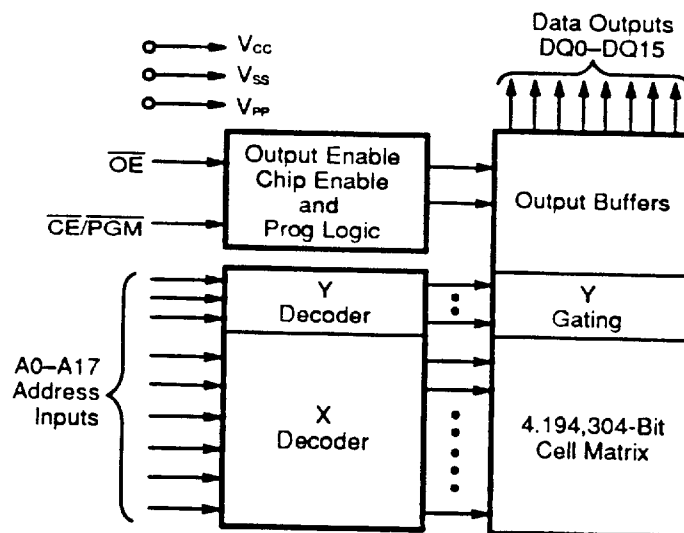
PRODUCT SELECTOR GUIDE

Family Part No.			Am27C4096				
Ordering Part No:							
Vcc ± 5%	-95	-105					
Vcc ±10%		-100	-120	-150	-200	-250
Max Access Time (ns)	90	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	90	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	50	50	50	65	75	100

CONNECTION DIAGRAMS

Top View

DIP

11408D-2

PLCC/LCC

11408D-3

Notes:

1. JEDEC nomenclature is in parentheses.
2. Don't use (DU) for PLCC.

PIN DESIGNATIONS

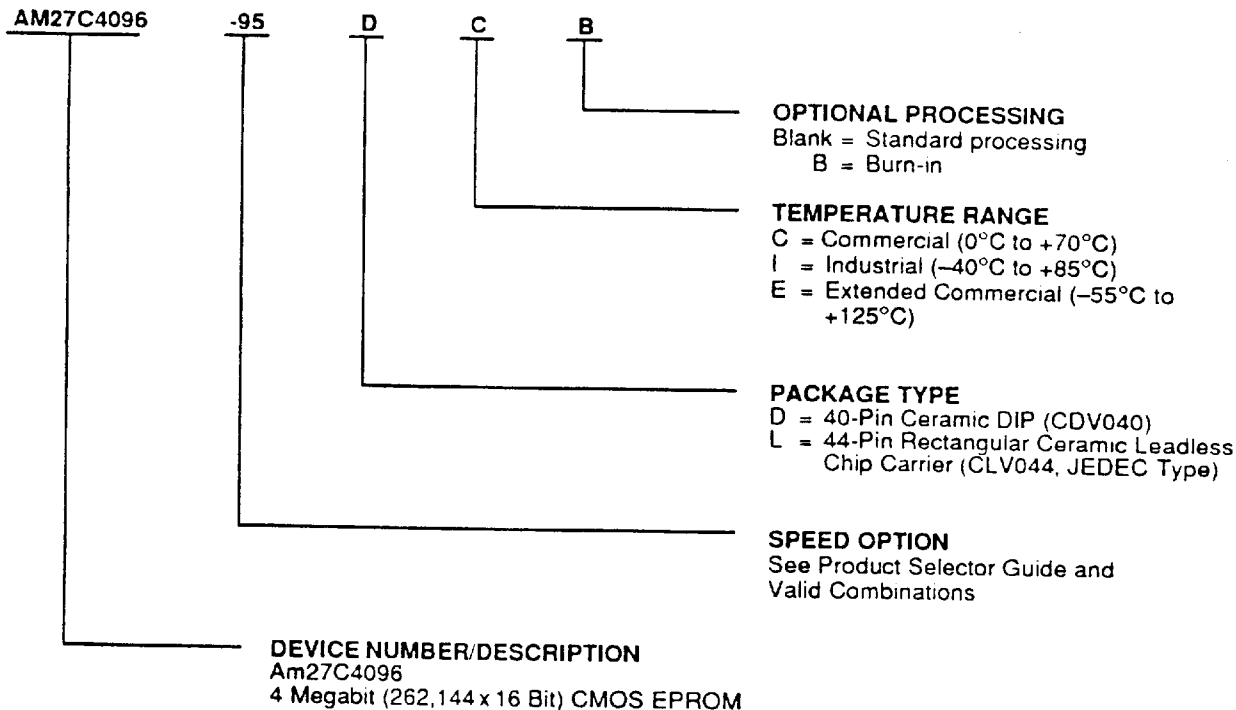|		
A0–A17	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)/$\overline{PGM}$ ($\overline{P}$)	=	Chip Enable Input
DQ0–DQ15	=	Data Input/Outputs
DU	=	No External Connection
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
Vcc	=	Vcc Voltage Input
VPP	=	Program Voltage Input
Vss	=	Ground

LOGIC SYMBOL

11408D-4
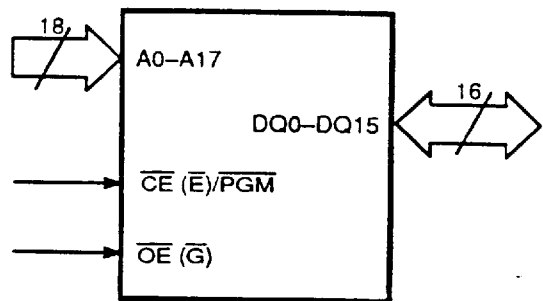
ORDERING INFORMATION
EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

```
AM27C4096    -95    D    C    B
```

OPTIONAL PROCESSING
Blank = Standard processing
     B = Burn-in

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended Commercial (–55°C to +125°C)

PACKAGE TYPE
D = 40-Pin Ceramic DIP (CDV040)
L = 44-Pin Rectangular Ceramic Leadless Chip Carrier (CLV044, JEDEC Type)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27C4096
4 Megabit (262,144 x 16 Bit) CMOS EPROM

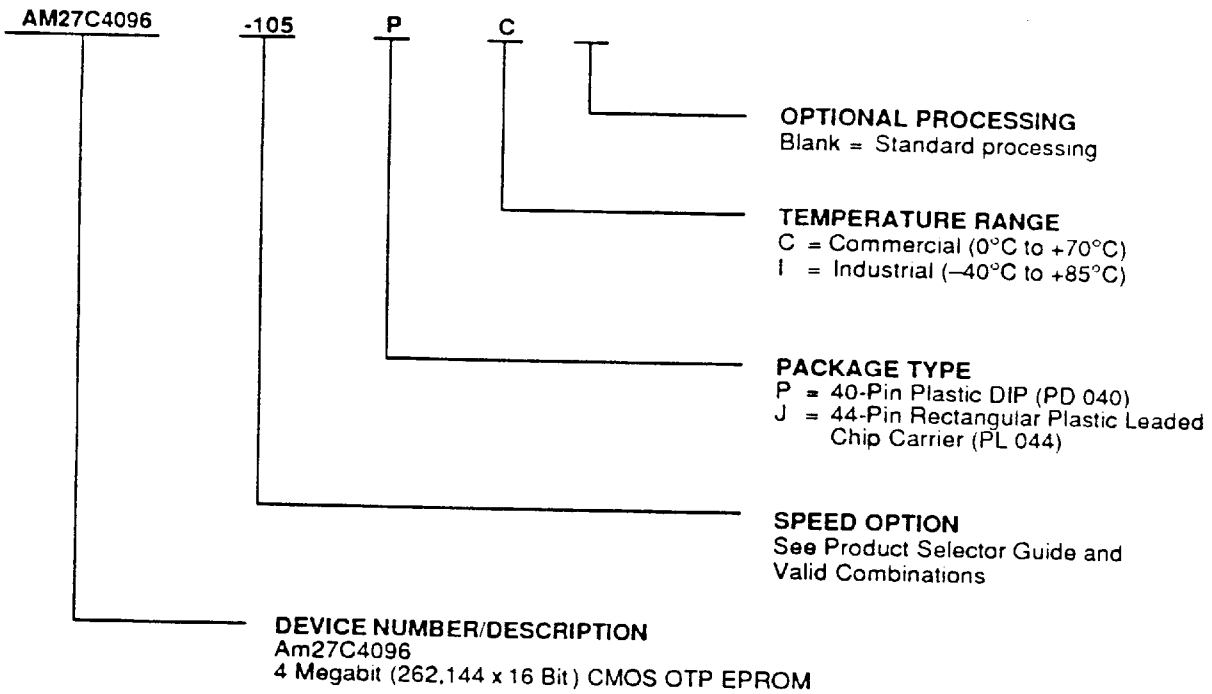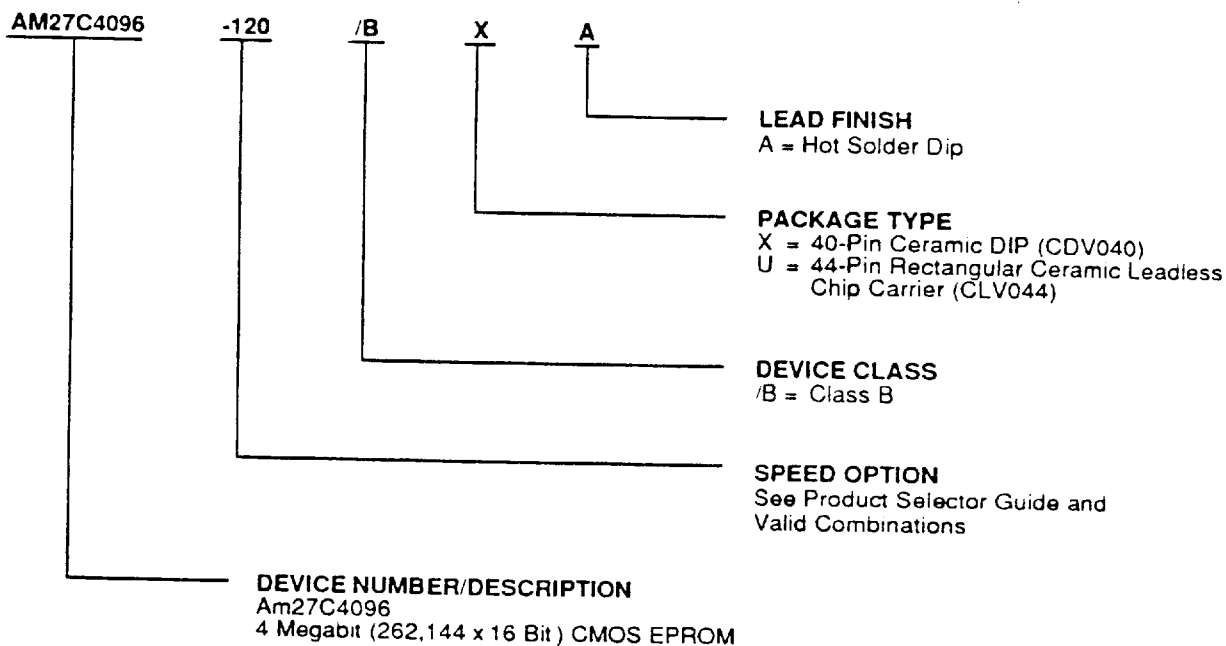| Valid Combinations	
AM27C4096-95	DC, DCB
AM27C4096-100	DC, DCB,
AM27C4096-105	DI, DIB
AM27C4096-120	DC, DCB, DE,
AM27C4096-150	DEB, DI, DIB,
AM27C4096-200	LC, LCB, LI, LIB, LE, LEB

Valid Combinations
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

■ 0257528 0033009 088 ■

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM27C4096 -105 P C

OPTIONAL PROCESSING
Blank = Standard processing

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (−40°C to +85°C)

PACKAGE TYPE
P = 40-Pin Plastic DIP (PD 040)
J = 44-Pin Rectangular Plastic Leaded
  Chip Carrier (PL 044)

SPEED OPTION
See Product Selector Guide and
Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27C4096
4 Megabit (262,144 x 16 Bit) CMOS OTP EPROM

Valid Combinations	
AM27C4096-105	PC, JC
AM27C4096-120	
AM27C4096-150	PC, JC, PI, JI
AM27C4096-200	

Valid Combinations
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

0257528 0033010 8TT

MILITARY ORDERING INFORMATION
Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

AM27C4096   -120   /B   X   A

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 40-Pin Ceramic DIP (CDV040)
U = 44-Pin Rectangular Ceramic Leadless
    Chip Carrier (CLV044)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and
Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27C4096
4 Megabit (262,144 x 16 Bit) CMOS EPROM

Valid Combinations	
AM27C4096-120	/BXA, /BUA
AM27C4096-150	
AM27C4096-200	
AM27C4096-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests
Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

■ 0257528 0033011 736 ■

FUNCTIONAL DESCRIPTION

Erasing The Am27C4096

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C4096 to an ultraviolet light source. A dosage of 15 W seconds/cm² is required to completely erase an Am27C4096. This dosage can be obtained by exposure to an ultraviolet lamp —wavelength of 2537 Å—with intensity of 12,000 μW/cm² for 15 to 20 minutes. The Am27C4096 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C4096 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C4096 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C4096

Upon delivery or after each erasure the Am27C4096 has all 4,194,304 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C4096 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the Vpp pin, $\overline{CE/PGM}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 16 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 μs programming pulses and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C4096. This part of the algorithm is done at Vcc = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at Vcc = Vpp = 5.25 V.

Please refer to Section 6 for programming flow chart and characteristics

Program Inhibit

Programming of multiple Am27C4096 in parallel with different data is also easily accomplished. Except for $\overline{CE/PGM}$, all like inputs of the parallel Am27C4096 may be common. A TTL low-level program pulse applied to an Am27C4096 $\overline{CE/PGM}$ input with Vpp = 12.75 V ± 0.25 V and $\overline{OE}$ HIGH will program that Am27C4096. A high-level $\overline{CE/PGM}$ input inhibits the other Am27C4096 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE/PGM}$ at V_{IH}, and Vpp between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C4096.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C4096. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device identifier code. For the Am27C4096, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C4096 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE/PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE/PGM}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE/PGM}$ has been LOW and addresses have been stable for at least tACC – tOE.

Standby Mode

The Am27C4096 has a CMOS standby mode which reduces the maximum Vcc current to 100 μA. It is placed in CMOS-standby when $\overline{CE/PGM}$ is at Vcc ± 0.3 V. The Am27C4096 also has a TTL-standby mode which reduces the maximum Vcc current to 1.0 mA. It is placed in TTL-standby when $\overline{CE/PGM}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections. a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE/PGM}$ be decoded and used as the primary device-selecting function. while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions. transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum. a $0.1–\mu F$ ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and Vss to minimize transient effects. In addition. to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a $4.7–\mu F$ bulk electrolytic capacitor should be used between Vcc and Vss for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE/PGM}$	$\overline{OE}$	A0	A9	Vpp	Outputs
Read		V_{IL}	V_{IL}	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	Hi–Z
Standby (TTL)		V_{IH}	X	X	X	X	Hi–Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	Hi–Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi–Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	19H

Notes:

1. $X = $ Either V_{IH} or V_{IL}

2. $V_H = 12.0$ V ± 0.5 V

3. $A1–A8 = A10–A17 = V_{IL}$

4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:
OTP Products .... –65°C to +125°C
All Other Products .... –65°C to +150°C

Ambient Temperature
with Power Applied .... –55°C to +125°C

Voltage with Respect to V_{SS}:

All pins except A9, V_{PP},
and V_{CC} (Note 1) .... –0.6 V to V_{CC} + 0.6 V

A9 and V_{PP} (Note 2) .... –0.6 V to 13.5 V

V_{CC} .... –0.6 V to 7.0 V

Notes:

1. *During transitions, the inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.*

2. *During transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) .... 0°C to +70°C
Industrial (I) Devices
Case Temperature (T_C) .... –40°C to +85°C
Extended Commercial (E) Devices
Case Temperature (T_C) .... –55°C to +125°C
Military (M) Devices
Case Temperature (T_C) .... –55°C to +125°C
Supply Read Voltages:
V_{CC} for Am27C4096-XX5 .... +4.75 V to +5.25 V
V_{CC} for Am27C4096-XX0 .... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 6, and 7 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = 400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +0.5	V
V_{IL}	Input LOW Voltage			−0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1.0	µA
I_{LO}	Output Leakage Current				5.0	µA
I_{CC1}	Vcc Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz OUT = 0 mA	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	Vcc TTL Standby	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	Vcc CMOS Standby	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	Vpp Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, Vpp = V_{CC}			100	µA

Notes:

1. Vcc must be simultaneously or before Vpp, and removed simultaneously or after Vpp.

2. Caution: The Am27C4096 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.

3. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.

4. Minimum DC Input Voltage is −0.5 V during transitions, the inputs may overshoot −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods less than 20 ns.
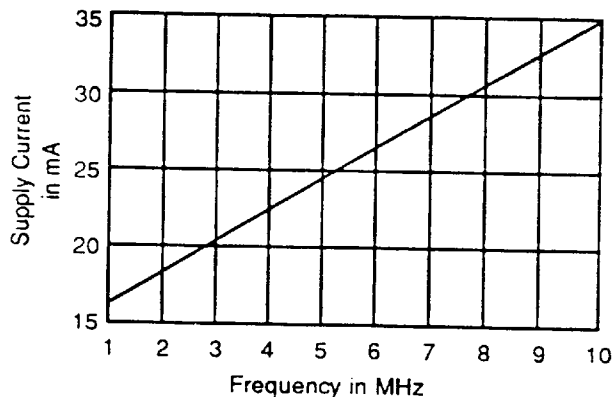

Figure 1. Typical Supply Current
vs. Frequency
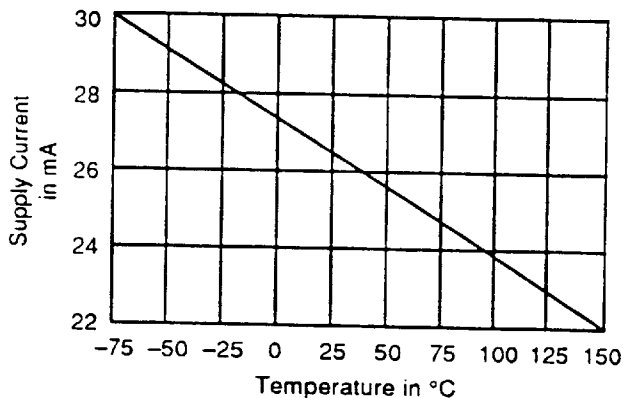Vcc = 5.5 V, T = 25°C

15573B-5

Figure 2. Typical Supply Current
vs. Temperature
Vcc = 5.5 V, f = 5 MHz

15573B-6

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CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV040		CLV044		PD040		PL044		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	$V_{IN} = 0$ V	10	13	10	13	6	8	10	13	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$ V	10	13	13	15	8	10	12	14	pF

Notes:

1. This parameter is only sampled and not 100% tested.

Switching CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C4096						Unit
JEDEC	Standard				-95	-105	-120	-150	-200	-255, -250	
A_{VQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min	–	–	–	–	–	–	ns
				Max	90	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min	–	–	–	–	–	–	ns
				Max	90	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min	–	–	–	–	–	–	ns
				Max	50	50	50	55	60	60	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	ns
				Max	30	30	40	40	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, CE, or OE, whichever ocurred first		Min	0	0	0	0	0	0	ns
				Max	–	–	–	–	–	–	

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. This parameter is only sampled and not 100% tested.

3. Caution: The Am27C4096 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.

4. Output Load: 1 TTL gate and $C_L = 100$ pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level — Inputs: 0.8 V to 2.0 V
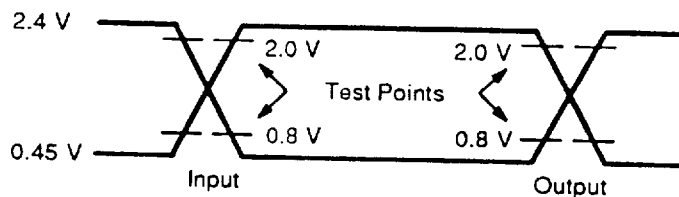   Outputs: 0.8 V to 2.0 V

SWITCHING TEST CIRCUIT
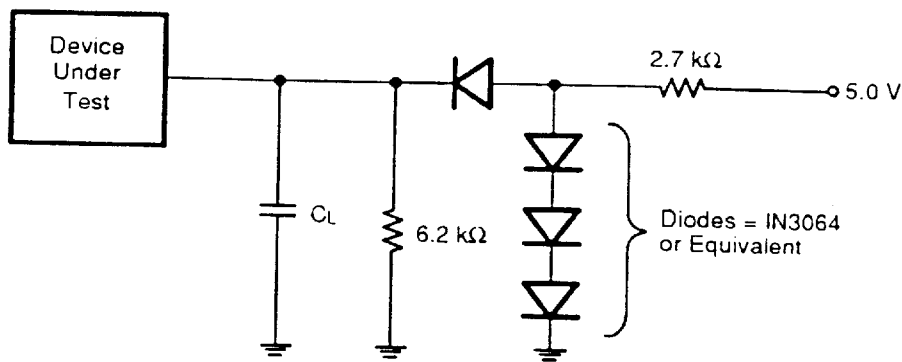
11408D-7

C_L = 100 pF including jig capacitance


SWITCHING TEST WAVEFORM

11408D-8

AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

Am27C4096

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORM
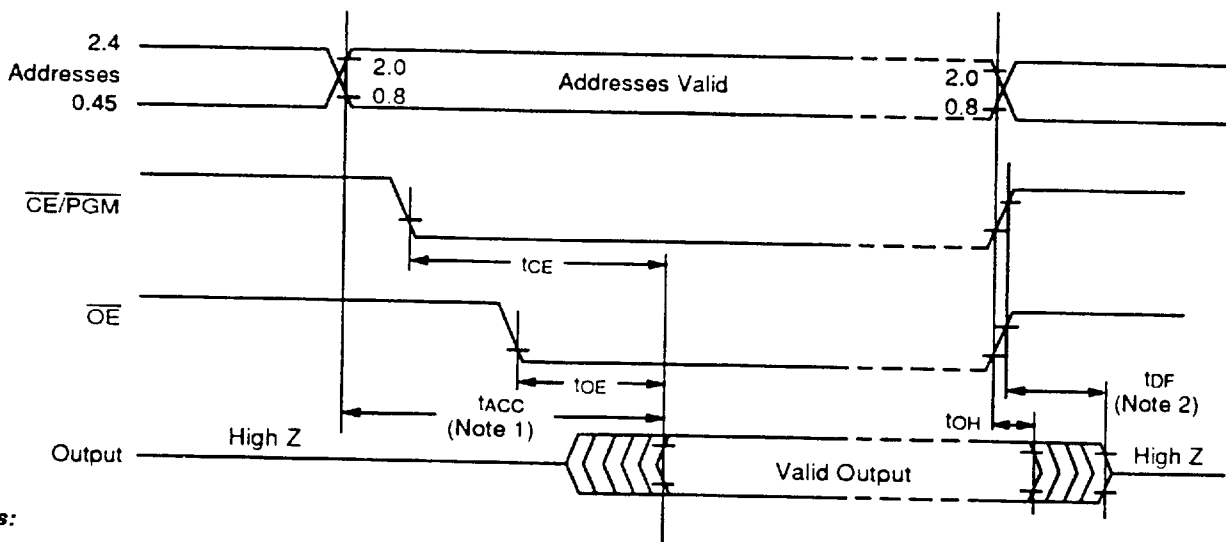
Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.

2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
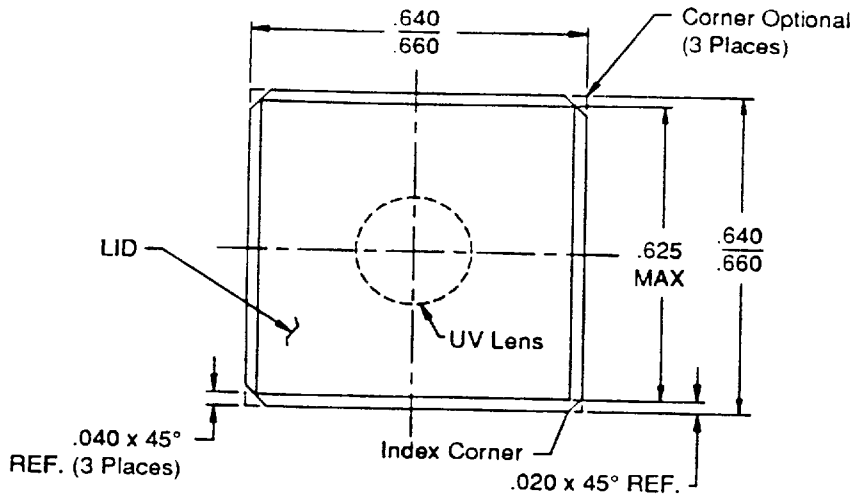
11408D-9

PHYSICAL DIMENSIONS*
CDV040
40-Pin Ceramic DIP (measured in inches)
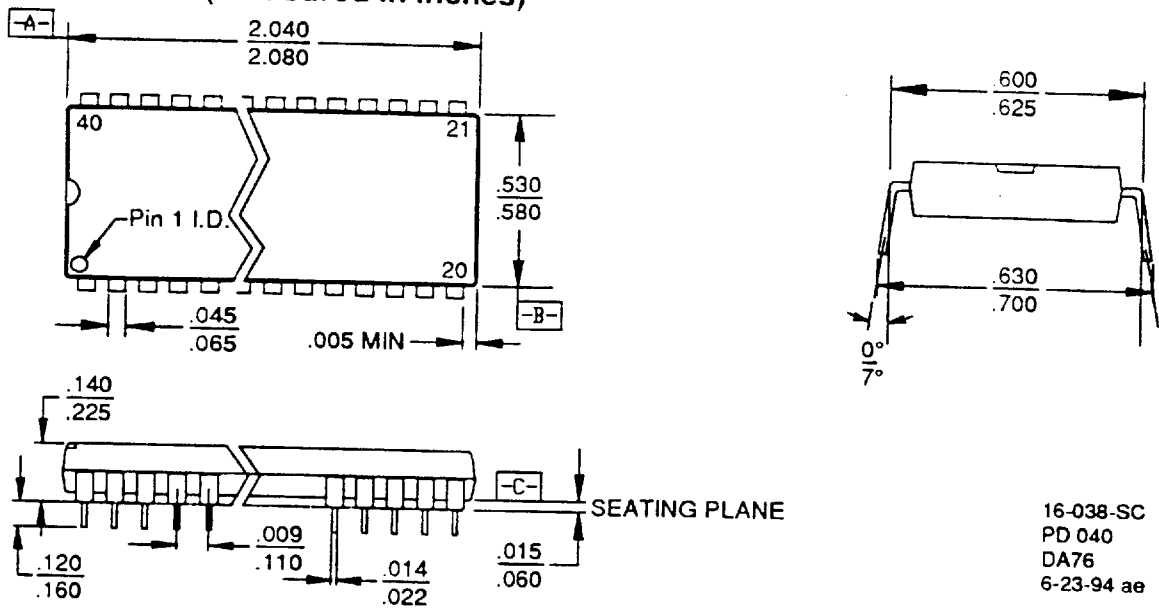

TOP VIEW

SIDE VIEW

END VIEW
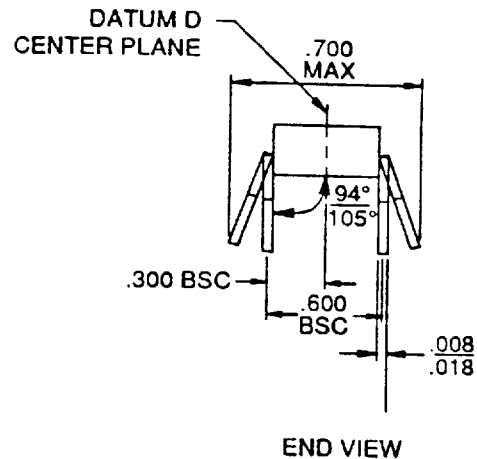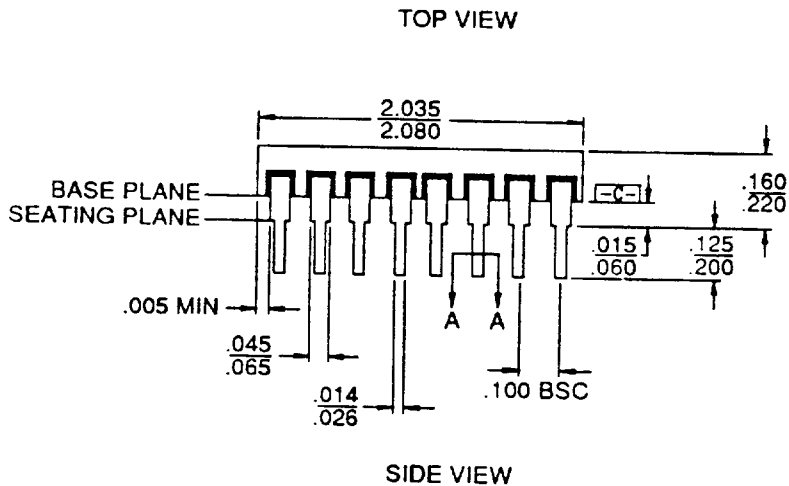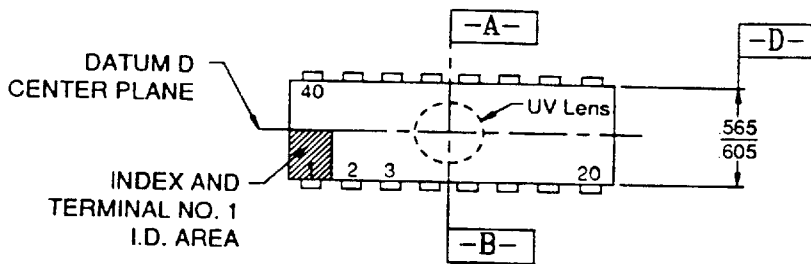
16-000038H-3
CDV040
DB11
6-23-94 ae

*For reference only. BSC is an ANSI standard for Basic Space Centering.

44-Pin Ceramic DIP (measured in inches)

TOP VIEW
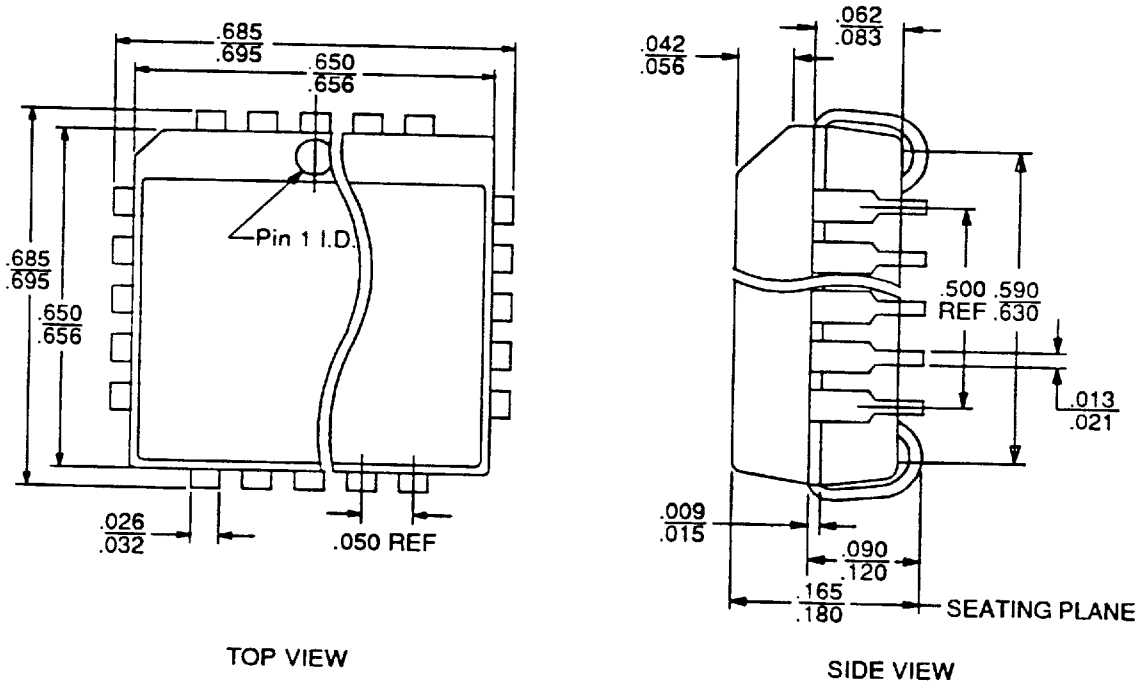
SIDE VIEW

BOTTOM VIEW
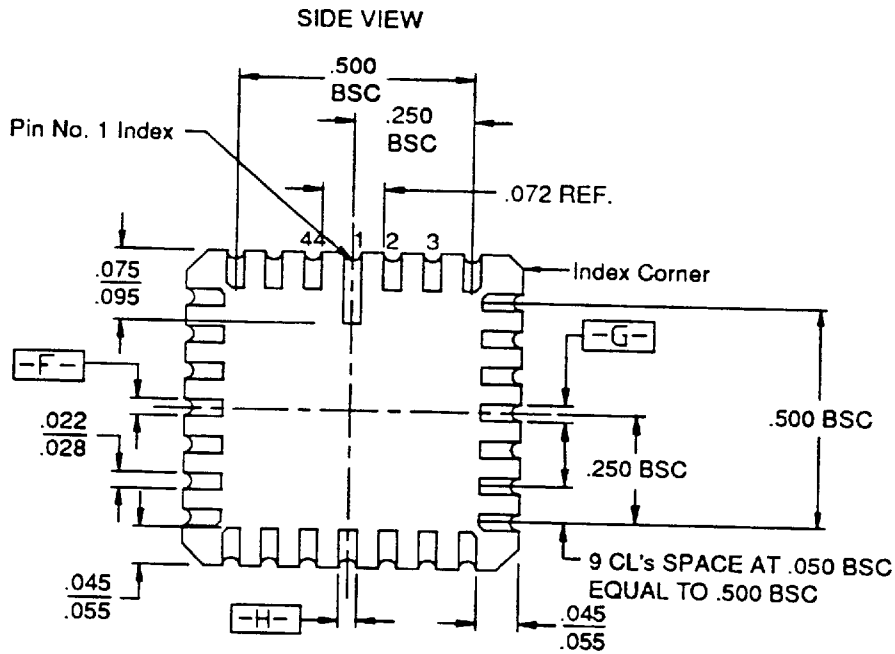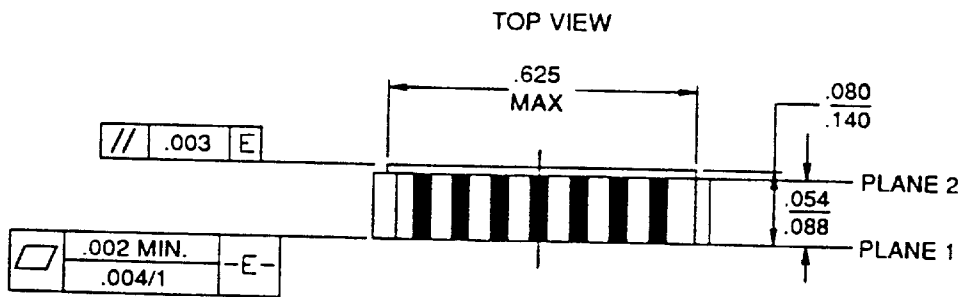
16-0000038C-5
CLV044
DA48
6-23-94 ae

Am27C4096

PD 040
40-Pin Plastic DIP (measured in inches)

16-038-SC
PD 040
DA76
6-23-94 ae

SEATING PLANE

PL 044
44-Pin Square Plastic Leaded
Chip Carrier (measured in inches)

TOP VIEW

SIDE VIEW

SEATING PLANE

16-038-SQ
PL 044
DA78
6-17-94 ae

Am27C4096

▄▄ 0257528 0033021 685 ▄▄