1.1 Scope.

This specification covers the requirements for a CMOS monolithic address generator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	ADSP-1410SD/883B
−2	ADSP-1410TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-48A.

1.3 Absolute Maximum Ratings.

Supply Voltage	−0.3V to 7V
Input Voltage	−0.3V to V_{DD}
Output Voltage	−0.3V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}: see MIL-M-38510, Appendix C.

ADSP-1410 – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Digital Input High Voltage	V_{IH}	−1, 2	2.0	2.0	2.0			V_{DD} = max	V min
Clock Input High Voltage*	V_{IHC}	−1, 2	3.0	3.5	3.5			V_{DD} = max	V min
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			V_{DD} = min	V max
Digital Output High Voltage	V_{OH}	−1, 2	2.4	2.4	2.4			V_{DD} = min I_{OH} = −1mA	V min
Digital Output Low Voltage*	V_{OL}	−1, 2	0.4	0.6	0.6			V_{DD} = min I_{OL} = +3mA	V max
Digital Input High Current	I_{IH}	−1, 2	10	10	10			V_{DD} = max V_{IN} = +5.0V	μA max
Digital Input Low Current	I_{IL}	−1, 2	10	10	10			V_{DD} = max V_{IN} = 0.0V	μA max
Three-State Leakage Current Low	I_{OZL}	−1, 2	50	50	50			V_{DD} = max V_{IN} = 0V (High Z)	μA max
Three-State Leakage Current High	I_{OZH}	−1, 2	50	50	50			V_{DD} = max V_{IN} = max (High Z)	μA max
Supply Current*	I_{DD1}	−1, 2	75	100	100			V_{DD} = max; TTL Inputs; f = max	mA max
	I_{DD2}	−1, 2	35	50	50			All V_{IN} = 2.4V	mA max
Instruction Setup Time*	t_{IS}	−1	20			30	30	Note 2	ns min
		−2	15			20	20		
Instruction Hold Time*	t_{IH}	−1	5			5	5	Note 2	ns min
		−2	4			4	4		
Instruction Cycle Time*	t_{CY}	−1	100			125	125	Note 2	ns min
		−2	90			100	100		
Input Data Setup Time	t_{IDS}	−1, 2	10			10	10	Note 2	ns min
Input Data Hold Time*	t_{IDH}	−1, 2	5			6	6	Note 2	ns min
Guaranteed Clock-to-Data Delay*	t_{ODD}	−1	35			45	45	Notes 2, 3	ns min
		−2	30			40	40		
		−1	55			70	70		ns max
		−2	50			60	60		
Output Data Disable Time*	t_{DDIS}	−1	20			25	25	Note 2	ns max
		−2	20			20	20		
Output Address Disable Time* (Latched Mode)	t_{ADISL}	−1	30			45	45	Note 2	ns max
		−2	25			40	40		
Output Address Disable Time* (Transparent Mode)	t_{ADIST}	−1	40			55	55	Note 2	ns max
		−2	35			50	50		
LATCHED MODE, GUARANTEED CLOCK-TO-OUTPUT DELAYS									
Pre-Update Address Delay*	t_{LAN}	−1	35			40	40	Notes 2, 3	ns min
		−2	30			35	35		
		−1	45			55	55		ns max
		−2	35			45	45		
Pre-Update CMP/Z Flag Delay*	t_{LFN}	−1	45			60	60	Notes 2, 3; C = 25pF	ns min
		−2	35			45	45		
		−1	55			75	75		ns max
		−2	45			60	60		

Table 1. (Continued on next page)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Output Data Enable Time	t_{DENA}	−1	30			40	40	Notes 2, 4	ns min
		−2	25			35	35		
		−1	50			65	65	Notes 2, 4	ns max
		−2	45			55	55		
Post-Update Address Delay*	t_{LAP}	−1	35			40	40	Notes 2, 3	ns min
		−2	30			35	35		
		−1	60			75	75	Notes 2, 4	ns max
		−2	50			55	55		
Post-Update CMP/Z Flag Delay*	t_{LFP}	−1	45			60	60	Notes 2, 3; C = 25pF	ns min
		−2	35			45	45		
		−1	70			95	95		ns max
		−2	55			75	75		
TRANSPARENT MODE, VALID-INSTRUCTION-TO-OUTPUT DELAYS									
Pre-Update Address Delay*	t_{TAN}	−1	50			65	65	Note 2	ns max
		−2	45			55	55		
Pre-Update CMP/Z Flag Delay*	t_{TFN}	−1	65			90	90	Note 2; C = 25pF	ns max
		−2	55			70	70		
Post-Update Address Delay*	t_{TAP}	−1	75			95	95	Note 2	ns max
		−2	65			80	80		
Post-Update CMP/Z Flag Delay*[4]	t_{TFP}	−1	90			115	115	Note 2; C = 25pF	ns max
		−2	75			95	95		
SUPPLEMENTAL PARAMETERS FOR DOUBLE-CHIP/DOUBLE-PRECISION OPERATIONS[5]									
Valid Instruction to Carry/ Shift Output Delay*	t_{CSD}	−1	65			80	80	Note 2	ns max
		−2	57			72	72		
Carry/Shift Input Setup Time*	t_{CSS}	−1	35			40	40	Note 2	ns min
		−2	28			35	35		
Carry/Shift Input to Valid MS Address (Post-Update Only)*	t_{MSD}	−1	45			55	55	Note 2	ns max
		−2	40			48	48		
Valid Instruction to MS CMP/Z Flag Delay	t_{CZD_C}	−1	115			120	120	Note 2	ns max
		−2	105			115	115		
Clock High to CMP/Z (Compare) Invalid Delay	t_{CZI}	−1, 2	4			4	4	Note 2	ns min
Valid Instruction to CMP/Z (Zero) Flag Delay	t_{CZD_Z}	−1	80			85	85	Note 2	ns max
		−2	70			80	80		
Instruction Valid to CMP/Z (Zero) Invalid Delay	t_{IID}	−1, 2	10			10	10	Note 2	ns min

NOTES

*Indicates that a limit for this parameter has changed from REV. A.

[1]T_A = +25°C; V_{DD} = +4.5V min to +5.5V max (unless otherwise noted).

[2]Input levels are GND and +3.0V; V_{DD} = +4.5V. Rise times are 5ns. Input timing reference levels and output reference levels are measured at +1.5V per Figure 1.

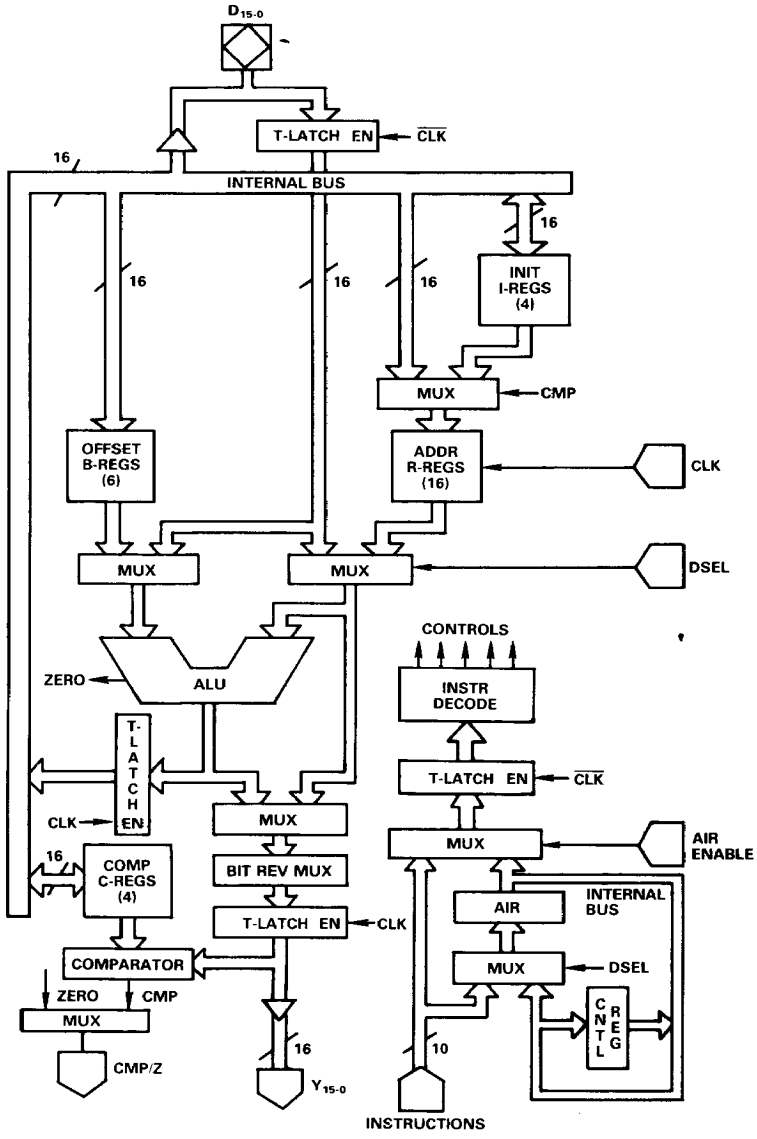
[3]Measured with the maximum usable instruction setup time before the rising edge of the clock. This max usable setup time may be calculated for any timing spec as: Maximum usable instruction setup time = max (t_{SPEC}) − min (t_{SPEC}) + min (t_{IS}). For example, Maximum usable setup time for t_{LAN} for the −2 part is: max (t_{LAN}) − min (t_{LAN}) + min (t_{IS}) = 45 − 35 + 20 = 30ns.

[4]Measured with the minimum instruction setup time for the respective −1 or −2 part.

[5]The Instruction Cycle Time, t_{CY}, does not apply to DCDP operation. Clock HI and LO relationships for DCDP operation are described in the text below under DCDP Parameters: t_{HI} is derived from the t_{CSD}, t_{CSS}, t_{MSD} and t_{IS} parameters, and the inequality $t_{LO} \geq t_{IS}$ must also hold.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

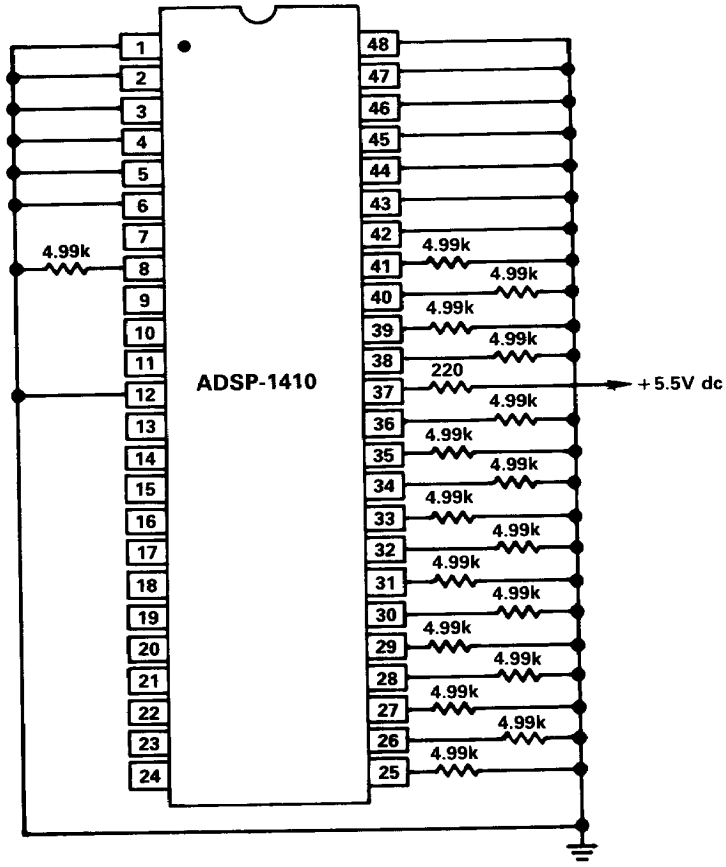
PIN	FUNCTION	PIN	FUNCTION
1	I4	48	I5
2	I3	47	I6
3	I2	46	I7
4	I1	45	I8
5	I0	44	I9
6	CLK	43	DSEL
7	CMP/Z	42	AIRE
8	Y15	41	D15
9	Y14	40	D14
10	Y13	39	D13
11	Y12	38	D12
12	GND	37	V_{DD}
13	Y11	36	D11
14	Y10	35	D10
15	Y9	34	D9
16	Y8	33	D8
17	Y7	32	D7
18	Y6	31	D6
19	Y5	30	D5
20	Y4	29	D4
21	Y3	28	D3
22	Y2	27	D2
23	Y1	26	D1
24	Y0	25	D0

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



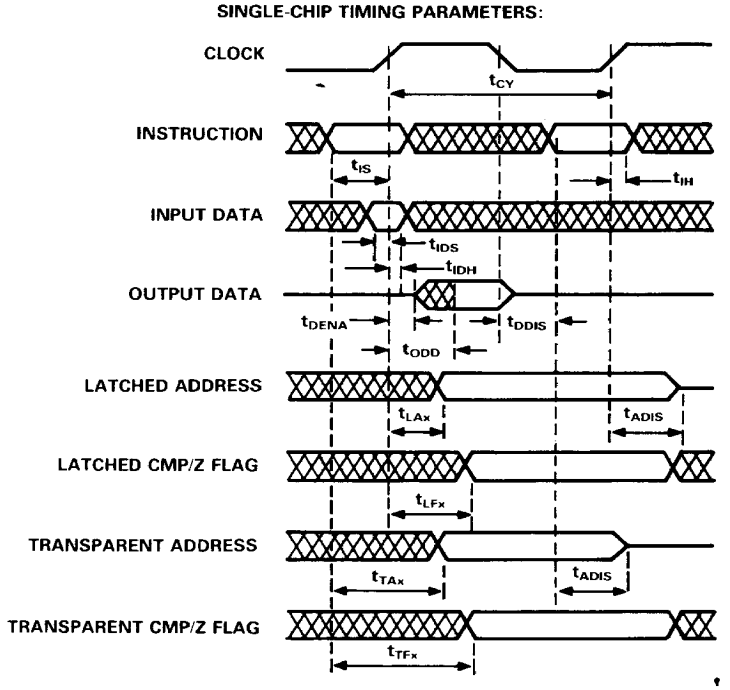


Figure 1. ADSP-1410 Timing Diagram

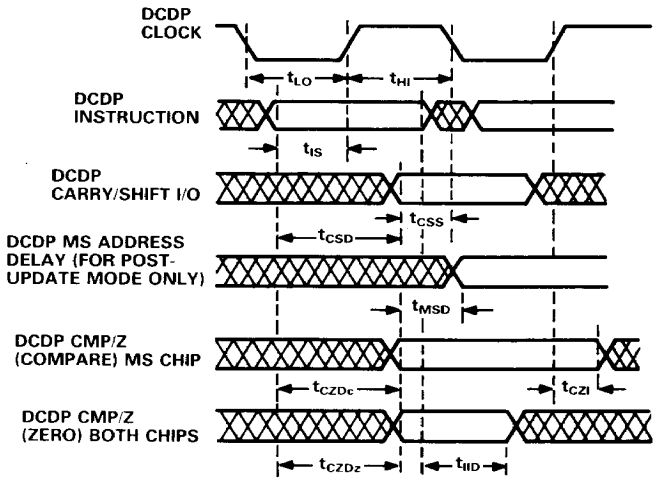


Figure 2. Supplemental Parameters for Double-Chip/Double-Precision Operation

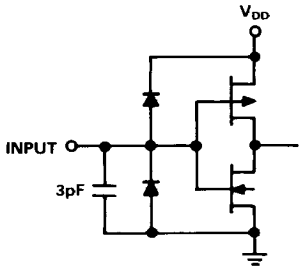


Figure 3. Equivalent Input Circuit

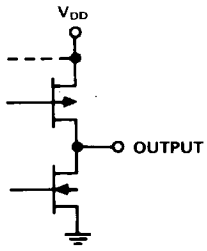


Figure 4. Equivalent Output Circuits

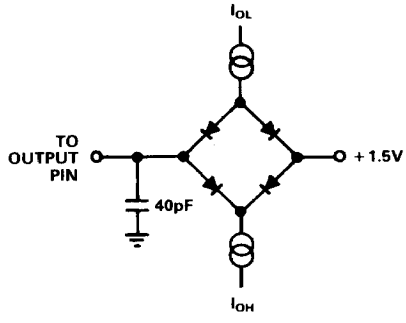


Figure 5. Normal Load for AC Measurements

REV. B

Instr.	Opcode (I_{9-0})	Description
Looping Instructions		
YINC*†:	1011ccrrrr	output & increment/init
YDEC*†:	1010ccrrrr	output & decrement/init
YADD*†:	11ccbb1rrr	output & add offset/init
YSUB*†:	11ccbb0rrr	output & subtract offset/init
Register Transfer Instructions		
YRTR*:	000101rrrr	output & xfr R to R
YRTB*:	0011bbrrrr	output & xfr R to B
YRTC*:	0010ccrrrr	output & xfr R to C
DTI:	0000111ii	xfr D to I
ITR:	1000iirrrr	xfr I to R
BTR:	0100bbrrrr	xfr B to R
RTD:	000100rrrr	xfr R to D
CTD:	00001100cc	xfr C to D
BTD:	00001101bb	xfr B to D
ITD:	00001110ii	xfr I to D
Logical and Shift Instructions		
YOR*†:	0111bbrrrr	output & OR B with/to R
YAND*†:	0110bbrrrr	output & AND B with/to R
YXOR*†:	0101bbrrrr	output & XOR B with/to R
YASR*†:	000111rrrr	output & arith SR R to R
YLSL*†:	000110rrrr	output & logical SL R to R
Control Register Instructions		
RST:	0000000001	reset CR
DTCR:	0000101110	xfr D to CR
CRTD:	0000101111	xfr CR to D
SETI:	0000100iix	set cond re-init on CMP mode
SETP:	00001010pp	set chip precision
SETY:	000001001x	set Y port to trans/latched mode
SELR:	000001101x	select upper/lower R bank
SELB:	000001100x	select upper/lower B bank
SETU:	000001011x	set post/pre update mode
SETA:	000001010x	set cond AIR mode
AIR Instructions		
WRA:	0000101100	write AIR with D
RDA:	0000101101	read AIR at D
LDA:	0000011110	load AIR on next cycle
Misc. Instructions		
YDTY:	0000011111	pass D to Y port
YREV*†:	1001bbrrrr	output R in bit-reverse format
NOP:	0000000000	no operation

*External data may substitute for R using DSEL.
†Operable in either pre- or post-update mode.

Table 2. ADSP-1410 Instruction Set