Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifier

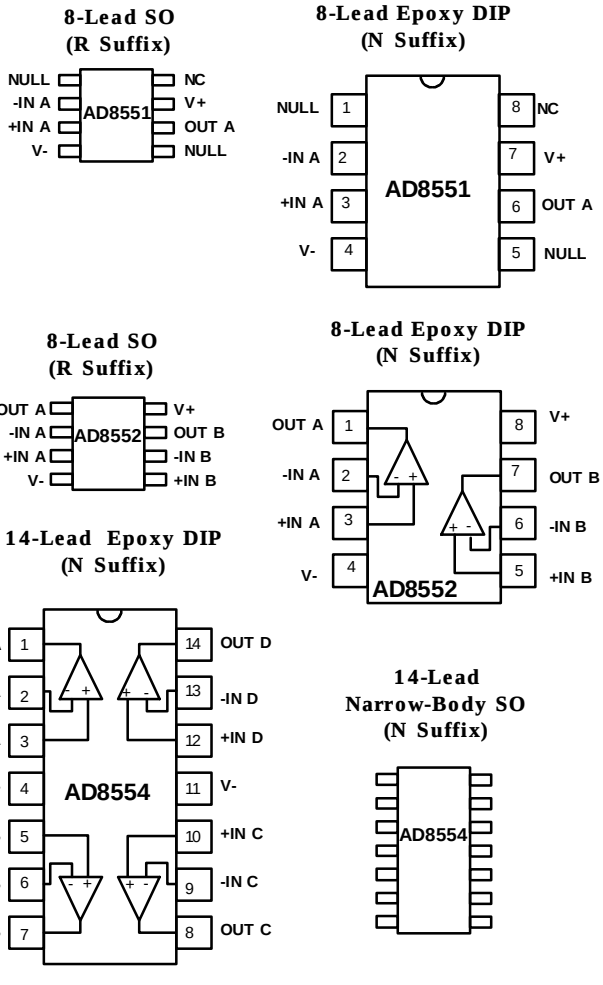
Preliminary AD8551/52/54

FEATURES

Low Offset Voltage: 5 µV
Input Offset Drift: 0.03 µV/°C
Rail-to-Rail Input and Output Swing
5 V Single-Supply Operation
High Gain, CMRR, PSRR: 120 dB
Ultra Low Input Bias Current: 20 pA
Low Supply Current: 650 µA/op amp
Overload Recovery Time: 2 ms
No External Components Required

APPLICATIONS

Automotive Sensors
Pressure and Position Sensors
Strain Gage Amplifiers
Medical Instrumentation
Thermocouple Amplifiers



Note: Pin orientation is equivalent for each package variation

GENERAL DESCRIPTION

This new family of amplifiers has **ultra-low offset, drift** and **bias current**. The AD8551, AD8552 and AD8534 are single, dual, and quad amplifiers featuring **rail-to-rail input and output** swings. All are guaranteed to operate from 2.7 to **5 volts single supply**.

The AD855x family provides the benefits previously found only in expensive auto-zeroing or chopper-stabilized amplifiers. Using Analog Devices' new topology these new zero-drift amplifiers combine low cost, with high accuracy. (No external capacitance is required.)

With an offset voltage of only 5µV and drift less than 0.03µV/°C, the AD8551 is perfectly suited for applications where error sources cannot be tolerated. Position and pressure sensors, medical equipment, and strain gage amplifiers benefit greatly from nearly zero drift over their operating temperature range. Many more systems require the rail-to-rail input and output swings provided by the AD855x family.

The AD8551/52/54 family is specified for the extended industrial (-40° to +125°C) temperature range. The AD8551 single and AD8552 dual amplifiers are available in 8-pin plastic DIP and SO surface mount packages. The AD8554 quad is available in the 14-pin DIP, and narrow 14-pin packages.

REV. 0

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ELECTRICAL SPECIFICATIONS (@ V_S=+5.0V, V_{CM} = 0.1V, V_O=1.4V, T_A=+25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage AD8551	V_{OS}			1	5	µV
		-40°C ≤ T_A ≤ +125°C			10	µV
AD8552/54	V_{OS}			1	8	µV
		-40°C ≤ T_A ≤ +125°C			12	µV
Input Bias Current	I_B			20	50	pA
		-40°C ≤ T_A ≤ +125°C			60	pA
Input Offset Current	I_{OS}			10	40	pA
		-40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 to 4.9V	110	130		dB
		-40°C ≤ T_A ≤ +125°C	100	120		dB
Large Signal Voltage Gain (Note 1)	A_{VO}	R_L = 10 kΩ , Vo=0.3 to 4.7V	110	120		dB
		-40°C ≤ T_A ≤ +125°C	100			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40°C ≤ T_A ≤ +125°C		0.02	0.04	µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$					pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$					pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100kΩ to Ground		4.95		V
		-40°C ≤ T_A ≤ +125°C				V
		R_L = 10kΩ to Ground		4.9		V
		-40°C ≤ T_A ≤ +125°C				V
Output Voltage Low	V_{OL}	R_L = 100kΩ to V+		50		mV
		-40°C ≤ T_A ≤ +125°C				mV
		R_L = 10 kΩ to V+		100		mV
		-40°C ≤ T_A ≤ +125°C				mV
Short Circuit Limit	I_{SC}		± 25	± 30		mA
		-40°C ≤ T_A ≤ +125°C		± 20		mA
Output Current	I_O		± 8			mA
		-40°C ≤ T_A ≤ +125°C	± 5			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7V to 5.5V	110	130		dB
		-40°C ≤ T_A ≤ +125°C	100	110		dB
Supply Current/Amplifier	I_{SY}	V_O = 0V		600		µA
		-40°C ≤ T_A ≤ +125°C		700		µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =10 kΩ		0.8		V/µs
Overload Recovery Time				2	5	ms
Gain Bandwidth Product	GBP			1.5		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 to 10 Hz		1.3		$\mu V_{p\text{-}p}$
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 to 1.0 Hz		0.4		$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f = 1 kHz		TBD		nV/√Hz
Current Noise Density	i_n	f=10 Hz		TBD		pA/√Hz

Note 1: Gain testing is highly dependent upon test bandwidth.

ELECTRICAL SPECIFICATIONS (@ V_S=+3.0V, V_{CM} = 0.1V, V_O=1.4V, T_A=+25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage AD8551	V_{OS}			1	5	µV
		-40°C ≤ T_A ≤ +125°C			10	µV
AD8552/54	V_{OS}			1	8	µV
		-40°C ≤ T_A ≤ +125°C			12	µV
Input Bias Current	I_B			20	50	pA
		-40°C ≤ T_A ≤ +125°C			60	pA
Input Offset Current	I_{OS}			10	40	pA
		-40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 to 2.9V	110	130		dB
		-40°C ≤ T_A ≤ +125°C	100	120		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ , Vo=0.3 to 4.7V	110	120		dB
		-40°C ≤ T_A ≤ +125°C	100			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40°C ≤ T_A ≤ +125°C		0.02	0.04	µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$					pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$					pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100kΩ to Ground		2.9		V
		-40°C ≤ T_A ≤ +125°C				V
		R_L = 10kΩ to Ground		2.75		V
		-40°C ≤ T_A ≤ +125°C				V
Output Voltage Low	V_{OL}	R_L = 100kΩ to V+		100		mV
		-40°C ≤ T_A ≤ +125°C				mV
		R_L = 10 kΩ to V+		250		mV
		-40°C ≤ T_A ≤ +125°C				mV
Short Circuit Limit	I_{SC}		±	±		mA
		-40°C ≤ T_A ≤ +125°C		±		mA
Output Current	I_O		± 5			mA
		-40°C ≤ T_A ≤ +125°C	±			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7V to 5.5 V	110	130		dB
		-40°C ≤ T_A ≤ +125°C	100	110		dB
Supply Current/Amplifier	I_{SY}	V_O = 0V		200		µA
		-40°C ≤ T_A ≤ +125°C		250		µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =10 kΩ		0.5		V/µs
Overload Recovery Time				2		ms
Gain Bandwidth Product	GBP			1		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p-p}$	0.1 to 10 Hz		TBD		μV_{p-p}
Voltage Noise Density	e_n	f = 1 kHz		TBD		nV/√Hz
Current Noise Density	i_n	f=10 Hz		TBD		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Supply Voltage.....+6V
Input Voltage .....GND to Vs + 0.3V
Differential Input Voltage[1] .....±5.0V
Output Short-Circuit Duration to Gnd.....Indefinite
Storage Temperature Range
N, R Package.....-65°C to +150°C
Operating Temperature Range
AD8551/52/54A .....-40°C to +125°C
Junction Temperature Range
N, R Package.....-65°C to +150°C
Lead Temperature Range (Soldering, 10 sec).....+300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Plastic DIP (N)	103	43	°C/W
8-Pin SOIC (R)	158	43	°C/W
14-Pin Plastic DIP (N)	76	33	°C/W
14-Pin SOIC(R)	120	36	°C/W

NOTES

[1] Differential input voltage is limited to ±5.0 volts or the supply voltage, whichever is less.

[2] θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; $\theta_{JA}$is specified for device soldered in circuit board for SOIC and TSSOP packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8551AN	-40°C to +125°C	8-Pin Plastic DIP	N-8
AD8551AR	-40°C to +125°C	8-Pin SOIC	SO-8
AD8552AN	-40°C to +125°C	8-Pin Plastic DIP	N-8
AD8552AR	-40°C to +125°C	8-Pin SOIC	SO-8
AD8554AN	-40°C to +125°C	14-Pin Plastic DIP	N-14
AD8554AR	-40°C to +125°C	14-Pin SOIC	SO-14

APPLICATIONS