

## Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifier

# **Preliminary**

### AD8551/52/54

#### **FEATURES**

Low Offset Voltage: 5 μV Input Offset Drift: 0.03 μV/°C Rail-to-Rail Input and Output Swing 5 V Single-Supply Operation High Gain, CMRR, PSRR: 120 dB Ultra Low Input Bias Current: 20 pA Low Supply Current: 650 μA/op amp Overload Recovery Time: 2 ms No External Components Required

#### **APPLICATIONS**

Automotive Sensors
Pressure and Position Sensors
Strain Gage Amplifiers
Medical Instrumentation
Thermocouple Amplifiers

#### **GENERAL DESCRIPTION**

This new family of amplifiers has ultra-low offset, drift and bias current. The AD8551, AD8552 and AD8534 are single, dual, and quad amplifiers featuring rail-to-rail input and output swings. All are guaranteed to operate from 2.7 to 5 volts single supply.

The AD855x family provides the benefits previously found only in expensive auto-zeroing or chopper-stabilized amplifiers. Using Analog Devices' new topology these new zero-drift amplifiers combine low cost, with high accuracy. (No external capacitance is required.)

With an offset voltage of only  $5\mu V$  and drift less than  $0.03\mu V/^{\circ}C$ , the AD8551 is perfectly suited for applications where error sources cannot be tolerated. Position and pressure sensors, medical equipment, and strain gage amplifiers benefit greatly from nearly zero drift over their operating temperature range. Many more systems require the rail-to-rail input and output swings provided by the AD855x family.

The AD8551/52/54 family is specified for the extended industrial (-40° to +125°C) temperature range. The AD8551 single and AD8552 dual amplifiers are available in 8-pin plastic DIP and SO surface mount packages. The AD8554

### REV. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

8-Lead Epoxy DIP 8-Lead SO (N Suffix) (R Suffix) NULL I ⊐ NC -IN A □ **□** ۷+ NULL AD8551 OUT A +IN A NULL V- F AD8551 OUT A NULL 8-Lead Epoxy DIP 8-Lead SO (N Suffix) (R Suffix) OUT A 🗆 8 АD8552 □ ООТ В -IN A □ +IN A C □ -IN B OUT B □ +IN B 6 -IN B 14-Lead Epoxy DIP (N Suffix) 5 14 OUT D 14-Lead 13 Narrow-Body SO (N Suffix) +IN D AD8554 10 +IN C AD8554 -IN C OUT C

Note: Pin orientation is equivalent for each package variation quad is available in the 14-pin DIP, and narrow 14-pin packages.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A. Tel: 617/329-4700 World Wide Web Site:http://www.analog.com Fax: 617/326-8703 © Analog Devices, Inc., 1997

### $\begin{tabular}{ll} \textbf{ELECTRICAL SPECIFICATIONS} \ (@\ V_S=+5.0V,\ V_{CM}=0.1V,\ V_O=1.4V,\ T_A=+25^{\circ}C\ unless\ otherwise\ specified.) \end{tabular}$

Parameter		Symbol	Conditions	Min	Тур	Max	Units
INPUT CHARACTERI	STICS						
Offset Voltage	AD8551	V <sub>OS</sub>			1	5	μV
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$			10	μV
	AD8552/54	V <sub>OS</sub>			1	8	μV
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$			12	μV
Input Bias Current		$I_{\mathrm{B}}$			20	50	pA
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$			60	pA
Input Offset Current		I <sub>OS</sub>			10	40	pA
-			$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$			50	nA
Input Voltage Range			1	0		5	V
Common-Mode Rejecti	on Ratio	CMRR	$V_{CM} = 0$ to 4.9V	110	130		dB
			$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$	100	120		dB
Large Signal Voltage G	ain (Note 1)	A <sub>VO</sub>	$R_L = 10 \text{ k}\Omega$ , Vo=0.3 to 4.7V	110	120		dB
Zange Signar + Sinage Guin (110te 1)		'0	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$	100			dB
Offset Voltage Drift		$\Delta V_{OS}/\Delta T$	$-40^{\circ}\text{C} \le T_{A} \le +125^{\circ}\text{C}$		0.02	0.04	μV/°C
Bias Current Drift		$\Delta I_{\rm B}/\Delta T$	10 0 = 1A = 1120 0		0.02	0.0.	pA/°C
Offset Current Drift		$\Delta I_{OS}/\Delta T$					pA/°C
	DICTICC	Δ105/Δ1	+				pri c
OUTPUT CHARACTERISTICS			D = 100kO to Cround		4.95		V
Output Voltage High		V <sub>OH</sub>	$R_L = 100 \text{k}\Omega$ to Ground		4.93		V
			$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$		4.0		
			$R_L = 10k\Omega$ to Ground		4.9		V
			$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$				V
Output Voltage Low		V <sub>OL</sub>	$R_L = 100 k\Omega$ to V+		50		mV
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$				mV
			$R_L = 10 \text{ k}\Omega \text{ to V}+$		100		mV
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$				mV
Short Circuit Limit		I <sub>SC</sub>		± 25	± 30		mA
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$		± 20		mA
Output Current		I <sub>O</sub>		± 8			mA
			$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$	± 5			mA
POWER SUPPLY							
Power Supply Rejection	n Ratio	PSRR	$V_S = 2.7V \text{ to } 5.5V$	110	130		dB
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$	100	110		dB
Supply Current/Amplif	ier	I <sub>SY</sub>	$V_{O} = 0V$		600		μA
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$		700		μΑ
DYNAMIC PERFORM	IANCE						
Slew Rate		SR	$R_{\rm L} = 10 \text{ k}\Omega$		0.8		V/µs
Overload Recovery Tim	ne				2	5	ms
Gain Bandwidth Produc		GBP			1.5		MHz
NOISE PERFORMANO	CE						
Voltage Noise		e <sub>n p-p</sub>	0.1 to 10 Hz		1.3		μV <sub>p-p</sub>
Voltage Noise		e <sub>n p-p</sub>	0.1 to 1.0 Hz		0.4		μV <sub>p-p</sub>
Voltage Noise Density		e <sub>n</sub>	f = 1  kHz		TBD		nV/√Hz
Current Noise Density		in	f=10 Hz		TBD		pA/√Hz

Note 1: Gain testing is highly dependent upon test bandwidth.

# **Preliminary**

AD8551/251/451

 $\begin{tabular}{ll} \textbf{ELECTRICAL SPECIFICATIONS} \ (@\ V_{S}=+3.0V,\ V_{CM}=0.1V,\ V_{O}=1.4V,\ T_{A}=+25^{\circ}C\ unless\ otherwise\ specified.) \end{tabular}$ 

Parameter		Symbol	Conditions	Min	Тур	Max	Units
INPUT CHARACTI	ERISTICS						
Offset Voltage	AD8551	V <sub>OS</sub>			1	5	μV
			$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$			10	μV
	AD8552/54	V <sub>OS</sub>			1	8	μV
			$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$			12	μV
Input Bias Current		$I_{\mathrm{B}}$			20	50	pA
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$			60	pA
Input Offset Current		I <sub>OS</sub>			10	40	pA
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$			50	nA
Input Voltage Range	e			0		5	V
Common-Mode Rejo	ection Ratio	CMRR	$V_{CM} = 0$ to 2.9V	110	130		dB
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$	100	120		dB
Large Signal Voltag	e Gain	A <sub>VO</sub>	$R_L = 10 \text{ k}\Omega$ , Vo=0.3 to 4.7V	110	120		dB
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$	100			dB
Offset Voltage Drift		$\Delta V_{OS}/\Delta T$	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$		0.02	0.04	μV/°C
Bias Current Drift		$\Delta I_B/\Delta T$					pA/°C
Offset Current Drift		$\Delta I_{OS}/\Delta T$					pA/°C
OUTPUT CHARAC		0.5					_
Output Voltage High		V <sub>OH</sub>	$R_L = 100k\Omega$ to Ground		2.9		V
, ,			$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$				V
			$R_L = 10k\Omega$ to Ground		2.75		V
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$				V
Output Voltage Low	7	V <sub>OL</sub>	$R_{L} = 100k\Omega$ to V+		100		mV
output voltage 20 m		OL	$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$		100		mV
			$R_L = 10 \text{ k}\Omega \text{ to V} +$		250		mV
			$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$		230		mV
Short Circuit Limit		I.a.	-40 C 3 1 <sub>A</sub> 3 +123 C	±	±		mA
Short Circuit Limit		I <sub>SC</sub>	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$	_	±		mA
Output Current		I <sub>O</sub>	-40 C 3 1 <sub>A</sub> 3 +123 C	± 5			mA
Output Current		l 10	$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$				mA
DOWED CLIDDLY			-40 C S I <sub>A</sub> S +123 C	±			IIIA
POWER SUPPLY	tion Datio	PSRR	$V_S = 2.7V \text{ to } 5.5 \text{ V}$	110	130		dB
Power Supply Rejec	uon Kauo	FSKK		100			dB
Supply Current/Amp	nlifiar	ī	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$	100	110 200		
Supply Current/Am	piliter	I <sub>SY</sub>	$V_O = 0V$				μΑ
	D. C. L. V.		$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$		250		μА
DYNAMIC PERFO	KMANCE	CD	D 101-0		0.5		V/···
Slew Rate	т.	SR	$R_L = 10 \text{ k}\Omega$		0.5		V/µs
Overload Recovery Time		GBP			2		ms MHz
Gain Bandwidth Product NOISE PERFORMANCE		UDP			1		MIUS
Voltage Noise	TINCE	e	0.1 to 10 Hz		TBD		μV <sub>p-p</sub>
Voltage Noise Dens	ity	e <sub>n p-p</sub>					$nV/\sqrt{Hz}$
	-	e <sub>n</sub>	f = 1  kHz		TBD		pA/√Hz
Current Noise Density		in	f=10 Hz		TBD		pA/ vHz

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage+6V
Input VoltageGND to $Vs + 0.3V$
Differential Input Voltage <sup>1</sup> ±5.0V
Output Short-Circuit Duration to GndIndefinite
Storage Temperature Range
N, R Package65°C to +150°C
Operating Temperature Range
AD8551/52/54A40°C to +125°C
Junction Temperature Range
N, R Package65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)+300°C

Package Type	$\theta_{JA}^2$	θЈС	Units
8-Pin Plastic DIP (N)	103	43	°C/W
8-Pin SOIC (R)	158	43	°C/W
14-Pin Plastic DIP (N)	76	33	°C/W
14-Pin SOIC(R)	120	36	°C/W

### NOTES

### **ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option
AD8551AN	-40°C to +125°C	8-Pin Plastic DIP	N-8
AD8551AR	-40°C to +125°C	8-Pin SOIC	SO-8
AD8552AN	-40°C to +125°C	8-Pin Plastic DIP	N-8
AD8552AR	-40°C to +125°C	8-Pin SOIC	SO-8
AD8554AN	-40°C to +125°C	14-Pin Plastic DIP	N-14
AD8554AR	-40°C to +125°C	14-Pin SOIC	SO-14

### **APPLICATIONS**

 $<sup>^{1}</sup>$  Differential input voltage is limited to  $\pm 5.0$  volts or the supply voltage, whichever is less.

 $<sup>^2\,\</sup>theta_{JA}$  is specified for the worst case conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for P-DIP packages;  $\theta_{JA}$  is specified for device soldered in circuit board for SOIC and TSSOP packages.