

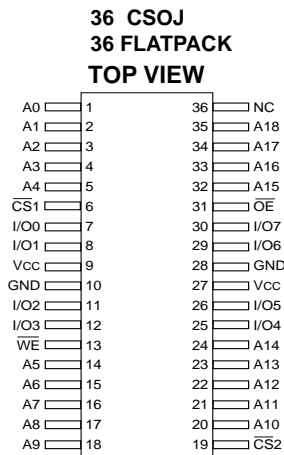


2x512Kx8 DUALITHIC™ SRAM

FEATURES

- Access Times 17, 20, 25, 35, 45, 55ns
- Revolutionary, Center Power/Ground Pinout
- Packaging:
 - 32 pin, Hermetic Ceramic DIP (Package 300)
 - 36 lead Ceramic SOJ (Package 100)
 - 36 lead Ceramic Flatpack (Package 226)
- Organized as two banks of 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs

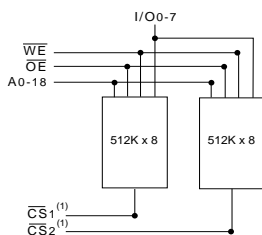
PIN CONFIGURATION FOR WS1M8-XDJX AND WS1M8-XFX



PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS1-2	Chip Selects
OE	Output Enable
WE	Write Enable
Vcc	+5.0V Power
GND	Ground

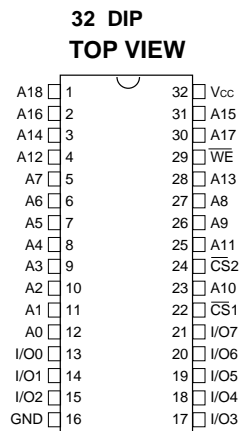
BLOCK DIAGRAM



NOTE:

1. CS1 and CS2 are used to select the lower and upper 512Kx8 of the device. CS1 and CS2 must not be enabled at the same time.

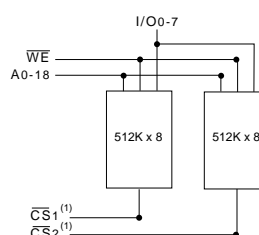
PIN CONFIGURATION FOR WS1M8-XCX

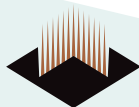


PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS1-2	Chip Selects
WE	Write Enable
Vcc	+5.0V Power
GND	Ground

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

NOTE: \overline{OE} is internally tied to the GND and not accessible on the WS1M8-XXC.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	20	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions			Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IH} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO} ¹	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = GND \text{ to } V_{CC}$		10	μA
Operating Supply Current	I _{CC} ¹	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		180	mA
Standby Current	I _{SB} ¹	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		40	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

1. \overline{OE} is internally tied to the GND and not accessible on the WS1M8-XXC.

LOW POWER DATA RETENTION CHARACTERISTICS (WS1M8L-XXX ONLY)

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions				Units
			Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		3.0	18.0*	mA



AC CHARACTERISTICS
(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	17		20		25		35		45		55		ns
Address Access Time	t _{AA}		17		20		25		35		45		55	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		0		ns
Chip Select Access Time	t _{ACS}		17		20		25		35		45		55	ns
Output Enable to Output Valid	t _{OE²}		9		10		12		25		25		25	ns
Chip Select to Output in Low Z	t _{CLZ¹}	2		2		2		4		4		4		ns
Output Enable to Output in Low Z	t _{OLZ²}	0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ¹}		9		10		12		15		20		20	ns
Output Disable to Output in High Z	t _{OHZ²}		9		10		12		15		20		20	ns

1. This parameter is guaranteed by design but not tested.
2. OE is internally tied to the GND and not accessible on the WS1M8-XXC.

AC CHARACTERISTICS
(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	17		20		25		35		45		55		ns
Chip Select to End of Write	t _{CW}	14		14		15		25		35		50		ns
Address Valid to End of Write	t _{AW}	14		14		15		25		35		50		ns
Data Valid to End of Write	t _{DW}	9		10		10		20		25		25		ns
Write Pulse Width	t _{WP}	14		14		15		25		35		40		ns
Address Setup Time	t _{AS}	0		0		0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		5		5		ns
Output Active from End of Write	t _{OW¹}	2		3		4		4		5		5		ns
Write Enable to Output in High Z	t _{WHZ¹}		9		9		10		15		15		25	ns
Data Hold Time	t _{DH}	0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

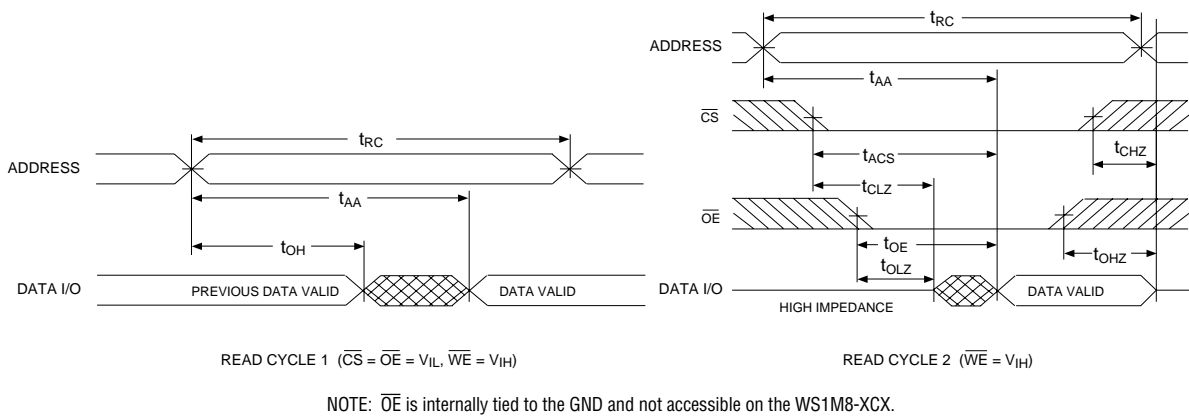
AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

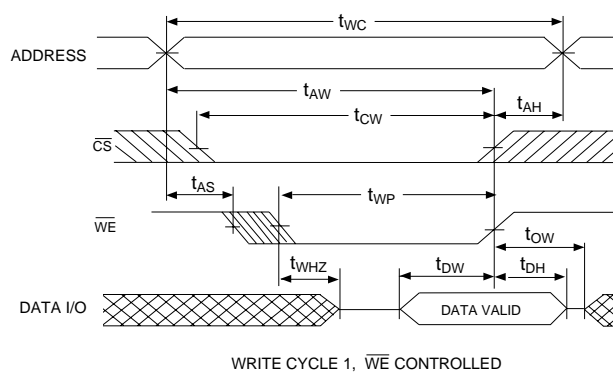
NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



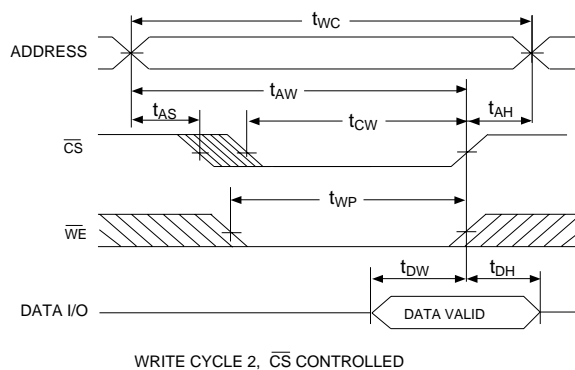
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - \overline{WE} CONTROLLED

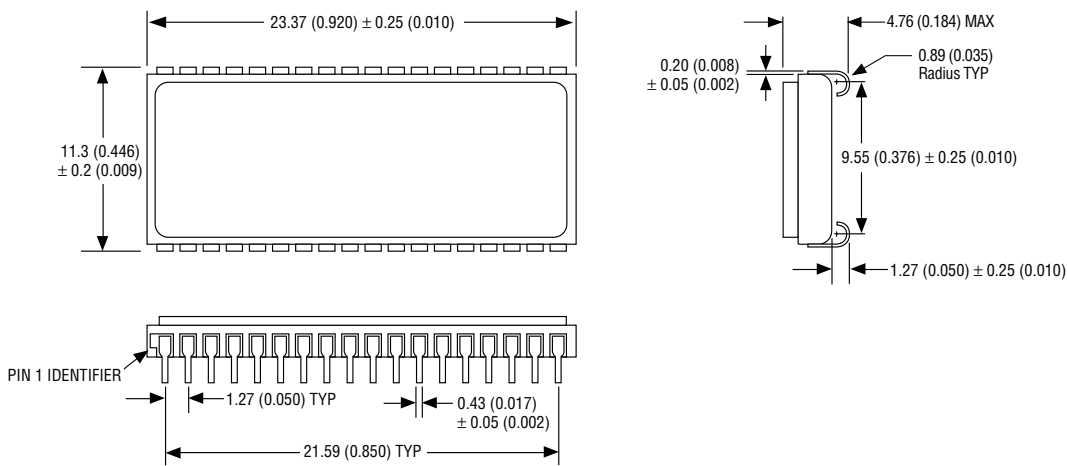


WRITE CYCLE - \overline{CS} CONTROLLED



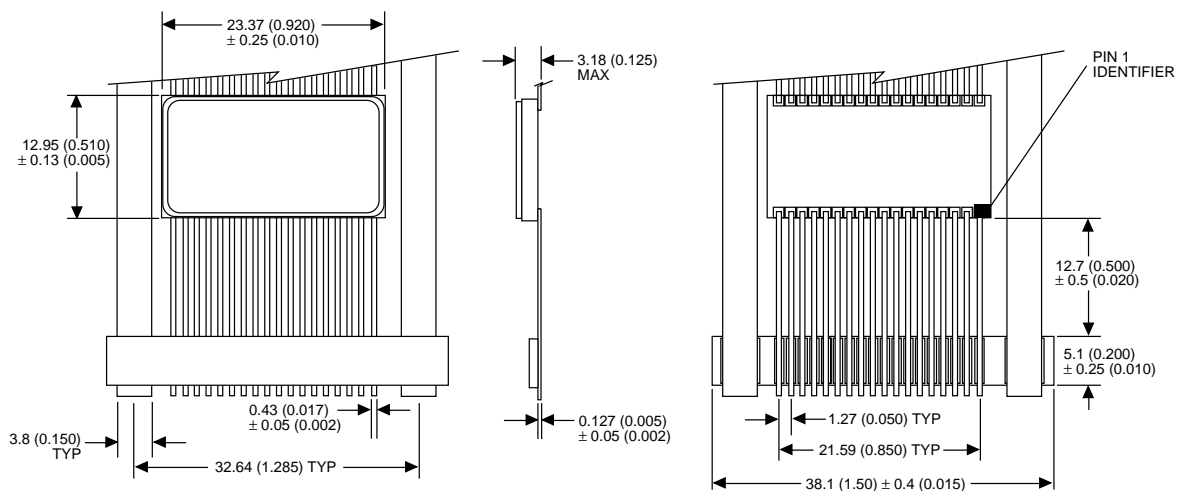


PACKAGE 100: 36 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

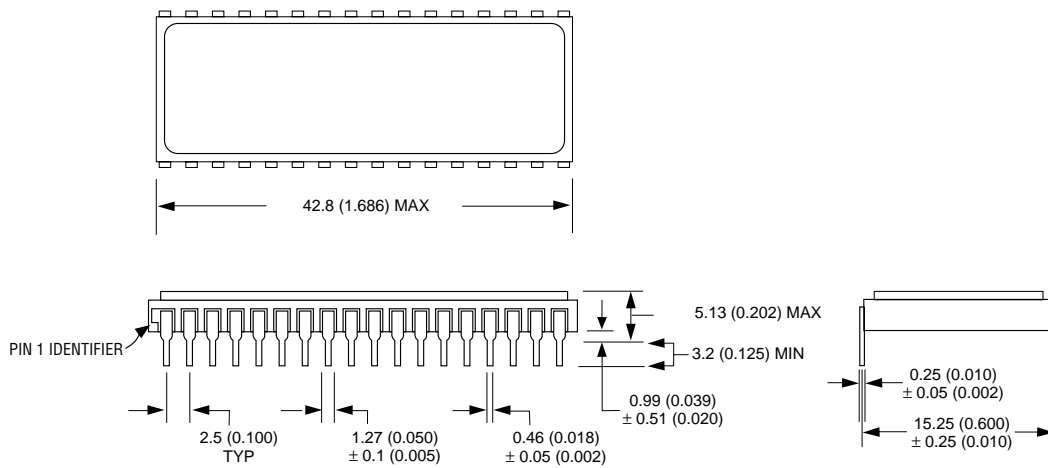
PACKAGE 226: 36 LEAD, CERAMIC FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S 1M8 X - XXX X X X

LEAD FINISH:

Blank = Gold plated leads
A = Solder dip leads

DEVICE GRADE:

M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE:

C = 32 pin Ceramic 0.600" DIP (Package 300)
DJ = 36 Lead Ceramic SOJ (Package 100)
F = 36 Lead Ceramic Flatpack (Package 226)

ACCESS TIME (ns)

IMPROVEMENT MARK:

Blank = Standard Power
L = Low Power Data Retention

ORGANIZATION, two banks of 512K x 8

SRAM

WHITE ELECTRONIC DESIGNS CORP.