VV5410

Mono and Colour Digital Video CMOS I

The VV5410/VV6410 are multi format digital output imaging devices based on STMicroelectronics's unique CMOS sensor technology. Both sensors require minimal support circuitry.

VV5410 (monochrome) and VV6410 (colourised) produce digital video output. The video streams from both devices contain embedded control data that can be used to enable frame grabbing applications as well as providing input data for the external exposure controller.

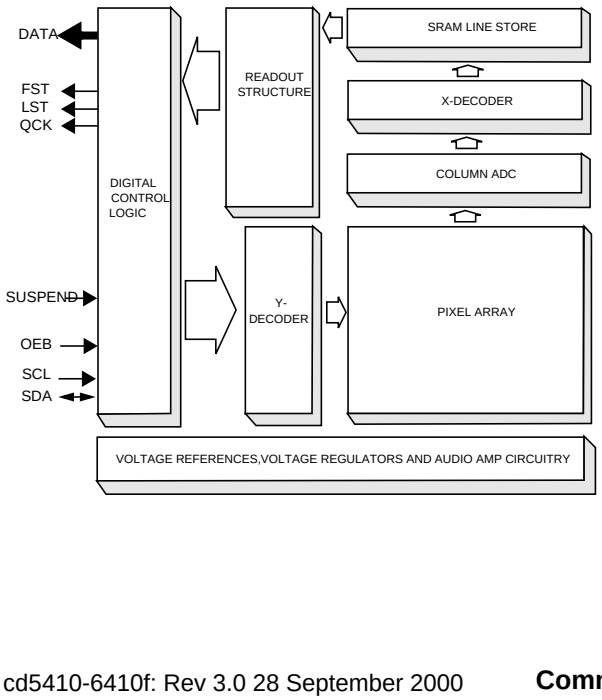
The pixel array in VV6410 is coated with a Bayer colour pattern. This colourised sensor can interface to a range of STMicroelectronics co-processors. A chipset comprising VV6410 and STV0657 will output 8bit YUV or RGB digital video. A USB camera can be realised by partnering VV6410 with STV0672. Finally a high quality digital stills camera can be produced by operating VV6410 with STV0680B-001. Please contact STMicroelectronics for ordering information on all of these products.

Both VV5410 and VV6410 are initialised in a power saving mode and must be enabled via I2C control before they can produce video. The I2C allows the master coprocessor to reconfigure the device and control exposure and gain settings.

USB systems are catered for with an ultra low power, pin driven, suspend mode.

The on board regulator can supply sufficient current drive to power external components, (e.g. the video coprocessor).

Functional block diagram



Key Features

- 3.3V operation
- Multiple video formats available
- Pan tilt image feature
- Sub sampled image full FOV featur
- On board 10 bit ADC
- On board voltage regulator
- Low power suspend mode for USB
- Automatic black and dark calibratio
- On board audio amplifier
- I2C communications

Applications

- PC camera
- Personal digital assistant
- Mobile video phones
- Digital stills cameras

Specifications

Effective image sizes after colour processing	352 x 288 176 x 144
Pixel resolution	up to 356
Pixel size	7.5µm x 6
Array size	2.73mm x
Exposure control	+81dB
Analogue gain	+12dB (re
SNR	c.56dB
Random Noise	1.17mV
Sensitivity (Green channel)	2.1V/lux.s
Dark Current	46mV/sec
VFPN	1.2mV
Supply voltage	3.0V- 6.0V
Supply current	26.2mA (r 85µA (sus
Operating temperature (ambient)	0^{o}C - 40^{o}C
Package type	36pin CLC

Table of Contents

1. Document Revision History

Revision	Date	Comments
1.0	13/06/2000	• Original release
2.0	06/07/2000	• Package drawing and pin description updated • Optical characterisation data added • Audio description extended • Pixel defect specification added • Product numbering updated • Reference design for BGA packaged 410 added • Gain ceiling recommendation
2.1	04/09/2000	• Remove all reference to BGA package option
3.0	28/09/2000	• Product maturity moves to Mat29 therefore d/s moves to

Table 1 : Document Revision History

2. Introduction

2.1 Overview

VV5410/VV6410 is a CIF format CMOS image sensor. The VV5410 sensor is the basic monochrome device colourised variant. The operation of VV5410 and VV6410 is very similar but any differences will be identified

VV6410 can output digital colourised pixel data at frame and line rates compatible with either NTSC or PAL VV5410 and VV6410 contain the same basic video timing modes. Table 2 summarises these video modes.

The various operating modes are detailed in Section 3.

Important: VV5410 and VV6410's output video data stream only contains raw data. A master co-processor generate a video waveform that can be displayed on a VDU

Mode	Input Clock (MHz)**Note**	System Clock Divisor	Image Size	Line Time (µs)	Lines per Frame
QCIF - 25 fps	8.00	8	180 x 148	250.00	160
QCIF - 30 fps	8.00	8	180 x 148	208.00	160
QCIF - 60 fps	16.00	8	180 x 148	104.00	160
CIF - 25 fps	16.00	4	356 x 292	125.00	320
CIF - 30 fps	16.00	4	356 x 292	104.00	320
NTSC (3.2 fsc)	28.636360 / 2.5	2	306 x 244	63.555564	525
PAL (3.2 fsc)	35.46895 / 2.5	2	356 x 292	63.999639	625

Table 2 : Video Modes

Note: The user can also provide a 24 MHz clock, rather than a 16 MHz clock, for the QCIF-60fps, CIF-25fps modes, which the sensor then internally divides by 1.5, (see data_format[22]), to give an effective input clock MHz.

2.2 Exposure Control

VV5410/VV6410 does not include any form of automatic exposure and/or gain control. Thus to produce a co image the integration period for the pixels, in the sensor array, an exposure control algorithm must be impler The new exposure values are written to the sensor via the serial interface.

2.3 Digital Interface

The sensor's offers a very flexible digital interface, the main components of which are listed below:

1. A tri-stateable 5-wire data bus (D[4:0]) for sending both video data and embedded timing references.
2. 4-wire and 8-wire data bus alternatives available. If the 8-wire option is selected then the FST/LST pins output data information.
3. A data qualification clock, QCK, which can be programmable via the serial interface to behave in a numb (Tri-stateable).
4. A line start signal, LST (Tri-stateable).
5. A frame start signal, FST (Tri-stateable).
6. OEB tri-states all 5 data bus lines, D[4:0], the qualification clock, QCK, LST, FST and D[7].
7. A 2-wire serial interface (SDA,SCL) for controlling and setting up the device.

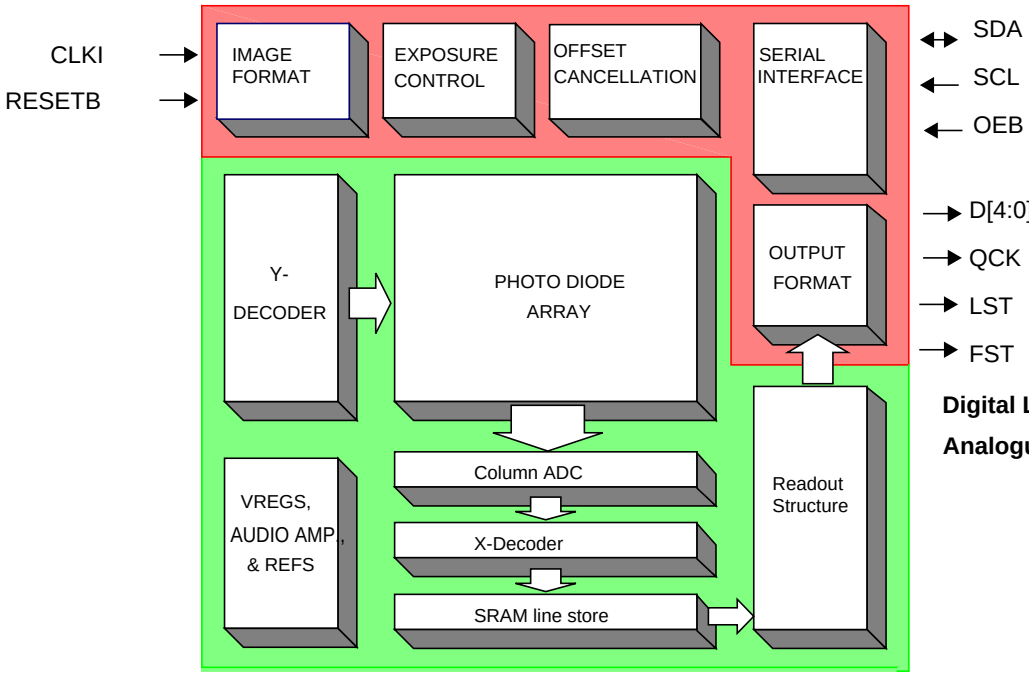


Figure 1 : Block Diagram of VV5410/VV6410 Image Sensor (5-wire output)

2.3.1 Digital Data Bus

Along with the pixel data, codes representing the start and end of fields and the start and end of lines are em video data stream to allow a co-processor to synchronise with video data the camera module is generating. S format for the output video data stream.

2.3.2 Frame Grabber Control Signals

To complement the embedded control sequences the data qualification clock (QCK), the line start signal (LS signal (FST) signals can be independently set-up as follows:

1. Disabled
2. Free-running.
3. Qualify only the control sequences and the pixel data.
4. Qualify the pixel data only

There is also the choice of two different QCK frequencies where one is twice the frequency of the other.

1. Fast QCK: the falling edge of the clock qualifies every 8, 5 or 4 bit blocks of data that makes up a pixel
2. Slow QCK: the rising edge qualifies 1st, 3rd, 5th, etc. blocks of data that make up a pixel value while th fies the 2nd, 4th, 6th etc. blocks of data. For example in 4-wire mode the rising edge of the clock qualifi cant nibbles while the falling edge of the clock qualifies the least significant nibbles.

2.3.3 2-wire Serial Interface

The 2-wire serial interface provides complete control over sensor setup and operation. Two serial interface b are supported. One allows all sensors to be written to in parallel while the other allows all sensors and co-proc to in parallel.

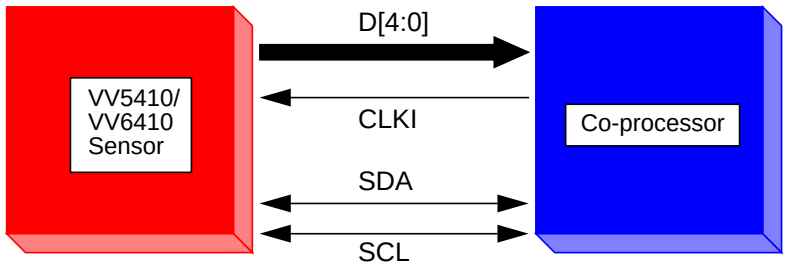
Section 9. defines the serial interface communications protocol and the register map of all the locations whic via the serial interface.

2.3.4 Sensor/Co-processor Interface Options

There are 3 main ways of interfacing to the VV5410/VV6410 sensor based on the above signals:

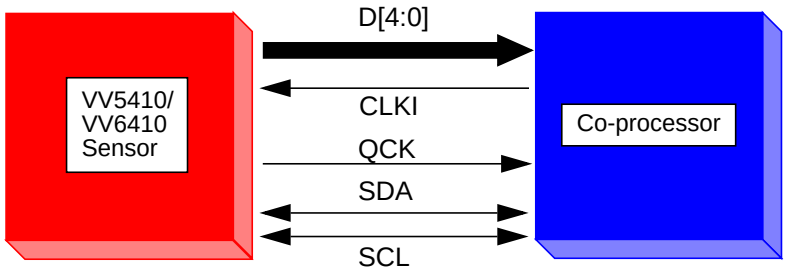
1. The colour co-processor supplies the sensor clock, CLKI, and uses the embedded control sequences t the frame and line level timings. Thus the host and sensor are running off derivatives of the same funda allow the co-processor to determine the best sampling position of the video data, during its power-up s outputs a 101010... sequence on each of its data bus lines for the host to lock on to.

1.



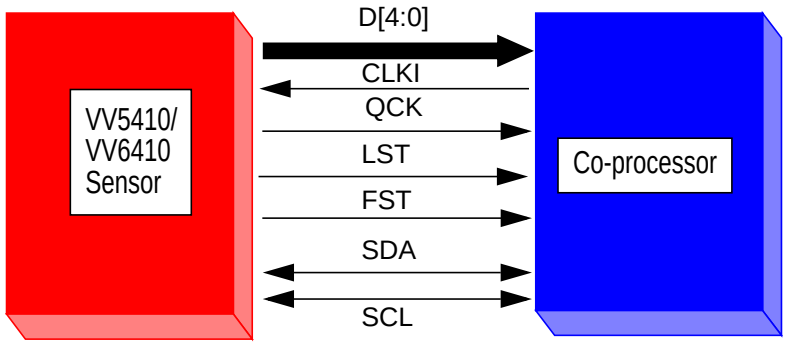
2. The colour co-processor supplies the sensor clock, CLKI, and uses a free-running QCK supplied by the the incoming video data stream. The embedded control sequences are used to synchronise the frame a

2.



3. The colour co-processor supplies the sensor clock, CLKI, and uses FST, LST and the data only mode f nise to the incoming video data. Primarily intended for interfacing to frame grabbers.

3.



2.4 Other Features

2.4.1 Audio Amplifier

Pins AIN and AOUTP & AOUTN are the input and outputs respectively for an audio amplifier.

2.4.2 Voltage Regulator

The on-chip voltage regulator requires only a few external components to form a fully functional voltage regu

2.4.3 Serial Interface Programmable Pins

The FST and QCK pins are re-configurable to follow the state of 2-bits in a serial register. The user could the
bits to control a peripheral device, a motor or shutter mechanism for example.

3. Operating Modes

3.1 Video Timing

The video format mode on power-up is CIF 30fps by default. After power-up the mode can be changed by a write to the *video_timing* register. The frame/field rate is also programmable via the serial interface. Bit [3] of selects between 30 and 25 frames per second for the CIF modes and 60/50 fields per second for the Digital modes. Please note that the sensor can exit low power in ANY of the available video modes.

The number of video lines in each frame is the same (320) for both the CIF modes. The slower frame rate (25 by simply extending the line period from 416 pixel periods to 500 pixel periods.

Table 3 details the setup for each of the video timing modes. A serial write to serial register [16] will force the registers in the serial interface to change to the appropriate values, regardless of their present state. If for ex data output mode is required than the default for a particular video mode, a write to the appropriate register a changed will restore the desired value.

Video Mode	Clock (MHz)	System Clock Divisor	Video Data	Line Length	Field Length
PAL (3.2 fsc)	28.636360 / 2.5	2	356 x 292	454	312/313
NTSC (3.2 fsc)	35.46895 / 2.5	2	306 x 244	364	262/263
CIF - 25 fps	16.0	4	356 x 292	500	320
CIF - 30 fps	16.0	4	356 x 292	416	320
QCIF - 25 fps	8.0	8	180 x 148	250	160
QCIF - 30 fps	8.0	8	180 x 148	208	160
QCIF - 60 fps	16.0	8	180 x 148	208	160

Table 3 : Video Timing Modes

3.1.1 Arbitration registers

When the operating video mode is changed a number of serial registers are forced into new states. The com follows:

Arbitrated feature	Video mode selected/value automatically programmed						
	PAL	NTSC	CIF 25fps	CIF 30fps	PTQCIF 25fps	PTQCIF 30fps	S
line length	453	363	499	415	249	207	
field length	311	261	319	319	159	159	
system clock division	2	2	4	4	8	8	
free running qck**note1**	yes	yes	no	no	no	no	
extra black lines**note2**	yes	yes	no	no	no	no	

Table 4 : Arbitration registers

note1: The free running qck, slow by default, is enabled by writing 8'h04 to serial register [20].

note2: The contents of the extra black lines are enabled on to the data bus by setting bit [5] of serial register [
register [24] is reset, indicating that the preferred coprocessor device is not the VP3 device, (a STMicroelectr
then the extra black lines are enabled by default regardless of the basic video mode selected.

The registers that control the image position within the pixel array and also the order in which the pixels are
been included in the table as their values are subject to a secondary series of registers. We will discuss the fo
and 2.3.

3.1.2 Input Clock Frequencies

It is recommended that a 16 MHz clock is used to generate CIF-25fps,CIF-30fps and QCIF-60fps and that an
to generate QCIF-25fps and QCIF-30fps, however the sensor can adapt to a range of other input frequencie
the required frame rates. For example, a 24 MHz clock can be used to generate CIF-30fps. By setting bit [7] o
the sensor can automatically divide the incoming clock by 1.5 by setting bit [7] of serial register [22], such tha
generator logic will still receive a 16 MHz clock.

Note that the clock division register is internally an 8 bit value, although the user may only program the lowe
nibble is reserved for setting the clock divisor as we change between primary video modes. The lower nibble
to reduce the effective frame rate within each video mode.

The system clock divisor column in Table 5 assumes that the programmable pixel clock divisor is set to the
implementing a divide by 1 of the internal pixel clock. Consider the following scenario where a user requires 1
image. As can be seen there are a wide range of options to achieve the same result.

clk in (MHz)	Divide by 3/2 enabled?	System clock divisor	Pixel clock divisor	pclk (MHz)	F
8	no	4	1	2	
12	yes	4	1	2	
16	no	4	2	2	
24	yes	4	2	2	

Table 5 : System clock divisor options

3.2 Pixel Array

The physical pixel array is 364 x 296 pixels. The pixel size is 7.5 µm by 6.9 µm. The image size for NTSC is 3
PAL and CIF it is 356 x 292 pixels, while for the QCIF modes the image size is 180 x 148 pixels. The remain
columns on each side of the PAL image size prevent columns 1 and 2 in PAL/CIF modes from being distorted
which occur when a pixel is close to the outer edge of the physical pixel array. Please note that these columns
part of the visible image if the user is operating the sensor in the pantilt QCIF mode.

Figure 3 shows how the 306 x 244 and 180 x 148 sub-arrays are aligned within the bigger 364 x 296 pixel ar
colourisation pattern requires that the top-left corner of the pixel sub-array is always a Green 1 pixel. To pres
colour pattern the NTSC sub-array has been offset relative to the centre of the array. The QCIF size images
orientated.

Image read-out is very flexible. Sections 3.3.2 - describe the options available to the user. By default the se
configured to be horizontally 'shuffled' non-interlaced raster scan. The horizontally 'shuffled' raster scan orde
conventional raster in that the pixels of individual rows are re-ordered, with the odd pixels within a row read-
the even pixels. This 'shuffled' read-out within a line, groups pixels of the same colour (according to the Baye
together, reducing cross talk between the colour channels. This option is on by default and is controllable via
The horizontal shuffle option would normally only be selected with the colour sensor variant, VV6410.

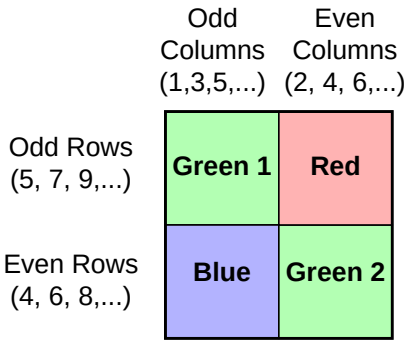


Figure 2 : Bayer Colourisation Pattern (VV6410 only)

3.3 X-offset and Y-offset

The image information is retrieved from the pixel array via a 2 dimensional address. The x and y address bus starting point described by x-offset, y-offset up to a maximum count in x and y that is determined by the imag this count and the count step size is dependent upon the special image format parameters described below. of the x and y address counters is entirely handled by the sensor logic

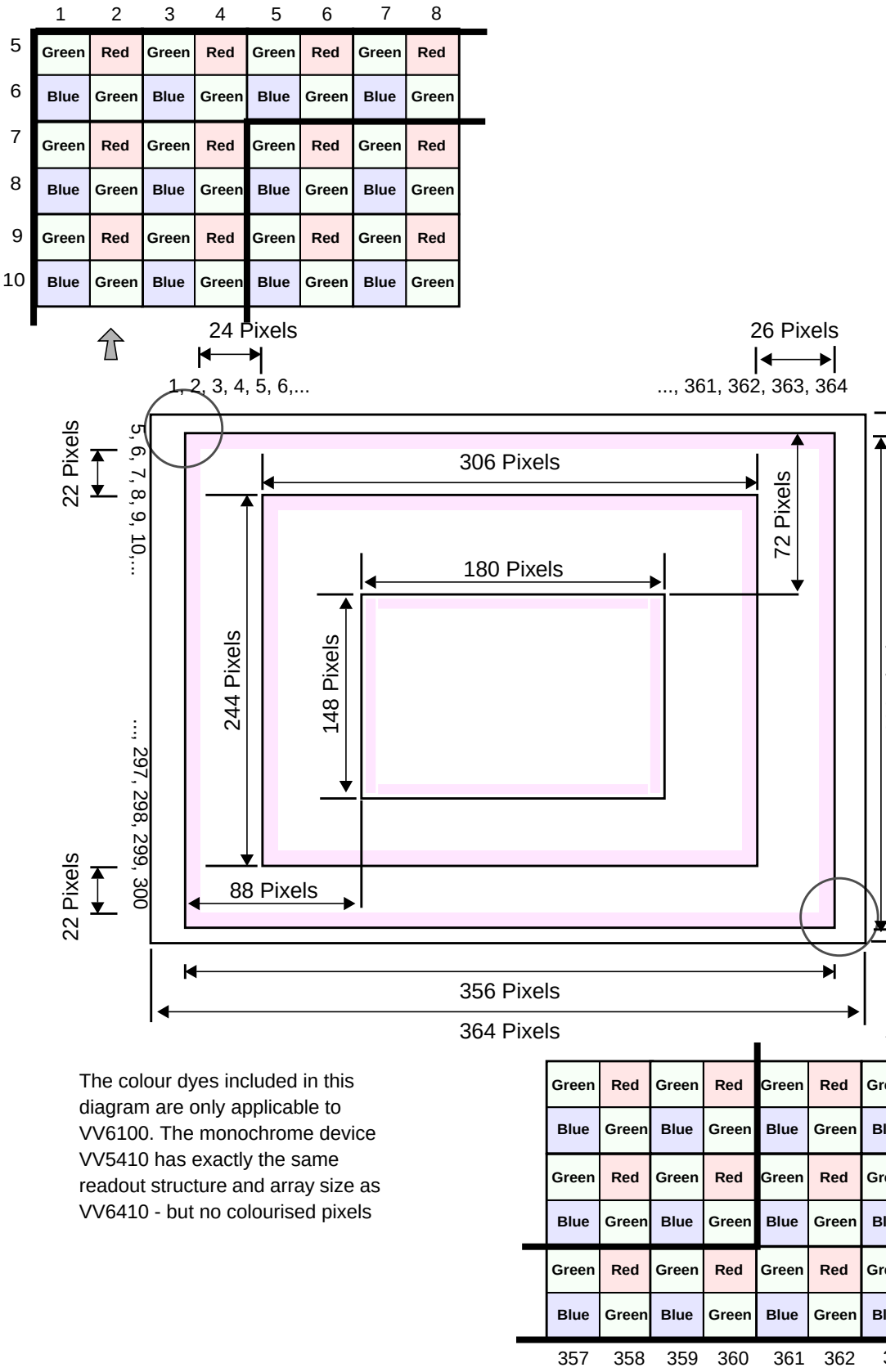
As can be seen in Figure 3 the visible array size is 364 columns by 296 rows. The PAL and CIF images are by 292 rows, thus we have a “border” of visible pixels that we do not read out if either of these modes are se

The images that are read out of the sensor are always “centred” on the array, therefore we allow a border of end of the image in the x-direction and a border of 2 rows at the top and bottom of the image in the y-directio and NTSC video modes are similarly centred within the full size array.

For all the modes except the pantilt QCIF the x and y offset coordinates are fixed. If the user selects the pan they may specify x and y-offsets in the range:

- (xoffset >= 1) and (xoffset <= 185)
- (yoffset >= 5) and (yoffset <= 149)

The sensor will automatically clip values outwith the specified ranges. The y addresses less than 5 are reser black lines and the y address greater than 296 are reserved for the sensor dark lines. Neither the black lines contain visible image data



The colour dyes included in this diagram are only applicable to VV6100. The monochrome device VV5410 has exactly the same readout structure and array size as VV6410 - but no colourised pixels

Figure 3 : Image Readout Formats

3.3.1 Image readout parameters

The following parameters are available to process the sensor readout:

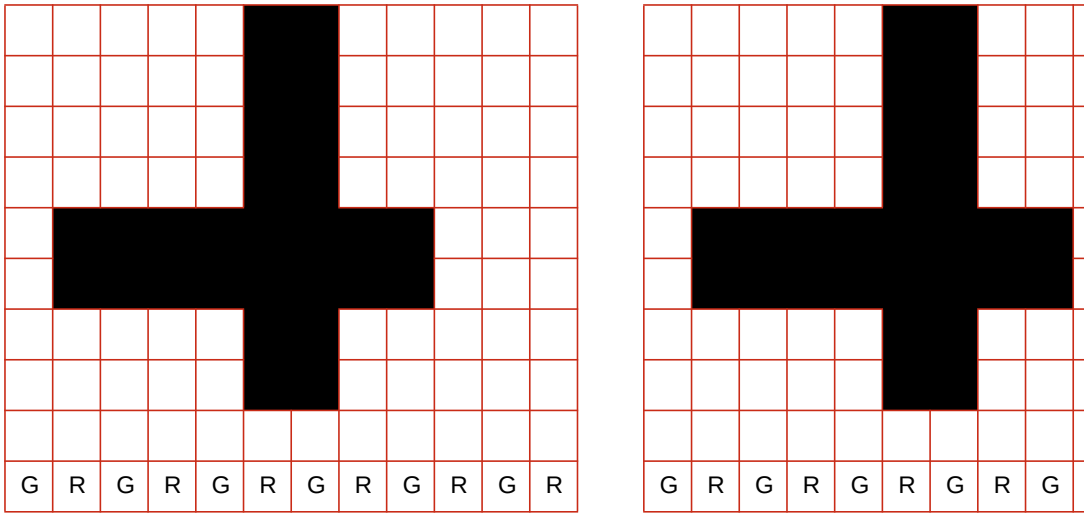
- Shuffle horizontal readout, enabled by setting bit [7] of serial register [17]
- Mirror horizontal readout, enabled by setting bit [3] of serial register [22]
- Shuffle vertical readout, enabled by setting [2] or serial register [22]
- Flip vertical readout, enabled by setting [4] of serial register [22]

The effect of each of these parameters is probably best described via a series of diagrams, see sections 3.3

Although all the above features may be used in conjunction with one another we will only display one specia parameter at any one time.

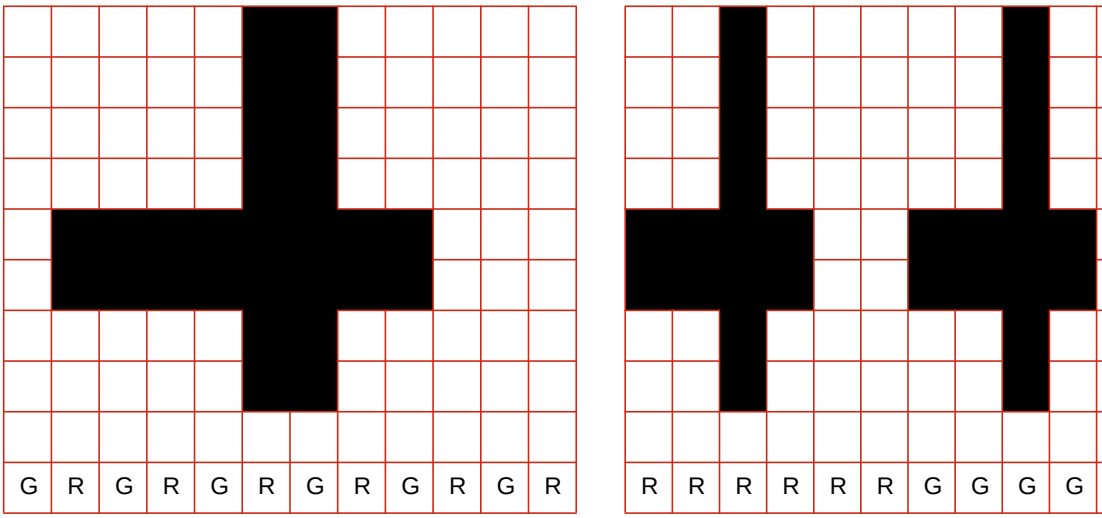
3.3.2 Horizontal shuffle

Figure 5 is the reference figure that shows the image readout without any of the optional image parameters, selected. Figure 5 shows how the image will appear if the horizontal shuffle bit has been selected. Note that (column 2,4,6 etc), are read out first followed by the odd columns, (1,3,5,7 etc).‘



Where G - Green and R - Red

Figure 4 : Standard Image Readout

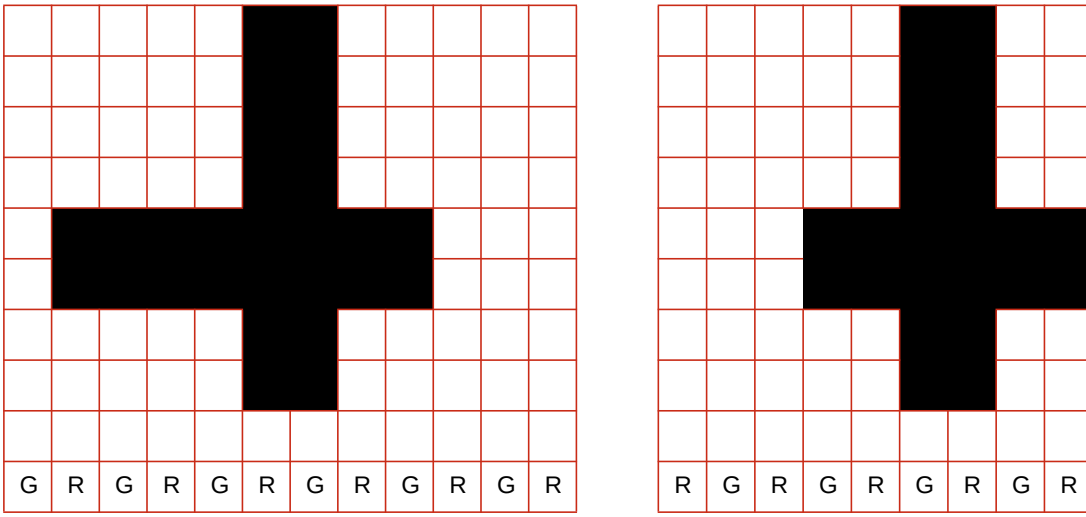


Where G - Green and R - Red

Figure 5 : Horizontal Shuffle Enabled

3.3.3 Horizontal mirror

Figure 6 shows the output image with the horizontal mirror feature enabled. Note that the columns are read



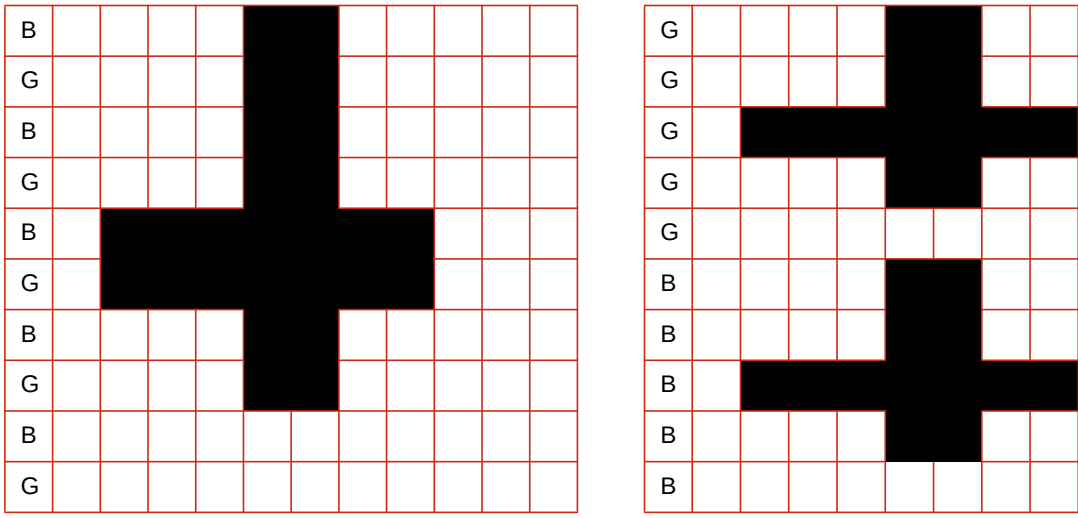
Where G - Green and R - Red

Figure 6 : Horizontal mirror enabled

3.3.4 Vertical Flip

Figure 7 shows the output image with the vertical flip feature enabled. Note that the even rows (rows 2,4,6 et

followed by the odd rows, (rows 1,3,5 etc)

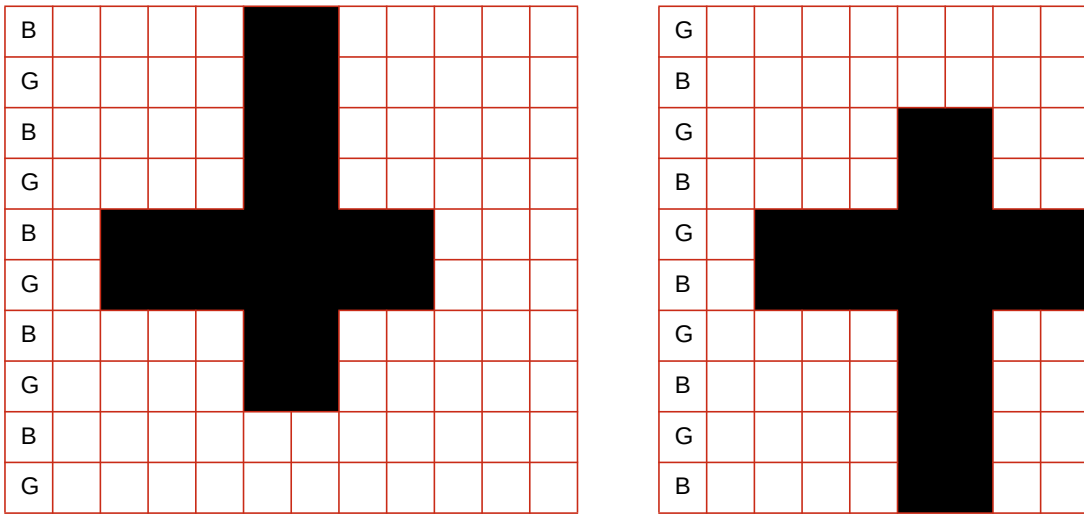


Where G - Green and B - Blue

Figure 7 : Vertical Shuffle enabled

3.3.5 Vertical Flip

Figure 3.4 shows the output image with the vertical flip feature enabled. Note that the rows are read out in re



Where G - Green and B - Blue

Figure 8 : Vertical Flip enabled

3.4 QCIF Output Modes

VV5410/VV6410 has two QCIF output modes, pan/tilt QCIF (ptQCIF) and sub sampled QCIF (ssQCIF), both same output format. The data contained within the active QCIF image differs between the sub sampled and the QCIF mode contains a quarter of the data of the CIF mode, the effective pixel clock can be run at a quar means that in CIF mode a system clock of 16MHz will produce a field rate of 30fps, whereas in QCIF mode a 8MHz is required to produce the same field rate. Note that the sensor divides the system clock internally by 4 for QCIF mode. If the user supplied the sensor with a 16Mhz system clock and selected QCIF mode then a f possible.

3.4.1 Pan/Tilt QCIF

In this mode the QCIF image is generated by outputting a cropped portion of the CIF image as illustrated in pan-tilt QCIF video mode is initially selected the image will be horizontally and vertically justified in the within (364 pixels by 292 pixels). The coordinates which define the top left corner of the QCIF portion of the array t defined by the x-offset & y-offset parameters in serial registers [88 - 91] inclusive.

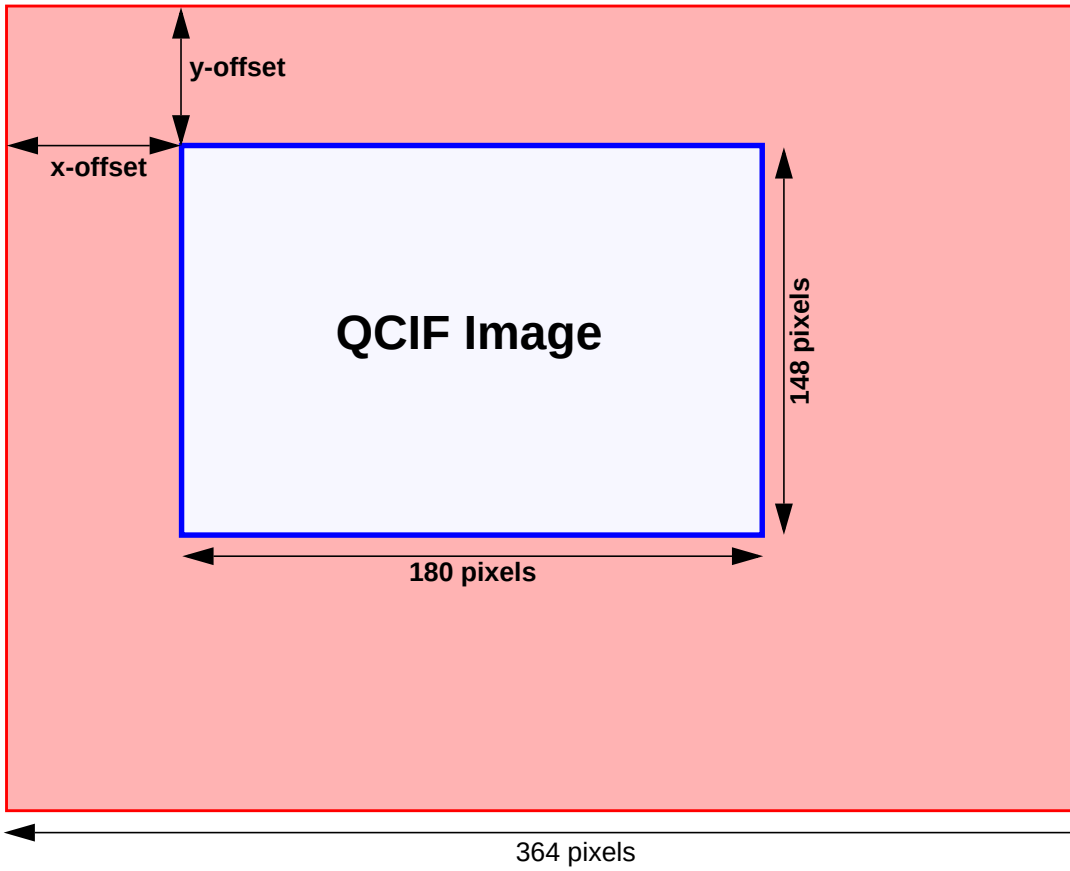


Figure 9 : Pan/Tilt QCIF Image Format

The x-offset and y-offset parameters are subject to minimum and maximum values which are set according t mode (horizontal shuffle etc). Any clipping (against a maximum) or clamping (against a minimum) will be auto by the sensor logic. Regardless of whether any of the shuffle/mirror modes have been selected the user sho the top left corner coordinates as the x-offset and y-offset. To preserve the Bayer pattern at the sensor output of the image should always be green followed by red. If the x or y offsets are adjusted by a single step, i.e. adj n to n+1, then this pattern will be corrupted. The user should always write an **odd** number to the x and y offs will preserve the Bayer pattern. The 5410, monochrome sensor is unaffected by such an adjustment to the x-o the pixels do not contain any colour information.

3.4.2 Sub-Sampled QCIF

In this mode the QCIF image is generated by sub-sampling the CIF image in groups of 4 to preserve the Baye
second group of pixels & lines skipped as illustrated in Figure 10. Although the former would not necessarily
monochrome sensor the same address sequence is preserved. VV5410 users should ignore the colour refer
Due to the crude nature of the sub-sampling, the resultant output image will be of inferior quality but contains
is intended for use in gesture recognition applications or perhaps as a preview option before switching to pa
view the required scene region in more detail.

Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green
Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green
Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green
Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green

Bayer Colourised Pixel Array

Green	Red			Green	Red			Green	Red		
Blue	Green			Blue	Green			Blue	Green		
Green	Red			Green	Red			Green	Red		
Blue	Green			Blue	Green			Blue	Green		

Sub-Sampled Bayer Colourised Pixel Array

Figure 10 : Sub-Sampled QCIF Image Format

4. Black Offset Cancellation

In order to produce a high quality output image from VV6410 it is important to maximise the dynamic range o
This can be achieved by accurately controlling the video signal black level. Within the sensor array of VV6410
of lines that are specified to be black, that is they are exposed to the incident light but they are always held in
VV6410 also has a number of dark lines, that is lines that are integrated for the same length of time as the vi
pixels within these dark lines are shielded from incident light by an opaque material (e.g. metal 3). The diagr
where the different types of lines that appear within the full array.

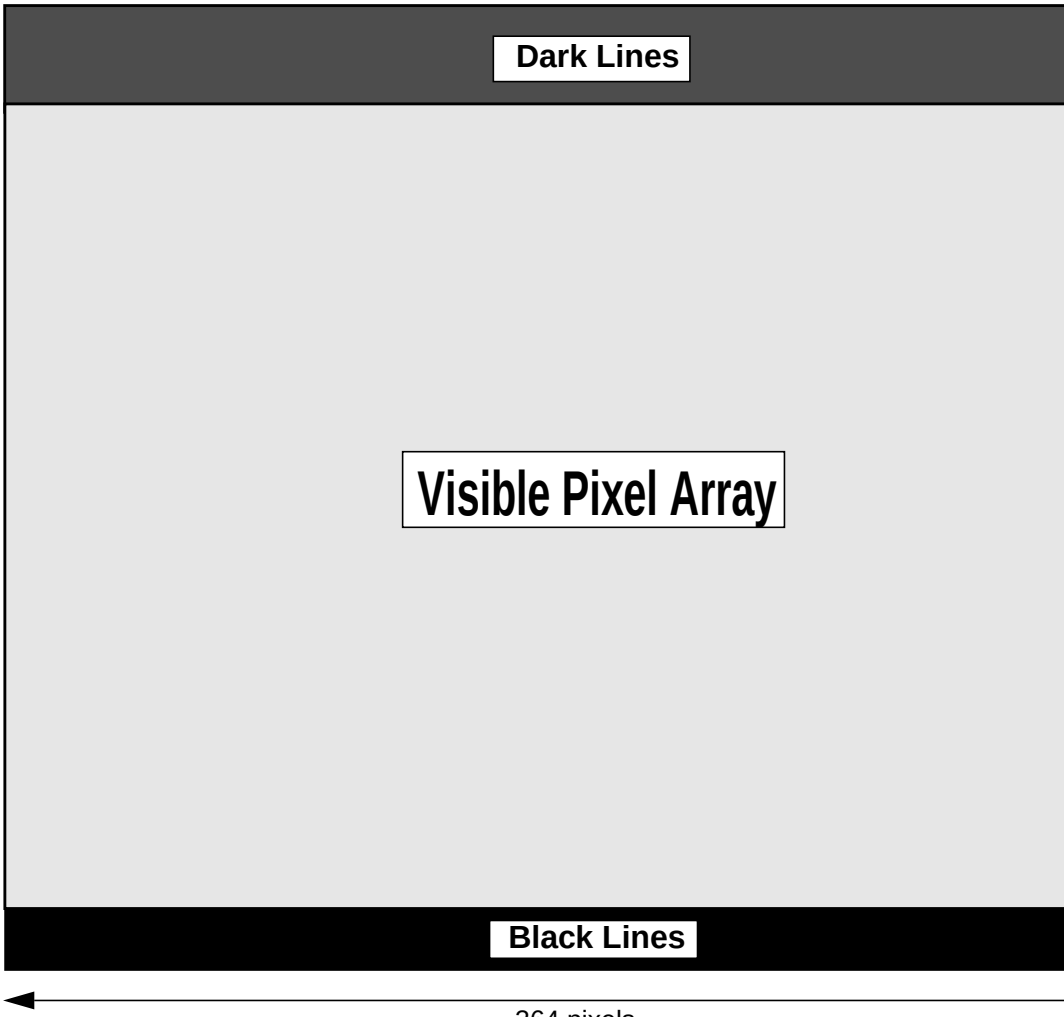


Figure 11 : Physical position of Black and Dark Lines

VV5410/VV6410 can perform automatic black offset cancellation. VV5410/VV6410 contains an algorithm tha
of the designated black pixels and applies a correction factor, if required, to provide an ideal black level for th

The user can control the application of the offset cancellation parameter. The internally calculated offset can
video stream or alternatively an externally calculated offset can be applied or finally there is the option of app
Details of how to select the aforementioned modes can be found in subsubsection 9.5.5.

The black offset cancellation algorithm accumulates data from the centre 2 of the 4 physical black lines. The
algorithm uses a leaky integrator model to control the size of the calculated offset. The leaky integrator mode
current offset plus a shifted version of the error between the ideal black level and the current offset. The mag
the error is programmable. It is also possible to control the range of pixel values that will inhibit a change in th
A narrow band (128 +/- 2 codes) or a wide band (128 +/- 4 codes) can be selected. If the latter is selected ar

returned in the current field lies between 124 and 132 then the offset cancellation will remain unchanged.

Following a gain change, or when exitting low-power, sleep or suspend modes, the internal (19bit) offset reg
the default resulting in an automatic black offset of -64.

5. Dark Offset Cancellation

VV5410/VV6410 performs dark line offset cancellation as well as black line offset cancellation. A dark line is incident light by an opaque material such as metal 3 (as an example) but these lines will be exposed to incide length of time as the visible pixels. If the dark pixels are completely shielded from light then no incident light pixels and the pixels will produce the same digital code as the black pixels, i.e. 128 internally (therefore 64 e algorithm used to calculate the dark offset cancellation is identical to that used to calculate the black offset ca the dark algorithm does assume that the dark pixels have already been black corrected therefore the target thus the dark offset cancellation is 0 by default.

The dark offset cancellation algorithm is configured by the dark offset cancellation setup register, [46], see su The only parameter in this that is different from the corresponding table that configures the black offset canc the control bit, [bit2], that determines the number of dark lines that are to be used by the cancellation algorith select half of the total number of available dark lines to be used to calculate the dark offset cancellation settin is selected the dark lines used by the algorithm are always preceeded by another dark line, thereby giving ex damaging edge effects that may occur on lines close to the edge of the shield material.

It should be noted that the black and dark offset cancellation are completely independent. For example it is p to select internal automatic black offset cancellation but to opt for no dark offset cancellation or indeed choose offset cancellation externally.

6. Exposure Control

6.1 Calculating Exposure Period

The exposure time, comprising coarse and fine components, for a pixel and the analogue gain are programm interface.

The coarse exposure value sets the number of complete lines a pixel exposes for, while the fine exposure se additional pixel clock cycles a pixel integrates for. The sum of the two gives the overall exposure time for the

Exposure Time = ((Coarse setting x Line Period) + (Fine setting)) x (CLKI clock period) x Clock Divider Ratio

note1: Clock Divider Ratio = 1/(Basic Clock Division * Optional Pixel Clock Divisor)

Default Clock Divider Ratio as follows: (Optional Pixel Clock Divisor = 1)

- PAL/NTSC - 1/2
- CIF - 1/4
- QCIF - 1/8

The maximum coarse and fine exposure settings are a function of the field and line lengths respectively. The exposure is current field length - 1 and the maximum fine exposure is current line length - fixed offset, see be value is requested that is beyond the maximum then the applied exposure setting will be clipped to the curre

Video Mode	Fine Exposure Offset (pck's)
NTSC	51
PAL	86
CIF	51
QCIF	23

Table 6 : Fine Exposure Offset

The current revision of VV5410/VV6410 in the following modes of operation:

VP3 mode (OFF), QCIF and PAL (Video mode)

has an error in the application of coarse exposure. Please contact STMicroelectronics for more detail

6.2 Gain Components

The analogue gain in VV5410/VV6410 is programmed via the 8 bit gain register[36]. The analogue gain com components, capacitive gain, (set by the ms nibble), and current gain, (set by the ls nibble). It is strongly rec capacitive gain setting is left at the default value of 4'b1111. Table 7 details the available gain settings in 9bi and 10bit, (CIF or QCIF), modes. We assume that mode_select[24], bit1 is 0. gain[7:0] is the value programm The ls nibble of the gain value is limited to 4'he, with 4'hf not permitted.

10bit ADC mode				9bit ADC mode		
gain[7:0]	igain[3:0]	cgain[5:0]	Overall Gain	gain[7:0]	igain[3:0]	cgain[5:0]
8'hfe	1 (0001_2)	63	8.000	8'hfe	1 (0001_2)	31
8'hfd	2 (0010_2)	63	5.333	8'hfd	2 (0010_2)	31
8'fc	3 (0011_2)	63	4.000	8'fc	3 (0011_2)	31
8'hfb	4 (0100_2)	63	3.200	8'hfb	4 (0100_2)	31
8'hfa	5 (0101_2)	63	2.667	8'hfa	5 (0101_2)	31
8'hf9	6 (0110_2)	63	2.2857	8'hf9	6 (0110_2)	31
8'hf8	7 (0111_2)	63	2.0000	8'hf8	7 (0111_2)	31
8'hf7	8 (1000_2)	63	1.7778	8'hf7	8 (1000_2)	31
8'hf6	9 (1001_2)	63	1.6000	8'hf6	9 (1001_2)	31
8'hf5	10 (1010_2)	63	1.4545	8'hf5	10 (1010_2)	31
8'hf4	11 (1011_2)	63	1.3333	8'hf4	11 (1011_2)	31
8'hf3	12 (1100_2)	63	1.2308	8'hf3	12 (1100_2)	31
8'hf2	13 (1101_2)	63	1.1429	8'hf2	13 (1101_2)	31
8'hf1	14 (1110_2)	63	1.0667	8'hf1	14 (1110_2)	31
8'hf0	15 (1111_2)	63	1.0000	8'hf0	15 (1111_2)	31

Table 7 : Analogue Gain Settings

note: The relationship between the programmed gain value as written to register[36] and the igain (c cgain (capacitive gain) is as follows:

igain

If mode_select[24], bit 1 is set then igain[3:0] is the inverse of gain[3:0], i.e. if gain[3:0] = 6, igain[3:0] = 9.

If mode_select[24], bit 1 is reset then igain[3:0] is the inverse of the mirror of gain[3:0], i.e. bit 3 of igain is the gain, i.e. gain = 4 and igain = 13.

cgain

cgain is a 6 bit value therefore we have to pad the 4 bits of the gain register. In 10bit modes cgain[1:0] is fixe cgain[5:2] is set to gain[7:4]. In the 9bit modes cgain[1:0] is also set to 2'b11, however cgain[5:2] is set to ga thus gain[7:4] = 4'b1111 gives cgain[5:0] = 6'b011111.

6.2.1 Recommended Gain Settings

To ensure optimum sensor performance it is recommended that the igain setting, controlled by the ls nibble register[36_{10}], be limited to 12.

6.3 Clock Division

Although the clock divisor register is an 8 bit register the user only has write access to the lower 4 bits as de upper 4 bits of the register are altered automatically when the video mode is changed by writing to Setup0[16] 4 bits are pre-programmed as follows:

Video mode	Register[37], bits[7:4]	Effective system clock div
CIF	4'b0001	Divide CLKI/CLKIP by 4
QCIF	4'b0011	Divide CLKI/CLKIP by 8
PAL/NTSC	4'b0000	Divide CLKI/CLKIP by 2

Table 8 : System Clock Divisor Options

6.4 Updating Exposure, Gain and Clock Division Settings

Although the user can write a new exposure, gain or clock division parameter at any point within the field the consume these new external values at a certain point. The exceptions to this behaviour are when the user h immediate update of gain and clock division. If the user has selected the former then the new gain or clock d applied as soon as the serial interface message has completed. The fine and coarse exposure values are al "timed" manner. There are a number of "update pending" flags available to the user (see Status0 reg[2] for de user to detect when the sensor has consumed one of the timed parameters. In the next section of this docum the timed parameters and describe when they are updated.

It is important to realise that there is a 1 frame latency between a new exposure value being applied to the s results of this new exposure value being read-out. The same latency does not exist for the gain value. To ens the new exposure and gain values are coincident the sensor delays the application of the new gain value by frame relative to the application of the new exposure value.

If the user is using the autoincrement option in the serial interface when writing a new series of exposure/gai parameters then it is important to ensure that the sensor receives the complete message bunch before upda parameters. It is also important that the timed parameters are updated in the correct order, we will discuss th section. If an autoincrement message sequence is in progress but we have reached the point in the field timi value would normally be updated, we actually inhibit the update. We inhibit the update to ensure that the gai passed to the sensor while a change in the exposure is still pending.

7. Timed Serial Interface Parameters

The previous section, Exposure Control, introduced the concept of a “timed parameter”, that is information th serial interface but will not be used immediately by the sensor, rather there will be a delay before the informat internal registers (referred to as the working registers) from the serial interface registers (referred to as the sh the contents of the working registers that will determine sensor behaviour.

The architecture of VV5410/6410 requires that many of the programmable registers are handled in such a m will identify all these registers, describe what they are all used for and then go on to explain when they are a

7.1 Listing and Categorizing the Parameters

The timed parameters are split into 6 categories as follows:

- fine exposure
- coarse exposure
- clock division
- gain
- pan parameter
- tilt parameter
- video timing

There is a “pending” flag for each of the above categories. These flags are stored in Status0 Register[2]. If on this indicates that the working register/s controlled by that flag have yet to be updated from the according sha feedback information could be useful if a user is, for example, attempting to write an exposure controller. The pending flags allows accurate timing of the serial interface communications.

7.1.1 Fine Exposure

The fine exposure category simply comprises registers[32,33].

7.1.2 Coarse Exposure

The coarse exposure category simply comprises registers[34,35].

7.1.3 Clock Division

The clock division category simply comprises register[37].

7.1.4 Gain

The gain category simply comprises register[36].

7.1.5 Pan Parameter

The pan parameter category comprises the following registers:

- Setup0[16] (The “pan_pend” flag will only be set if the subsampled QCIF mode is entered or exited)
- Setup1[17] (The “pan_pend” flag will only be set if the hshuffle control bit is changing state)
- Data_format[22] (The “pan_pend” flag will only be set if the hmirror control bit is changing state)
- X-offset[87,88] (The “pan_pend” flag set unconditionally)

7.1.6 Tilt Parameter

The tilt parameter category comprises the following registers:

- Setup0[16] (The “tilt_pend” flag will only be set if the subsampled QCIF mode is entered or exited)
- data_format[22] (The “tilt_pend” flag will be set if the hshuffle control bit or the hmirror control bit is cha
- Y-offset[89,90] (The “tilt_pend” flag set unconditionally)

7.1.7 Video Timing Parameter

The video timing parameter category comprises all the other shadow/working register pairs. The video timing pending flag will be unconditionally set if any of the following registers are written to:

- Setup0[16]
- Setup1[17]
- fg_mode[20]
- data_format[22]
- op_format[23]
- mode_select[24]
- Dark Pixel Offset[44,45]
- Dark Pixel Cancellation Setup Register
- Black Pixel Offset[44,45]
- Black Pixel Cancellation Setup Register
- Line Length[82,83]
- Field Length[97,98]

7.2 Timed Parameter Update Points

The timed parameter categories are updated as follows:

note: We refer to odd and even fields in the Table 9 below. In a video mode like CIF or QCIF the fields are a we still have to be able to differentiate between fields to enable correct updating of register parameters.

Timed parameter category	Updated point
fine exposure	Conditional on a change pending in the line length register. ***Line length change pending***: update fine exposure at the odd transition ***Line length change not pending***: update fine exposure during active video (SAV) region of the end of frame (EOF) line (the line the last line of active video) in the odd field.
coarse exposure	Updated during the SAV region of the first dark line in an odd fie
clock division	Updated at the odd to even field transition
gain	Updated during the SAV region of the EOF line in the odd field
pan parameter	Updated during the SAV region of the EOF line in the odd field
tilt parameter	Updated during the SAV region of the first visible line in an odd
video timing	Updated at the odd to even field transition

Table 9 : Timed Parameter Update Points

The order that the above timed parameters are updated is critical. Let us assume that all the pending flags a written to at least one register in each category. The working registers will be updated in the following order:

1. Coarse exposure

2. Tilt parameters

3. Gain, Pan parameters and conditionally the fine exposure (see Table 9 for details)
4. Clock division, video timing parameters and conditionally the fine exposure (see Table 9 for details)

8. Digital Video Interface Format

8.1 General description

The video interface consists of a bidirectional, tri-stateable 5-wire data bus. The nibble transmission is synch
edge of the system clock (Figure 31).

Read-out Order	Progressive Scan (Non-interlaced)			
Form of encoding	Uniformly quantised, PCM, 8/10 bits per sample			
Correspondence between video signal levels and quantisation levels:	The internal10-bit pixel data is clipped to ensure that 0_H a Wire) or FF_H (4/8 Wire) values do not occur when pixel da output on the data bus.			
	10-Bit Data		8-Bit Data	
	Pixel Values	1 to 1022	Pixel Values	1 to
	Black Level	64	Black Level	16

Table 10 : Video encoding parameters

Digital video data may be either 8 or 10 bits per sample, and can be transmitted in one of the following ways

10-bit data

1. A series pair of 5-bit nibbles, most significant nibble first, on 5 wires.
2. An 8-bit number e.g. line code. line numbers and status line data is padded with 00 in the least significa up a 10-bit value.

8-bit data

1. A single 8 bit byte over 8 output wires**note**.
2. A series pair of 4-bit nibbles, most significant nibble first, on 4 wires.
3. The top 8-bits of a 10-bit value e.g. pixel data or line averages is used as the 8-bit equivalent.

note: if the 8-wire output mode has been selected then the normal FST/LST pin function is sacrificed as thes to output data information

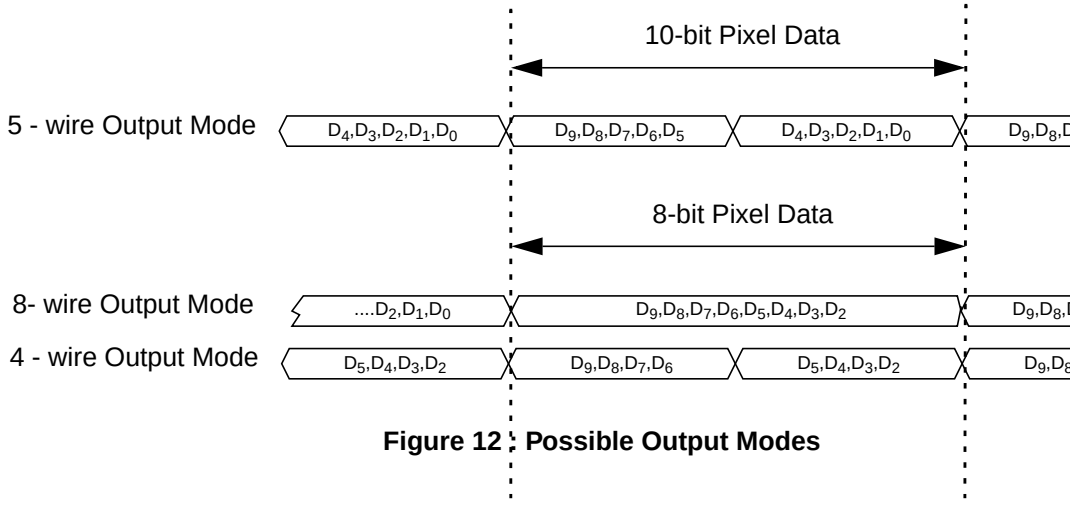


Figure 12 : Possible Output Modes

In the following description the 4-wire mode is used as an example. The 5-wire mode can be viewed as a va mode. Data is output on the least significant data wires available. e.g. in 4-wire mode, data is output on data

5-wire mode data is output on D[4:0].

Multiplexed with the sampled pixel data is control information including both video timing references, sensor data and the pixel average from the current line.

Video timing reference information takes the form of field start characters, line start characters, end of line ch counter.

Where hexadecimal values are used, they are indicated by a subscript H, such as FF_H; other values are dec

8.2 Embedded control data

To distinguish the control data from the sampled video data all control data is encapsulated in embedded co These are 6 bytes long and include a combined escape/sync character sequence, 1 control byte (the 'comm bytes of supplementary data.

To minimise the susceptibility of the embedded control data to random bit errors redundant coding techniques allow single bit errors in the embedded control words to be corrected. However, more serious corruption of c corruption of escape/sync characters cannot be tolerated without loss of sync to the data stream. To ensure t detected a simple set of rules has been devised. The four exceptions to the rules are outlined below:

1. Data containing a command word that has two bit errors.
2. Data containing two 'end of line' codes that are not separated by a 'start of line' code.
3. Data preceding an 'end of field' code before a start of frame' code has been received.
4. Data containing line that do not have sequential line numbers (excluding the 'end of field' line).

If the host detects one of these violations then it should abandon the current field of video

8.2.1 The combined escape and sync character

Each embedded control sequence begins with a combined escape and sync character that is made up of thr two of these are FF_H FF_H- constituting two words that are illegal in normal data. The next word is 00_H - guara signal transition that allows a host to determine the position of the word boundaries in the serial stream of nil escape and sync characters are always followed by a command byte - making up the four byte minimum em sequence.

8.2.2 The command word

The byte that follows the combined escape/sync characters defines the type of embedded control data. Thre used to carry the control information, four are 'parity bits' that allow the host to detect and correct a certain le transmission of the command words, the remaining bit is always set to 1 to ensure that the command word n 00_H. The coding scheme used allows the correction of single bit errors (in the 8-bit sequence) and the detect

The three data bits of the command word are interpreted as shown in Figure 13.The even parity bits are bas relationships:

1. An even number of ones in the 4-bit sequence (C_2, C_1, C_0 and P_0).
2. An even number of ones in the 3-bit sequence (C_2, C_1, P_1).
3. An even number of ones in the 3-bit sequence (C_2, C_0, P_2).
4. An even number of ones in the 3-bit sequence (C_1, C_0, P_3).

Table 13 shows how the parity bits maybe used to detect and correct 1-bit errors and detect 2-bit errors.

8.2.3 Supplementary Data

The last 2 bytes of the embedded control sequence contains supplementary data. The are two options:

1. The last 2 bytes of the SAV 6 byte sequence contain the current 12-bit line number. The 12-bit line num by splitting it into two 6-bit values. Each 6-bit value is then converted into an 8-bit value by adding a zer odd word parity bit at the end.
2. The 5th byte of the EAV sequence contains a pixel average for that line either based upon the middle 2 CIF,PAL or NTSC video modes are selected or the middle 128 pixels if the QCIF video mode is selected FF_H.

Note: in 5-wire mode, the embedded control data is calculated as detailed above and output as the most sig least significant 2-bits are padded with zero.

Line Code	Nibble X_H (1 C_2 C_1 C_0)	Nibble Y_H (P_3 P
End of Line	1000_2 (8_H)	0000_2 ($0_$
Blank Line (BL)	1001_2 (9_H)	1101_2 ($D_$
Black line (BK)	1010_2 (A_H)	1011_2 ($B_$
Visible Line (VL)	1011_2 (B_H)	0110_2 ($6_$
Start of Even Field (SOEF)	1100_2 (C_H)	0111_2 ($7_$
End of Even Field (EOEF)	1101_2 (D_H)	1010_2 ($A_$
Start of Odd Field (SOOF)**note1**	1110_2 (E_H)	1100_2 ($C_$
End of Odd Field (EOOF)**note2**	1111_2 (F_H)	0001_2 ($1_$

Table 11 : Embedded Line Codes

note1: This code is only generated in the PAL or NTSC video modes

note2: This code is only generated in the PAL or NTSC video modes

We include Table 12 to show how the 8 bit control codes are mapped onto the output data bits in the 5 wire

Line Code	Most significant nibble Data[4:0]	Least significa Data[4:(
End of Line	1_0000_2 (10_H)	0_0000_2 (0
Blank Line (BL)	1_0011_2 (13_H)	1_0100_2 (1
Black line (BK)	1_0101_2 (15_H)	0_1100_2 (0
Visible Line (VL)	1_0110_2 (16_H)	1_1000_2 (1
Start of Even Field (SOEF)	1_1000_2 (18_H)	1_1100_2 (1
End of Even Field (EOEF)	1_1011_2 ($1B_H$)	0_1000_2 (0
Start of Odd Field (SOOF)	1_1101_2 ($1D_H$)	1_0000_2 (1
End of Odd Field (EOOF)	1_1110_2 ($1E_H$)	0_0100_2 (0

Table 12 : Mapping 8bit control codes to 5 wire output mode

Parity Checks				Comment
P_3	P_2	P_1	P_0	
✔	✔	✔	✔	Code word un-corrupted
✔	✔	✔	✘	P_0 corrupted, line code OK
✔	✔	✘	✔	P_1 corrupted, line code OK
✔	✘	✔	✔	P_2 corrupted, line code OK

Table 13 : Parity Checking

Parity Checks				Comment
P_3	P_2	P_1	P_0	
✘	✔	✔	✔	P_3 corrupted, line code OK
✘	✘	✔	✘	C_0 corrupted, invert sense of C_0
✘	✔	✘	✘	C_1 corrupted, invert sense of C_1
✔	✘	✘	✘	C_2 corrupted, invert sense of C_2
All other codes				2-bit error in code word.

Table 13 : Parity Checking

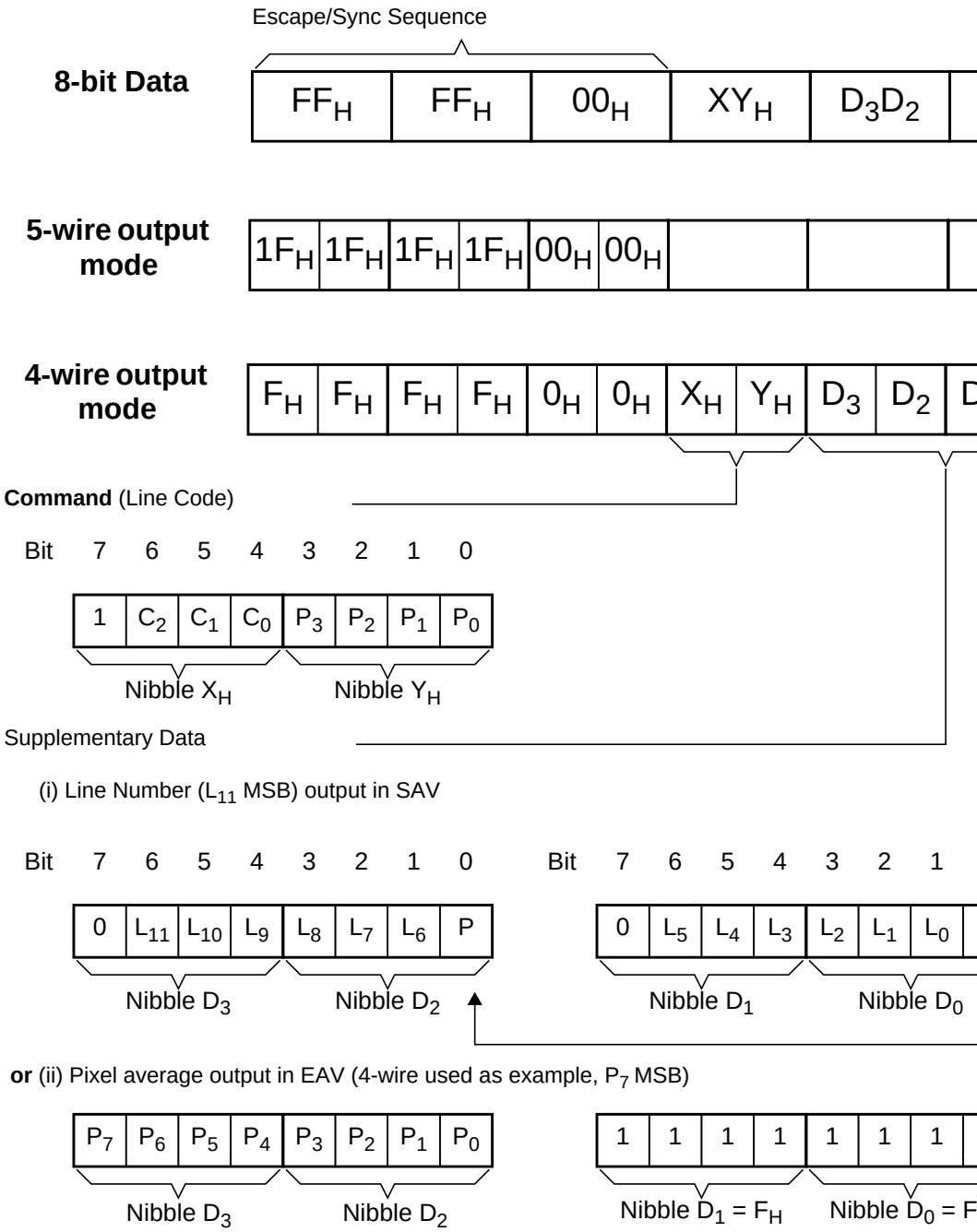


Figure 13 : Embedded Control Sequence

8.3 Video timing reference and status/configuration data

Each frame of video sequence comprises 2 fields. Each field of data is constructed of the following sequence

1. A start of field line
2. A number of black lines
3. A number of blank (or dark) lines
4. A number active video lines
5. An end of field line
6. A number of blank or black lines

Video Format	NTSC			PAL			CIF			Q	
VP3 mode	On		Off	On		Off	On		Off	On	
Extra Black Lines	On	Off	N/A	On	Off	N/A	On	Off	N/A	On	C
1st Field											
Start of Field Line	1	1	1	1	1	1	1	1	1	1	
Black Lines	8	2	8	8	2	16	8	2	16	8	
Blanking Lines	1	7	0	1	7	0	1	7	0	1	
Dark Lines	0	0	8	0	0	2	0	0	10	0	
Active Video lines	244	244	244	292	292	292	292	292	292	148	1
End of Field Line	1	1	1	1	1	1	1	1	1	1	
Blanking Lines	0	7	0	0	9	0	0	17	0	0	
Black Lines	7	0	0	9	0	0	17	0	0	1	
Total	262	262	262	312	312	312	320	320	320	160	1
2nd Field											
Start of Field Line	1	1	1	1	1	1	1	1	1	1	
Black Lines	8	2	8	8	2	16	8	2	16	8	
Blanking Lines	1	7	0	1	7	0	1	7	0	1	
Dark Lines	0	0	8	0	0	2	0	0	10	0	
Active Video lines	244	244	244	292	292	292	292	292	292	148	1
End of Field Line	1	1	1	1	1	1	1	1	1	1	
Blanking Lines	0	8	0	0	10	0	0	17	0	0	
Black Lines	8	0	1	10	0	1	17	0	0	1	
Total	263	263	263	313	313	313	320	320	320	160	1

Table 14 : Field and Frame Formats

Table 14 details the number of each type of data lines for NTSC, PAL, CIF and QCIF output formats. Each lin an embedded control sequence that identifies the line type (as outlined in Table 14). The control sequence is two bytes that contain a coded line number. The line number sequences starts with the start-of-frame line at one per line up until the end-of-frame line. Each line is terminated with an end-of-line embedded control sequ embedded sequences must be used to recognise visible video lines as a number of null bytes may be insert successive data lines.

There are a series of figures (Figure 14 - Figure 25) on the following pages that show line type construction

of the available video modes in VV5410/VV6410.

8.3.1 Blank lines

In addition to padding between data lines, actual blank data lines may appear in the positions indicated above with start-of-blank-line embedded control sequences and are constructed identically to active video lines exc contain only blank bytes, 07_H, (expressed as $01C_H$ in 10bit form).

8.3.2 Black line timing

The black lines (which are used for black offset calculation) are identical in structure to valid video lines exce with a start-of-black line code and contain either information from the sensor black lines or blanking data.

By default VP3 mode (see mode_select[24] for details) is selected. It is an option in any of the VP3 modes to black lines to be output (line 3-8). If the VP3 mode is not selected then all the black lines are enabled - no bl

Internally there is the concept of dark lines - to be used for dark offset cancellation (see following diagrams t position within the frame timing model), however externally the dark lines share the same line type code as t

8.3.3 Padding Lines and Fields

The user may choose to extend the inter-field period by increasing the field length by writing to serial registe event, the appropriate number of additional black or blank lines is inserted between the End Of Field (EOF) l Field (SOF) line. This means that the distance between SOF and EOF will remain constant.

The user can also extend the line length by writing to serial registers 82 and 83. The line length padding is ins sequence, ensuring that the distance between the SAV and EAV sequences will remain constant.

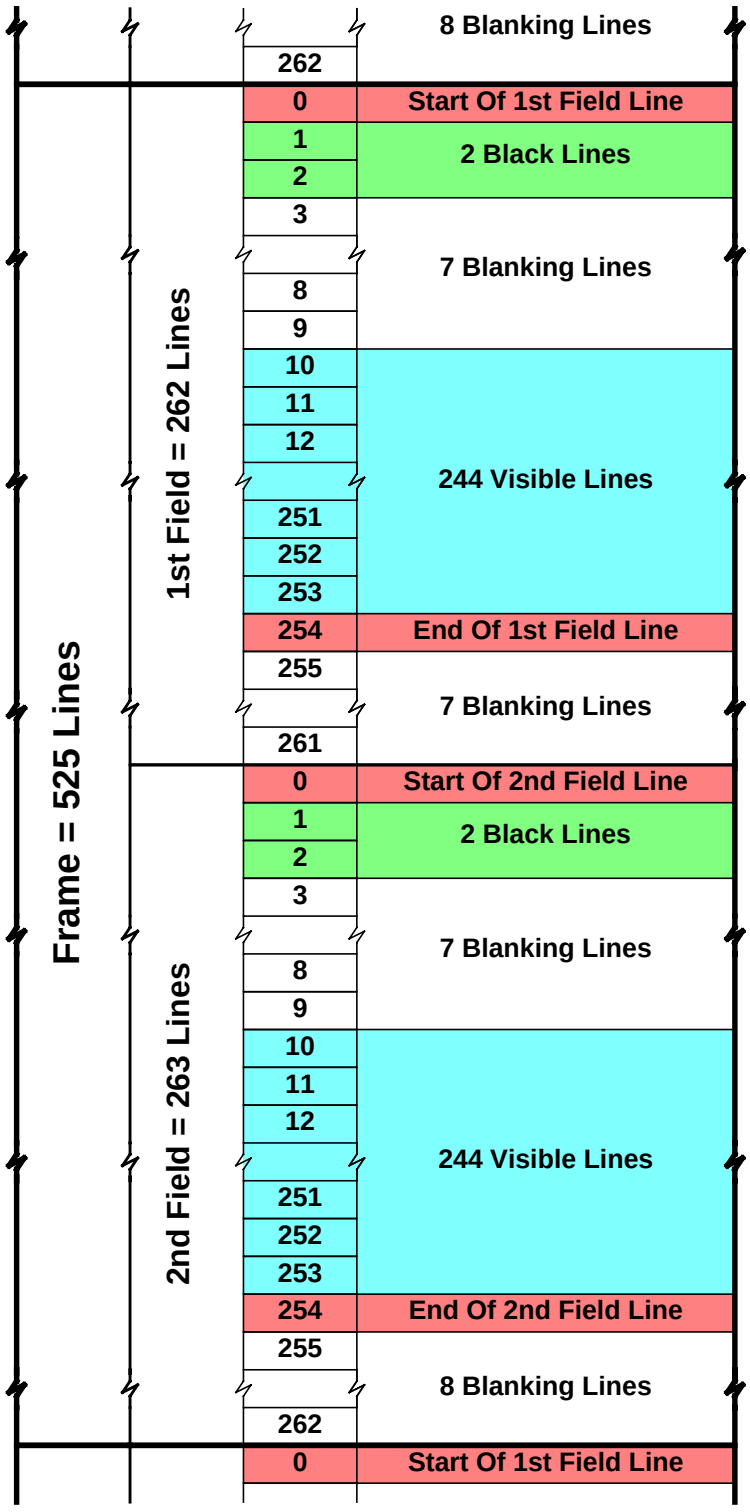


Figure 14 : NTSC Field and Frame Formats - VP3 Mode On, Extra Black Lines

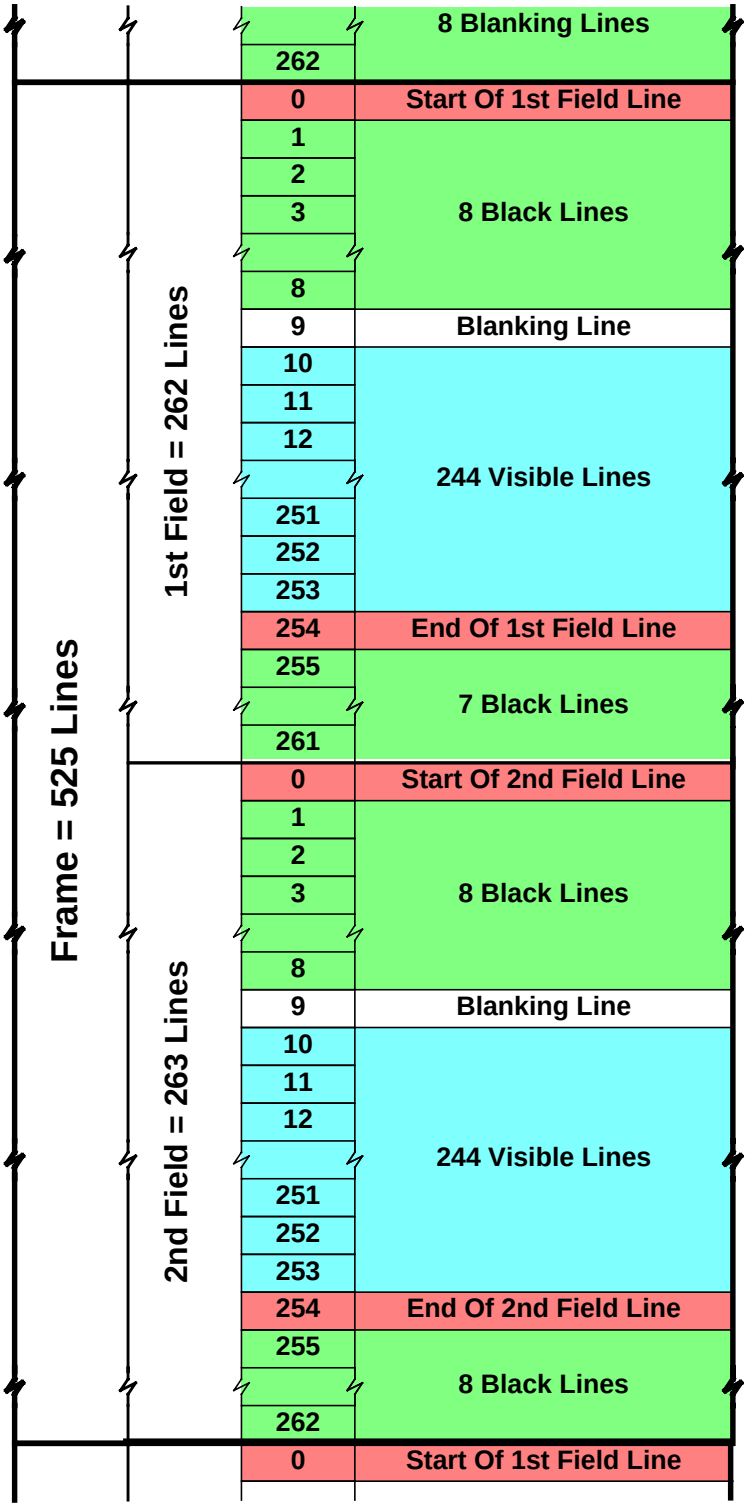


Figure 15 : NTSC Field and Frame Formats - VP3 Mode On, Extra Black Lines

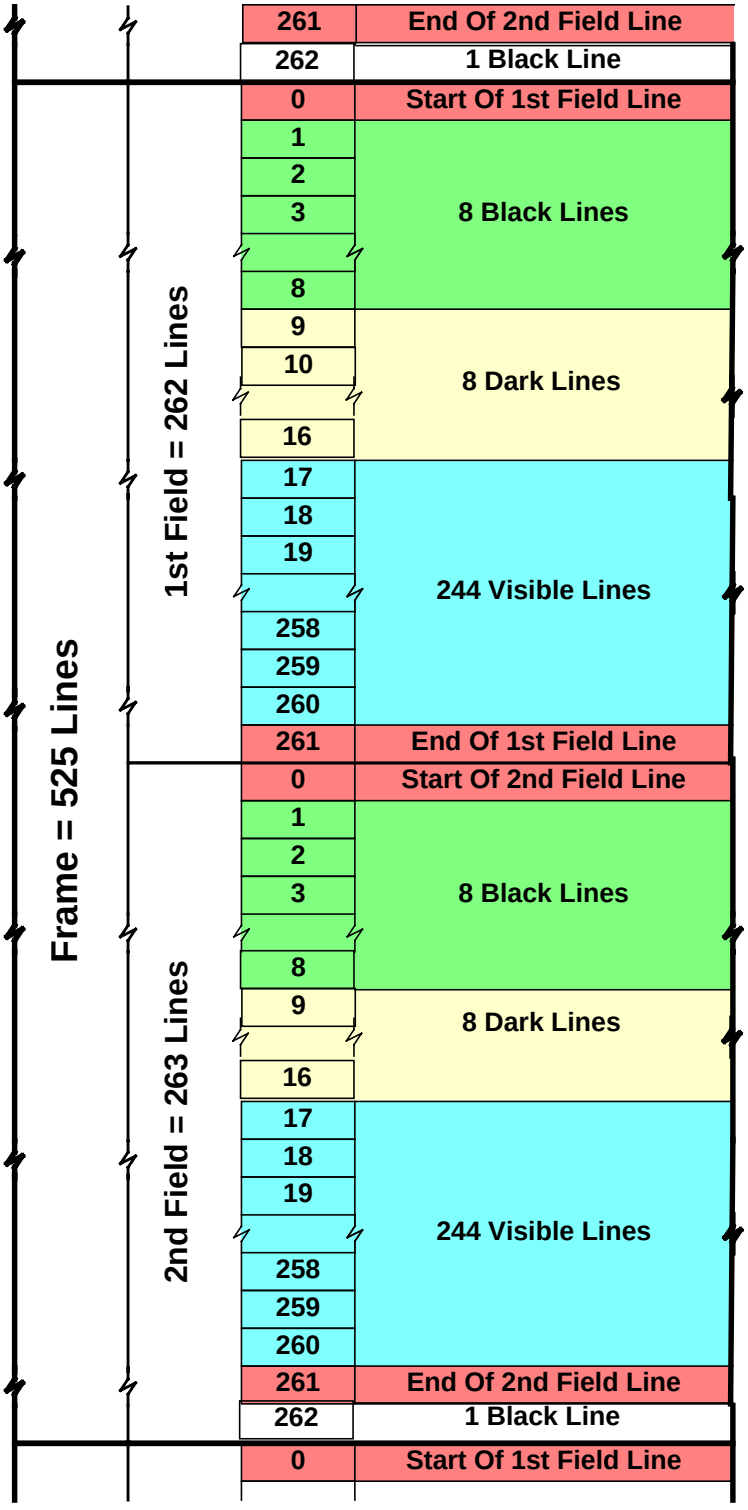


Figure 16 : NTSC Field and Frame Formats - VP3 Mode Off

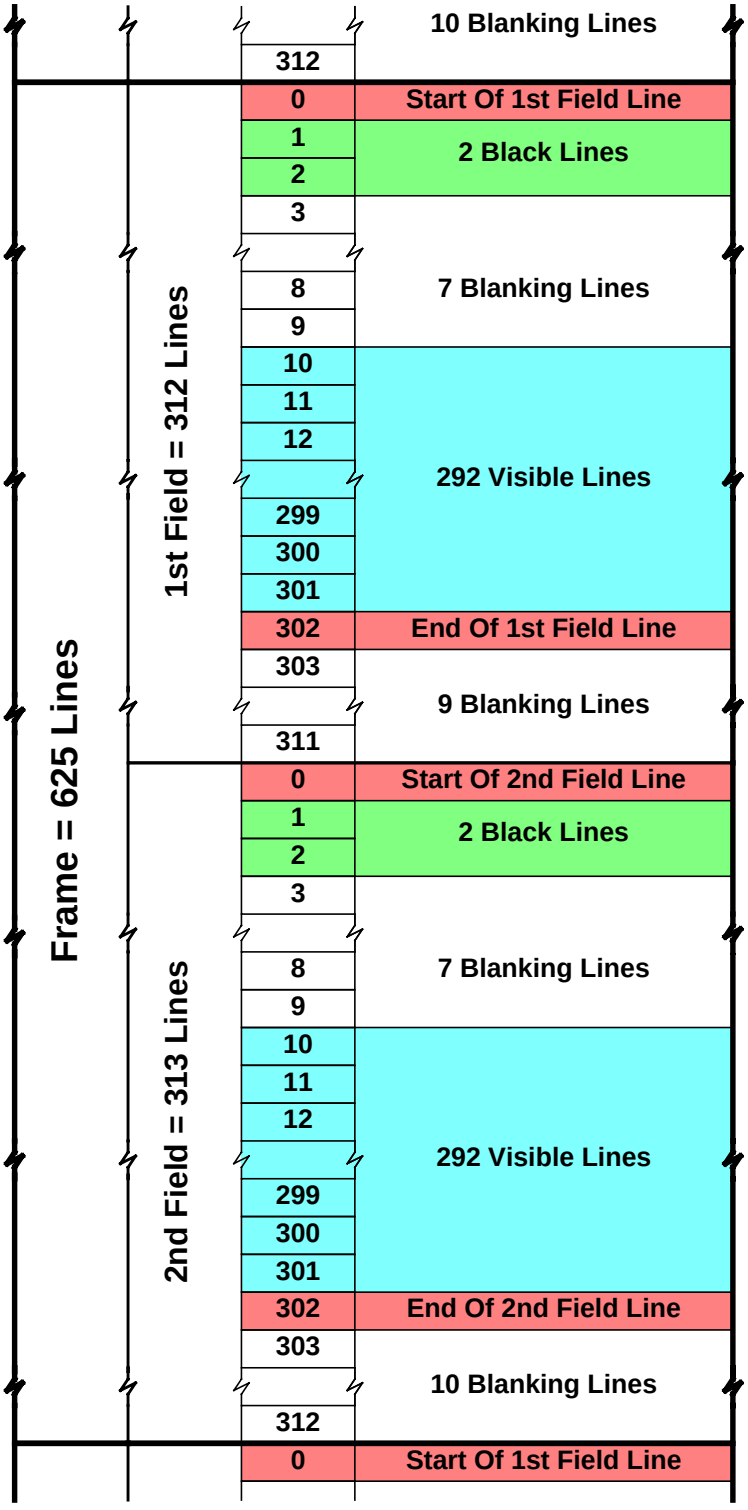


Figure 17 : PAL Field and Frame Formats - VP3 Mode On, Extra Black Lines O

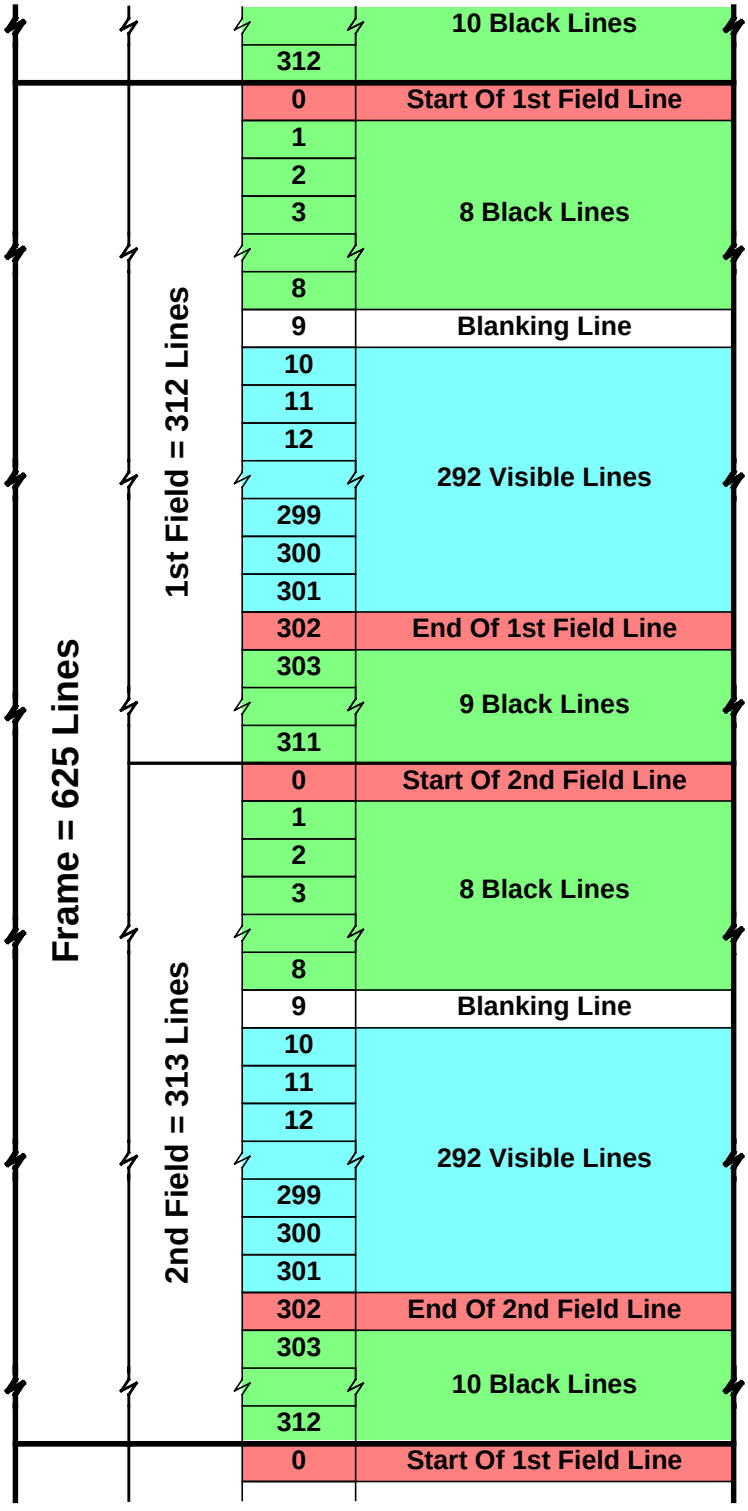


Figure 18 : PAL Field and Frame Formats - VP3 Mode On, Extra Black Lines

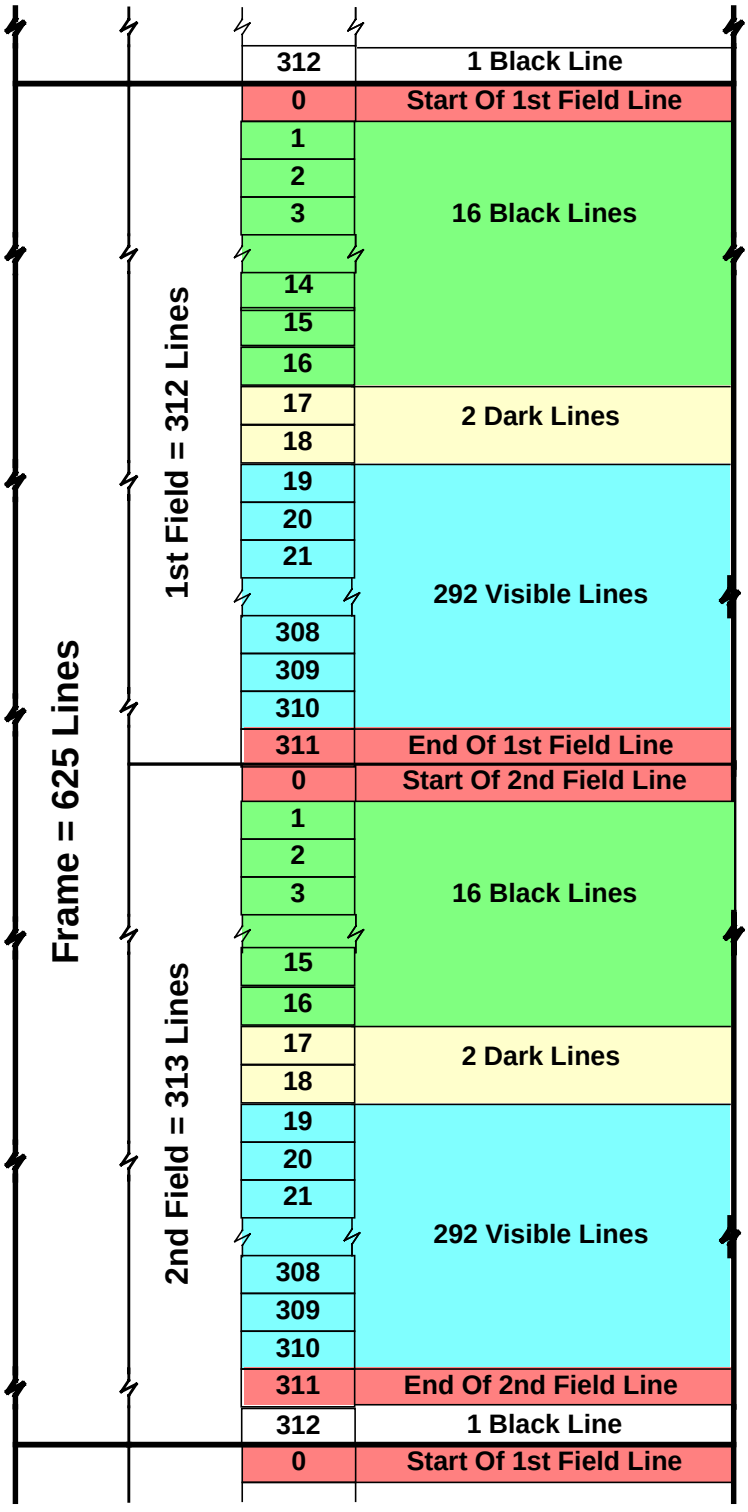


Figure 19 : PAL Field and Frame Formats - VP3 Mode Off

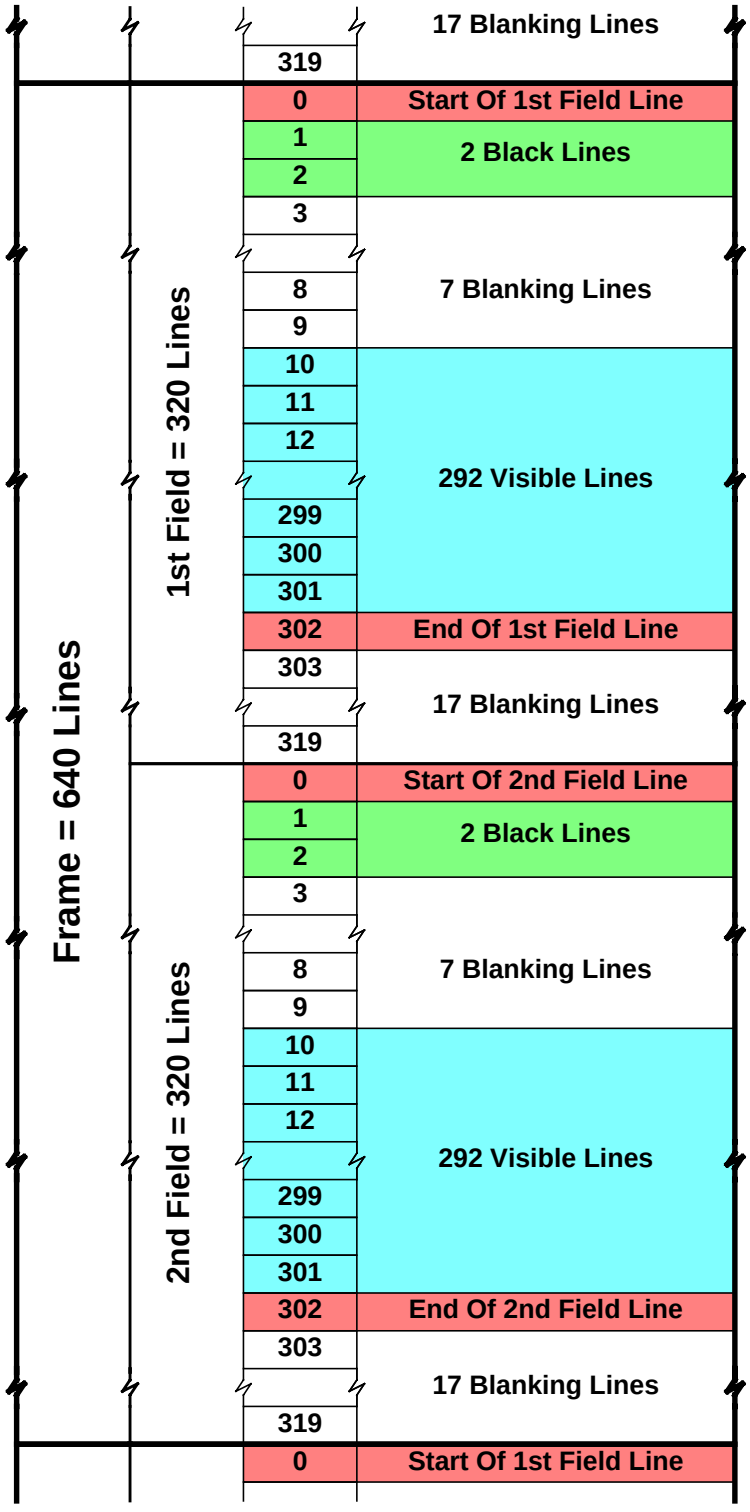


Figure 20 : CIF Field and Frame Formats - VP3 Mode On, Extra Black Lines C

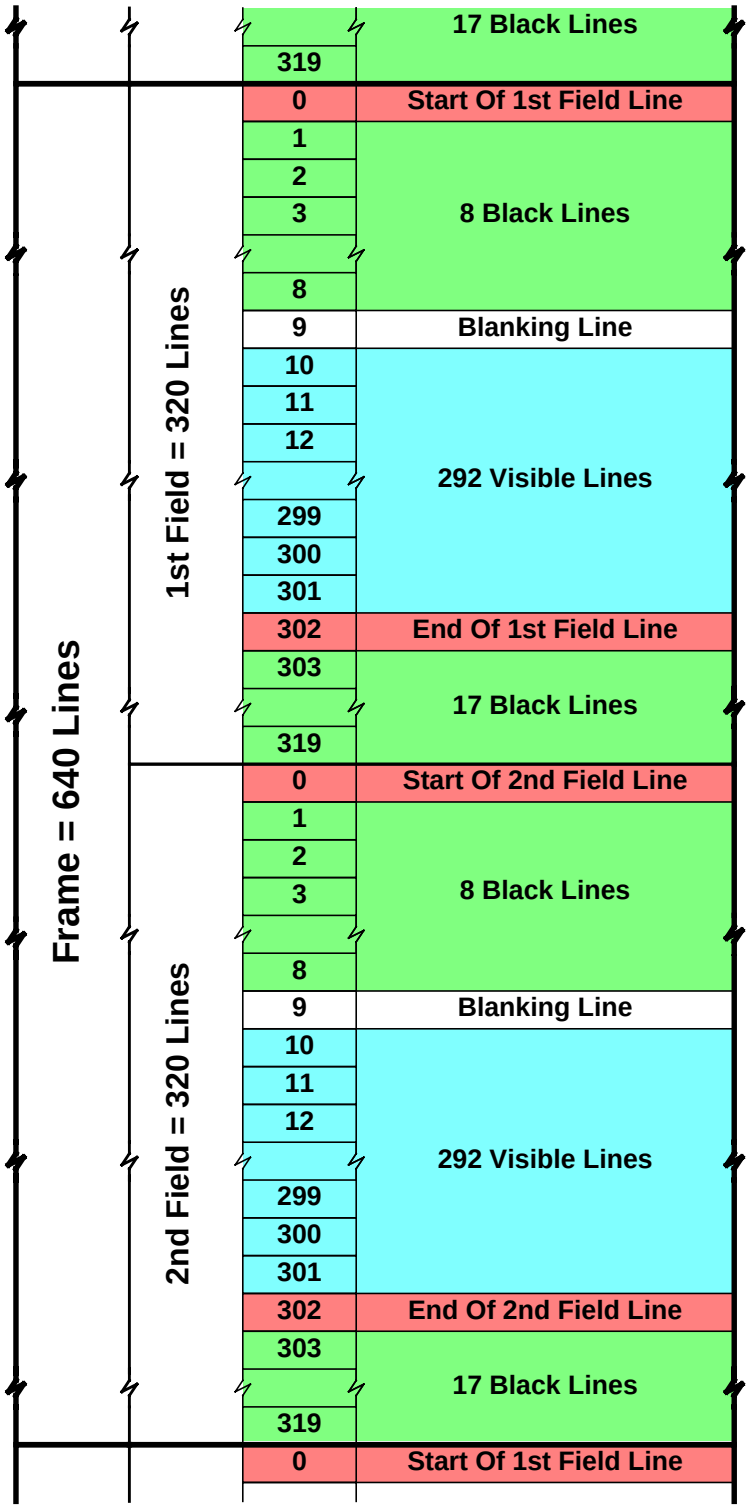


Figure 21 : CIF Field and Frame Formats - VP3 Mode On, Extra Black Lines O

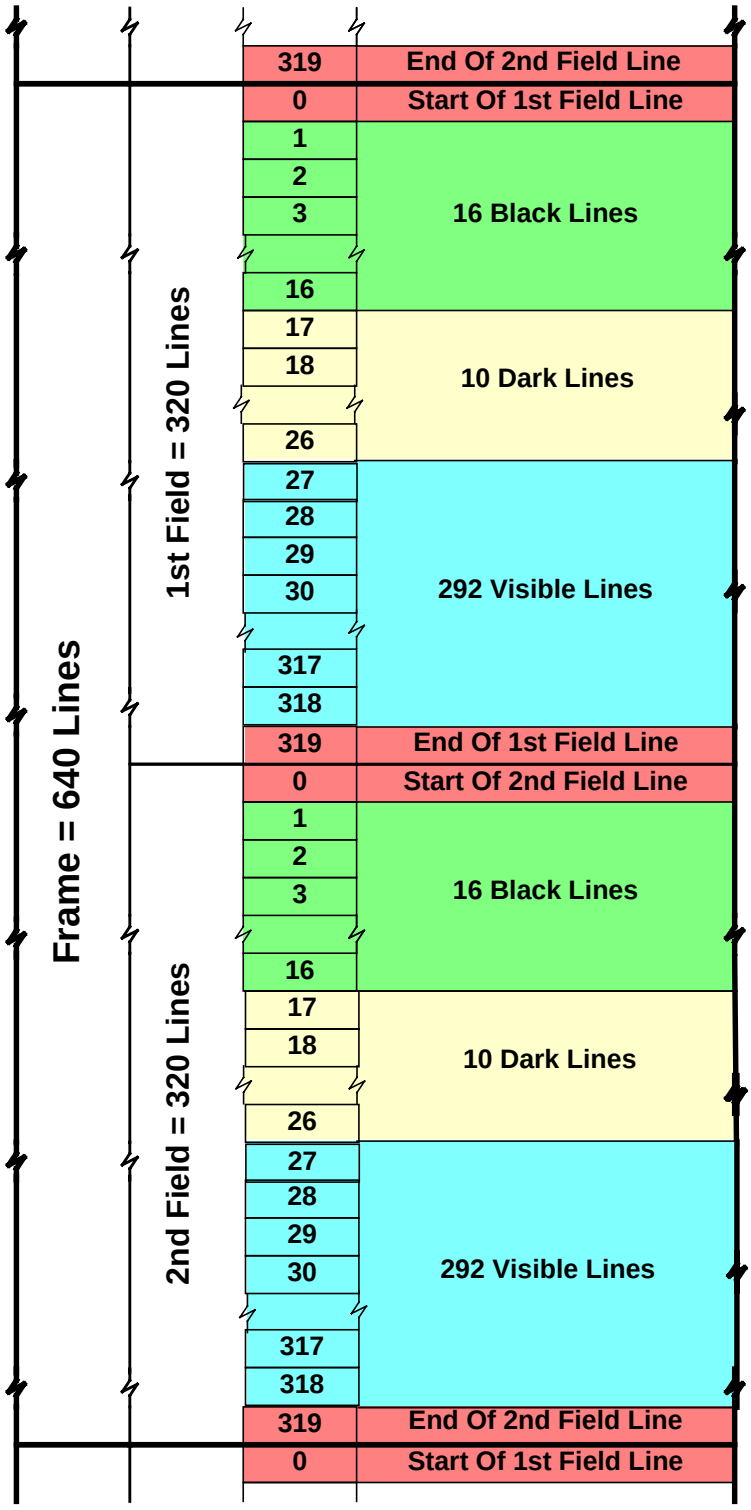


Figure 22 : CIF Field and Frame Formats - VP3 Mode Off

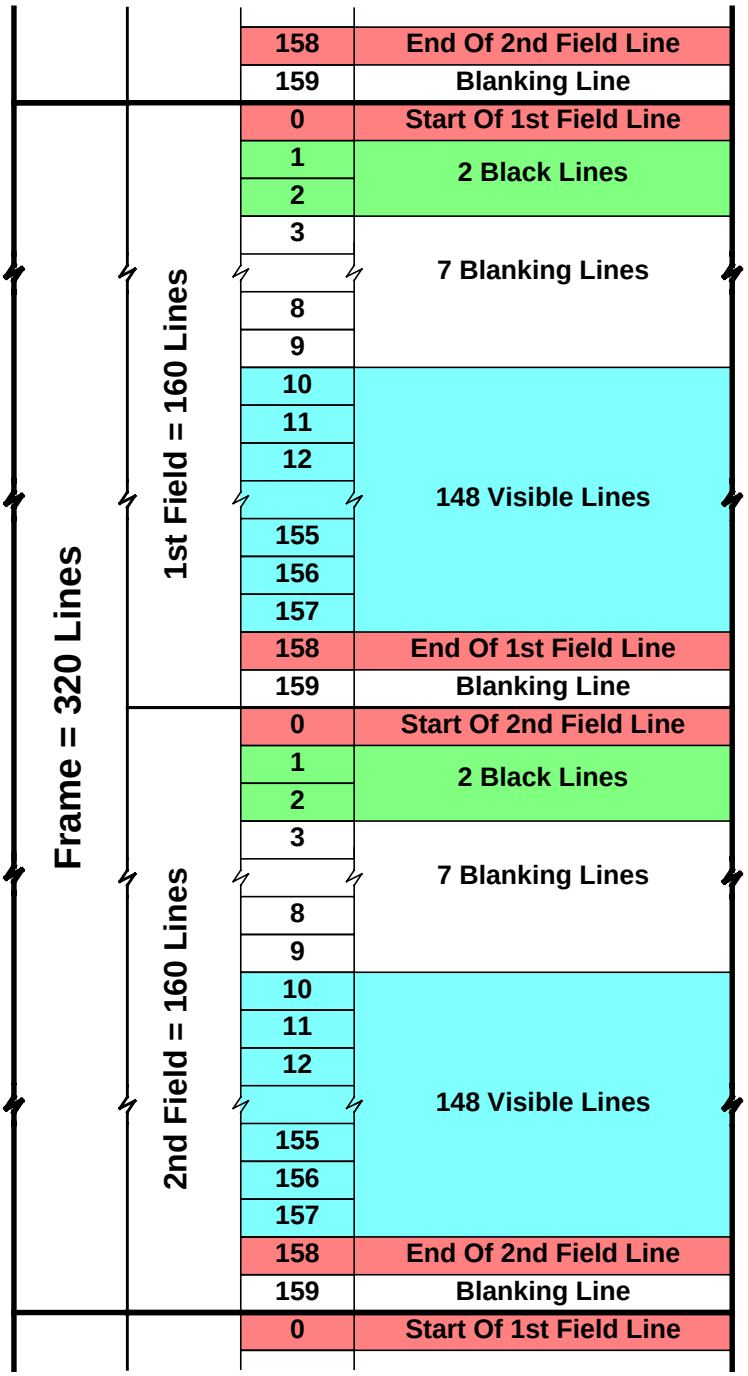


Figure 23 : QCIF Field and Frame Formats - VP3 Mode On, Extra Black Lines

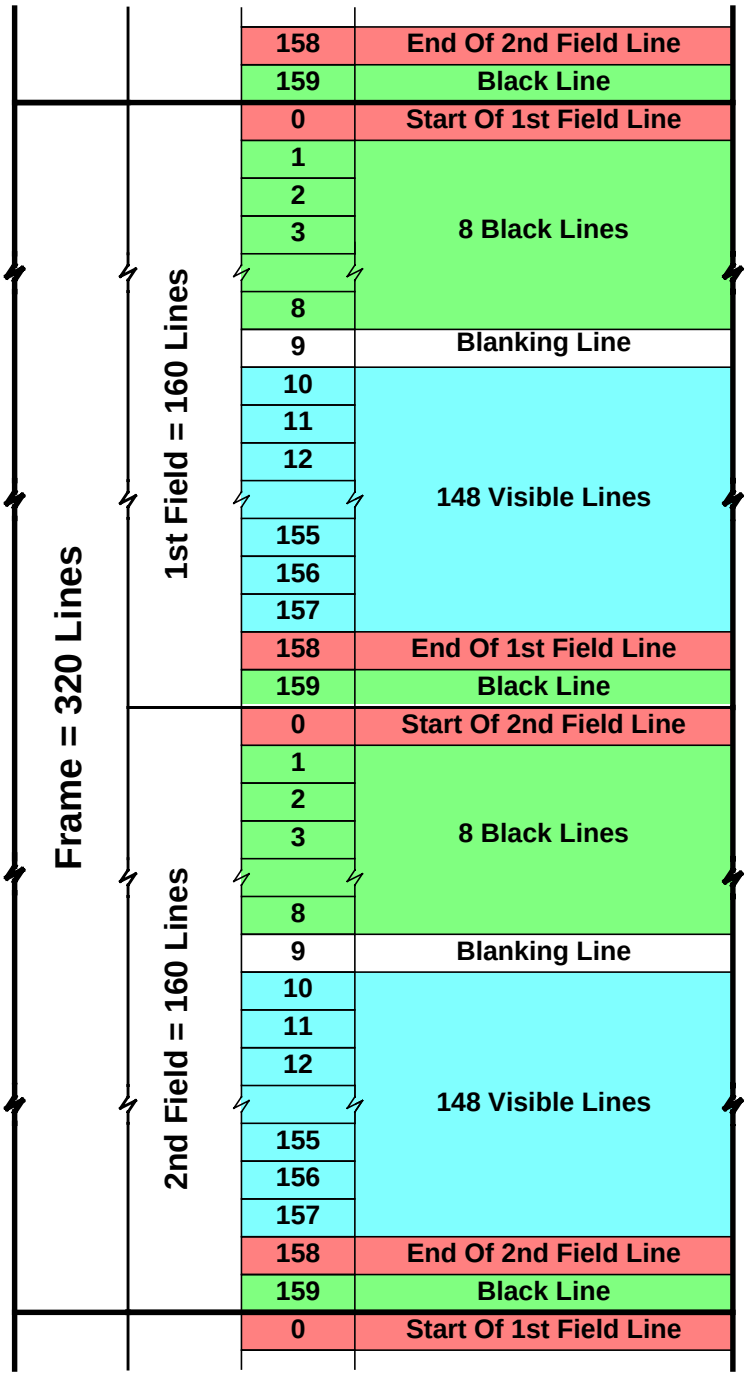


Figure 24 : QCIF Field and Frame Formats - VP3 Mode On, Extra Black Lines

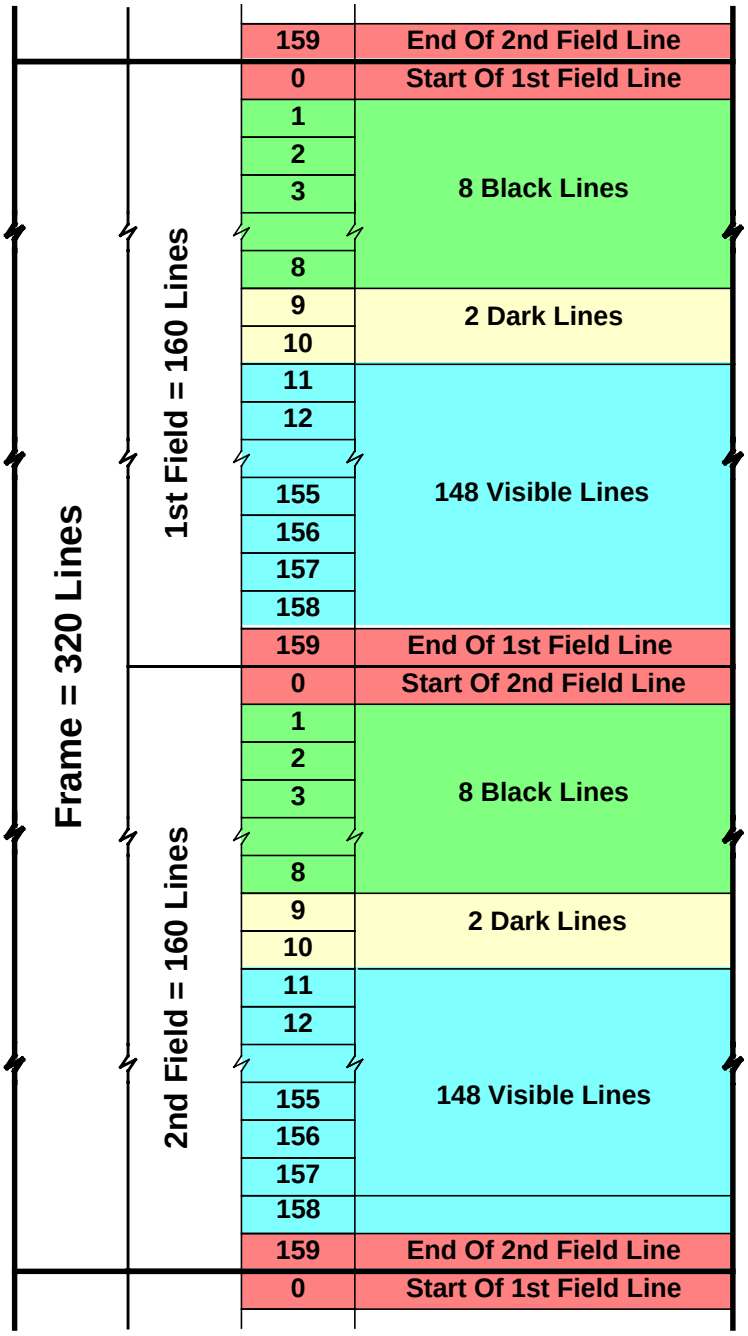
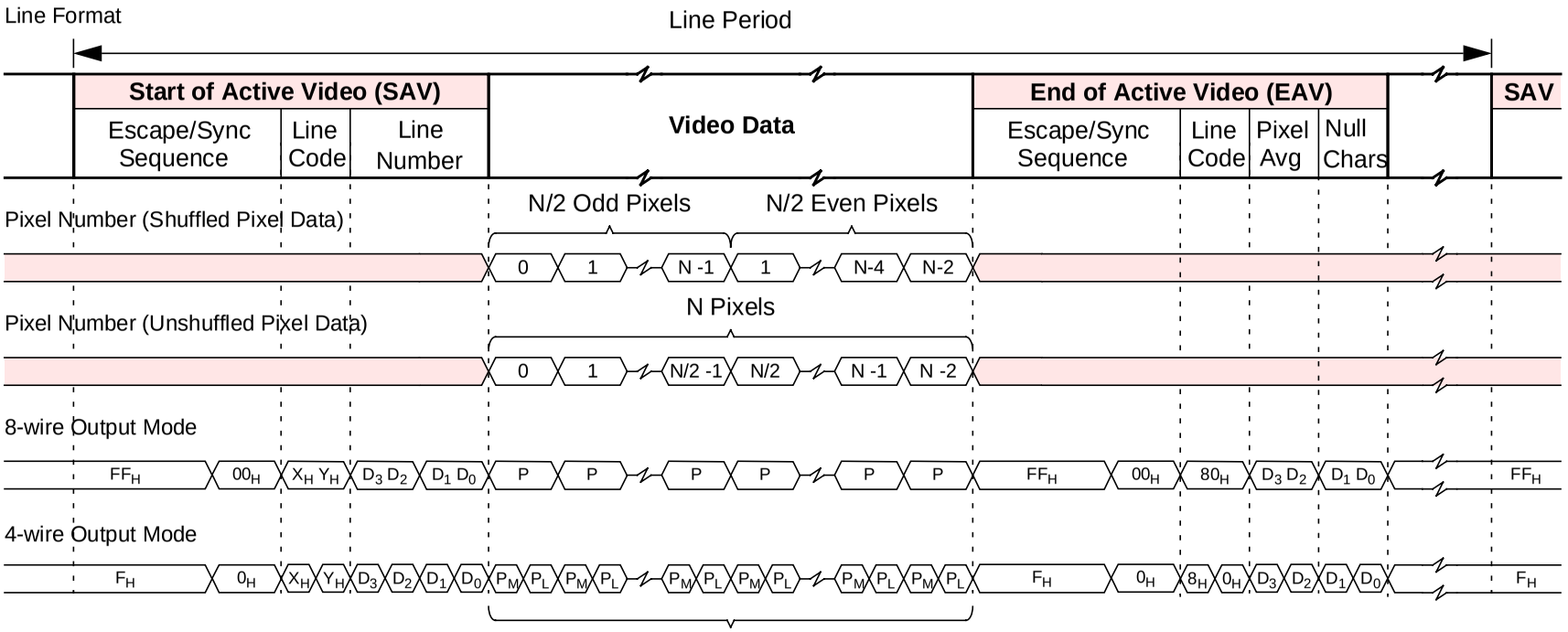
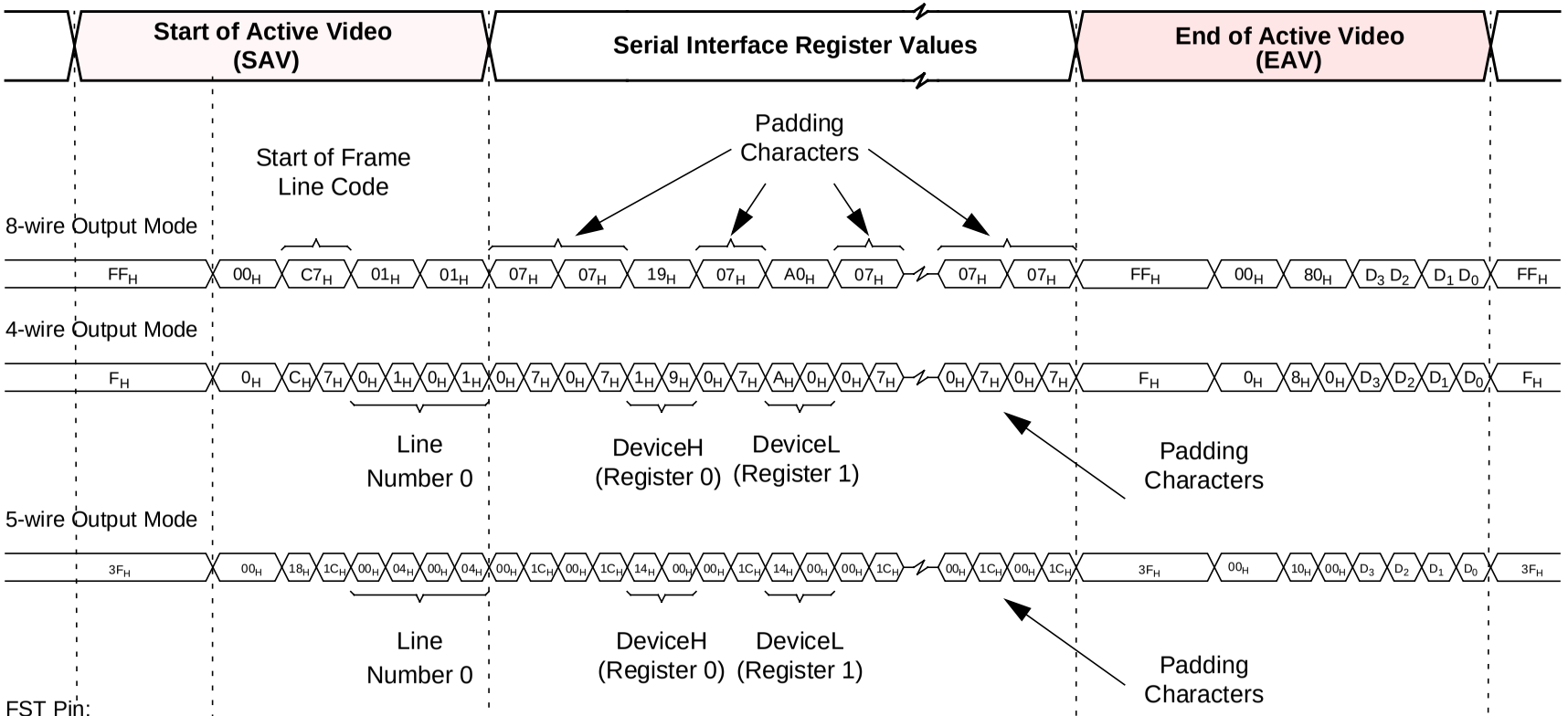


Figure 25 : QCIF Field and Frame Formats - VP3 Mode Off



(i)	Blanking Line (BL)	P = Blanking Level (07_H)
(ii)	Black Line (BK)	P = Valid Black Pixel Data
(iii)	Visible Line (VL)	P = Valid Pixel Data
(iv)	Start of Frame (SOF)	P = Sensor Status Data, data at pixel position 0 and 1 set to blanking level, 07_H.
(v)	End of Frame (EOF)	P = Blanking Level (07_H)



FST Pin:

(i) Frame start pulse - qualifies status line information - selected by writing 2'b01 to fg_mode register[7:6], see Table 32 for details

(ii) Flash synchronisation mode for FST - high in line following EOF, falls at start of EAV in Status line - selected by writing 2'b1x to serial register, 14(hex)

8.3.4 Valid video line timing

All valid video data is contained on active video lines. The pixel data appears as a continuous stream of byte
lines. The pixel data may be separated from the line header and end-of-line control sequence by a number o

8.3.5 Start of frame line timing

The start of frame line which begins each video field contains no video data but instead contains the content
interface register map. Immediately following the SAV sequence there are 2 padding pixels, (see Figure 27),
levels, (07_H). There will be more blanking codes output after all the serial interface registers have been outpu
pixels continue to be output until terminated by an end-of-line control sequence. To ensure that no escape/sy
reserved FF,FF,00 sequence), appear in the sensor status/configuration information the code 07_H is output a
interface value.

If a serial interface register location is unused then a default value, the DeviceH register, is output. The read-
registers is independent of whether the pixel read-out order is shuffled or un-shuffled.

8.3.6 End of frame line timing

The end of frame line contains no video data. Its sole purpose is to indicate the end of a frame.

8.4 Detection of sensor using data bus state

On power-up a sensor will pull all data lines high and these lines will remain high while the device is in the po
power state. The device is removed from this low power mode by the I2C host writing to sensor register, setu
When the device exits the low power mode it will follow a defined power up sequence, please see Figure 30
Upon completion of the power up sequence the sensor will begin streaming video.

8.5 Resetting the Sensor Via the Serial Interface

Bit 2 of setup0 register allows the VV5500/VV6500 sensor to be reset to its power-on state via the serial inte
“Soft Reset” bit causes all of the serial interface registers including the “Soft Reset” bit to be reset to their de
“Soft Reset” leaves the sensor in low-power mode.

8.6 Resetting the Sensor Via the RESETB pin

On power-up the RESETB pin is configured as an active low system reset which has the same effect as a so
the serial interface as described above.

8.7 Resynchronising the Sensor Via the RESETB pin configured as SINB

Bit 5 of the pin mapping register [21] allows the RESETB pin to be re-configured as an active low (edge trigg
synchronisation signal which will reset the video timing to the beginning of a field but will NOT reset the seria
the host does not have to reconfigure the sensor following a resynchronisation.

SR0-SR1	"Soft-Reset" Command. At the end of the command the sensor is reset and enters low-power mode.
SR2	The sensor enters low-power mode.
SR3-SR4	"Exit Low Power Mode" Command. Powers-up analogue circuits and initates the sensor's 4-frame start-up sequence
SR5-SR6	1 Frame of alternating 9_H & 6_H data on D[3:0] for the host to determine the best sampling phase for the nibble data (D[3:0]).
SR7-SR8	4 Frames after the "Exit Low-Power mode" command, the sensor starts outputing valid video data.

8.8 Power-up, Low-power and Sleep modes

Please note that the following descriptions of low power and sleep modes assumes that the user has selecte output mode, that is D[3:0] will transmit the digital video data. If the 5-wire or 8-wire modes are selected the sa is followed however the contents of the data bus will differ slightly.

PU0	System Power Up
PU1	Sensor enters low power mode and databus bits driven high.
PU2	Host enables the sensor clock, CLKI.
PU3-PU4	The host sends a “Soft-Reset” command to the sensor via the serial interface. This the sensor is in low-power mode.
PU5	Host issues command to remove sensor from low-power mode.
PU6-PU7	Sensors begins execution 4 frame start sequence.
PU8-PU9	One frame of alternating 9_H & 6_H data on D[3:0] for the host to determine the best s phase for video data.
PU10-PU11	4 Frames after the “Exit Low-Power Mode” serial comms, the sensor starts outputir data.

Table 15 : Typical System Power-Up

8.8.1 Power-Up/Down (Figure 29)

The sensor enters low-power mode on power-up. On power-up all of the data bus lines are driven high imme device is in low-power mode (Section 8.8.2).

The sensor will remain in the low power mode until the external host sends the appropriate message over I2 power bit - bit0 of serial reguister, setup0, index 10_{16}.

After the “Exit Low-Power Mode” command has been sent the sensor will output for one frame, a continuous s 9_H and 6_H values on D[3:0] The patterns generated in 5 and 8 wire modes are given in Table 16 below. By lo resulting 0101/1010 patterns appearing on the data bus lines the host can determine the best sampling posit data. After the last 9_H 6_H pair has been output the data bus returns to F_H,($1F_H$ in 5 wire mode), until the start point the first active video frame will be output. After the host has determined the correct sampling position fo then wait for the next start of frame line (SOF).

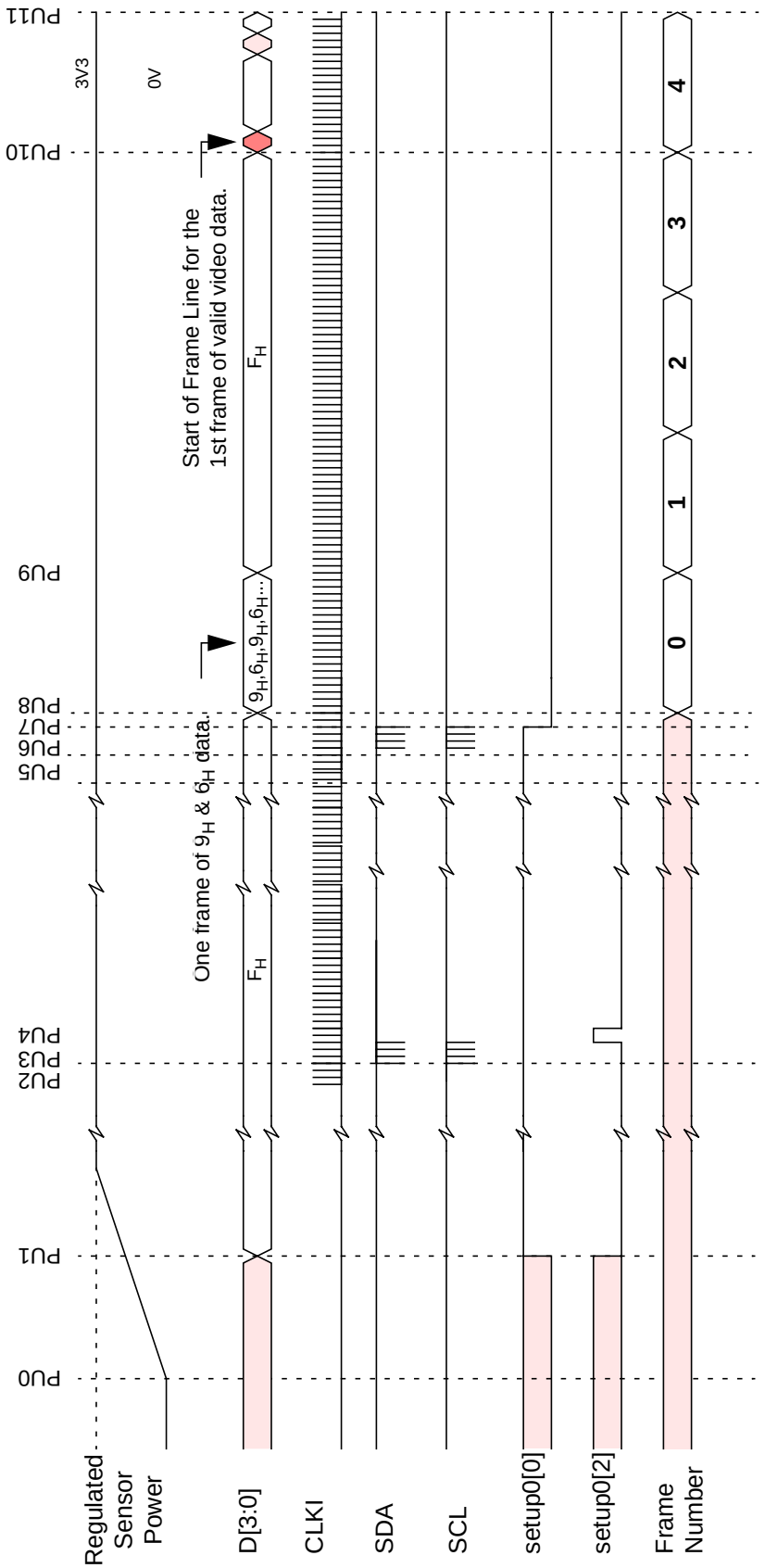


Figure 29 : Typical System Power-Up Procedure

Mode	10-bit Value	Output Data Bus Pattern
4-Wire	258_H	$9_H/6_H$ ($1001_2/0110_2$)
5-Wire	136_H	$09_H/16_H$ ($01001_2/10110_2$)
8-Wire	096_H / 069H	$25_H/1A_H$ ($00100101_2/00011010$

Table 16 : Output Data Bus Patterns for determination of Best Sampling Posit

8.8.2 Low-Power Mode (Figure 30)

Under the control of the serial interface the sensor analog circuitry can be powered down and then repowere power bit is set via the serial interface, all the data bus lines will go high at the end of the end of frame line o At this point the analog circuits in the sensor will power down. The system clock must remain active for the du mode.

During low power mode only the analog circuits are powered down, the values of the serial interface register gain are preserved. The internal frame timing is reset to the start of a video frame on exiting low-power mode. to the previous section, the first frame after the serial comms contains a continuous stream of alternating 9_H equivalent for the alternative ouput databus widths - to allow the host to re-confirm its sampling position. The the first start of frame line is generated.

8.8.3 Sleep Mode

Sleep mode is similar to the low-power mode, except that analog circuitry remains powered. When the sleep received via the serial interface the pixel array will be put into reset and the data lines all will go high at the e frame. Again the system clock must remain active for the duration of sleep mode.

When sleep mode is disabled, the CMOS sensor's frame timing is reset to the start of a frame. During the firs from sleep mode the data bus will remain high, while the exposure value propagates through the pixel array. second frame the first start of field line will be generated.

8.8.4 System clock status during sensor low-power modes

To allow the sensor to enter and exit the low power and sleep modes the system clock, CLKI, must be active

8.9 Suspend mode

Under the control of the SUSPEND pin VV5410/VV6410 can be forced into an ultra low power mode. The se less than 80uA of current while suspended. While the sensor is in this mode video output is turned off and no communications can occur.

The SUSPEND mode is effectively identical to a power on reset - all the video timing blocks within the sensor contents of the serial interface, therefore the user will have to perform a compete reconfiguration of the devic SUSPEND. The sensor will also repeat the full 4 field power up sequence.

Mode	Description	Approx. Sensor Cu
Suspend	Sensor in lowest power state. Suspend has been asserted by host.	c.80uA

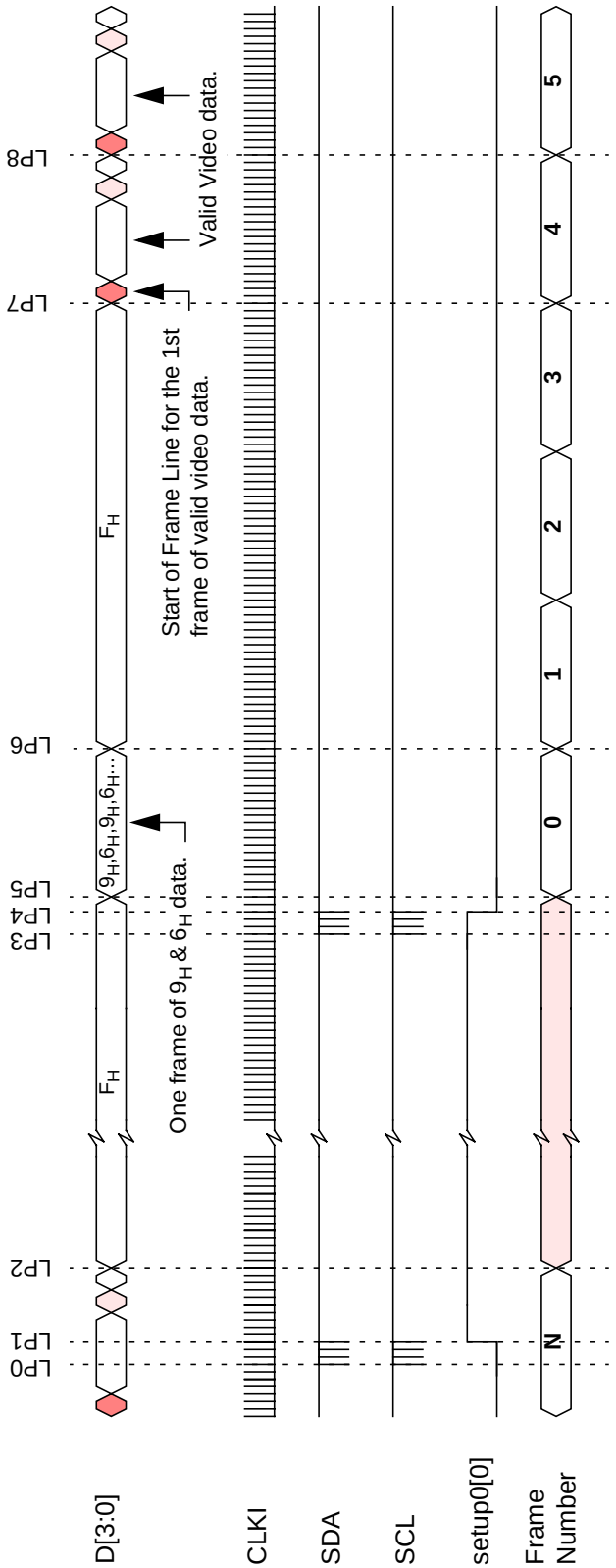
Table 17 : VV5410/VV6410 suspend mode power consumption

8.10 Data Qualification Clock, QCK

VV5410/VV6410 provides a data qualification clock, (see Figure 31), to qualify the information output on data can generate two styles of qualification clock:

- Fast QCK, clocks at nibble rate. The falling edge of this clock qualifies data

.



LP0-LP1	"Enter Low Power Mode" Command.
LP2	At end of current frame, the sensor will enter the low power mode and the databus will be driven high.
LP3-LP4	"Exit Low Power Mode" Command sent to sensor - sensor begins power up sequence.
LP5-LP6	1 Frame of alternating 9_H & 6_H data on D[3:0] for the host to determine the best sampling phase for the nibble data (D[3:0]).
LP7-LP8	4 Frames after the "Exit low Power Mode" command, the sensor starts outputing valid video data.

- The slow QCK, clocks at pixel rate. Both the falling and rising edge of this clock are used to qualify data. data nibble is qualified by the rising edge of the slow QCK and the least significant nibble is qualified by the slow QCK.

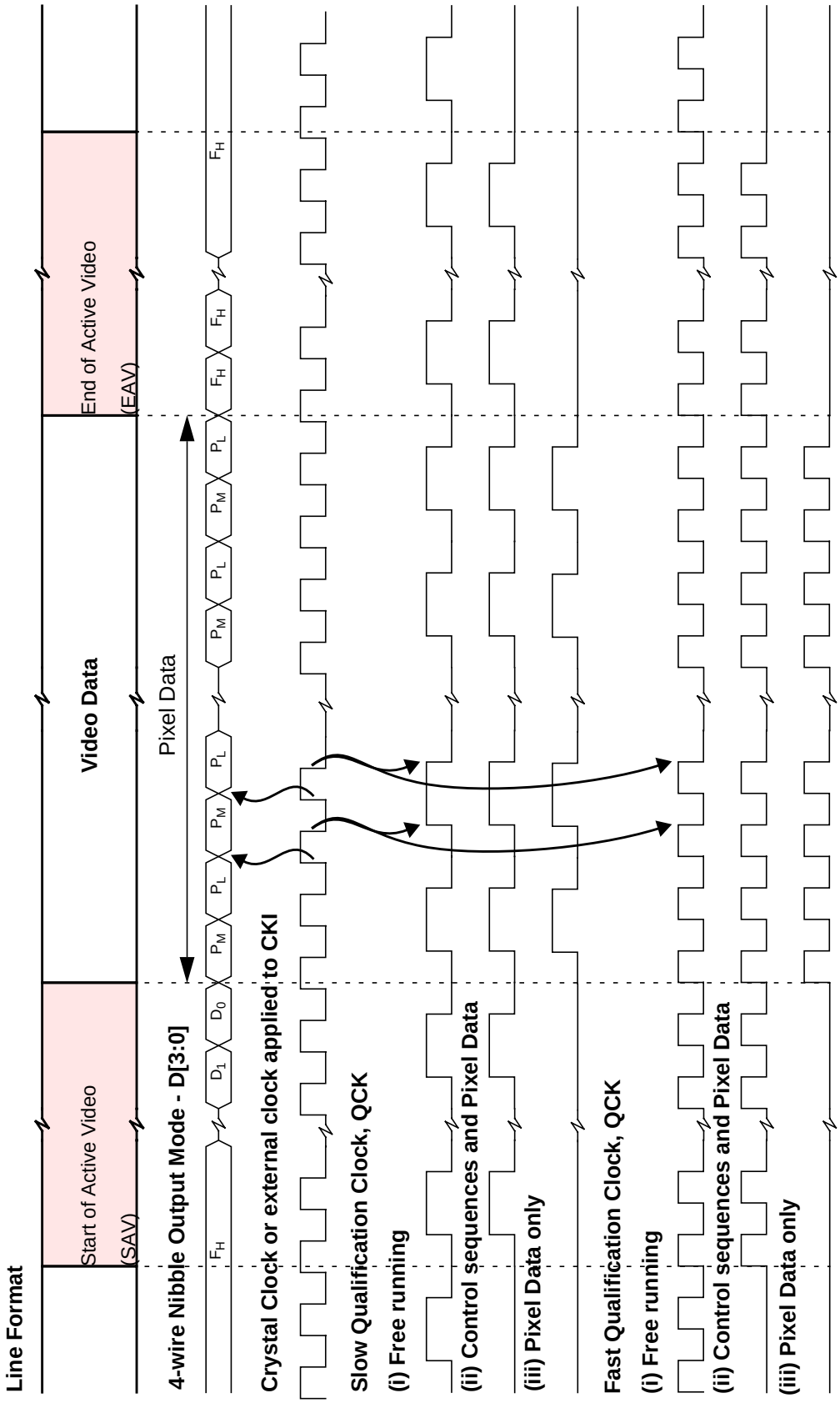
There are 4 modes of operation of QCK.

1. Disabled (Always low - default mode of operation)
2. Free running - qualifies the entire output data stream.
3. Qualify embedded control sequences, status data, (from the SOF line), and pixel data.
4. Qualify pixel data only, (this will include data from the black lines).

The operating mode for QCK is set via the serial interface. The QCK output can be tri-stated either when OE via the appropriate control bit in the serial interface, (see data_format register[22]).

The QCK pin can also be configured to output the state of a serial interface register bit. This feature allows th external devices, e.g. stepper motors, shutter mechanisms.

Full details of how to configure the QCK output pin can be found in 2 registers, fg_mode[20] and pin_mappin


Line Format
Start of Active Video (SAV)
Video Data
End of Active Video (EAV)
Pixel Data
4-wire Nibble Output Mode - D[3:0]
Crystal Clock or external clock applied to CKI
Slow Qualification Clock, QCK
(i) Free running
(ii) Control sequences and Pixel Data
(iii) Pixel Data only
Fast Qualification Clock, QCK
(i) Free running
(ii) Control sequences and Pixel Data
(iii) Pixel Data only
FH
D1
D0
PM
PL

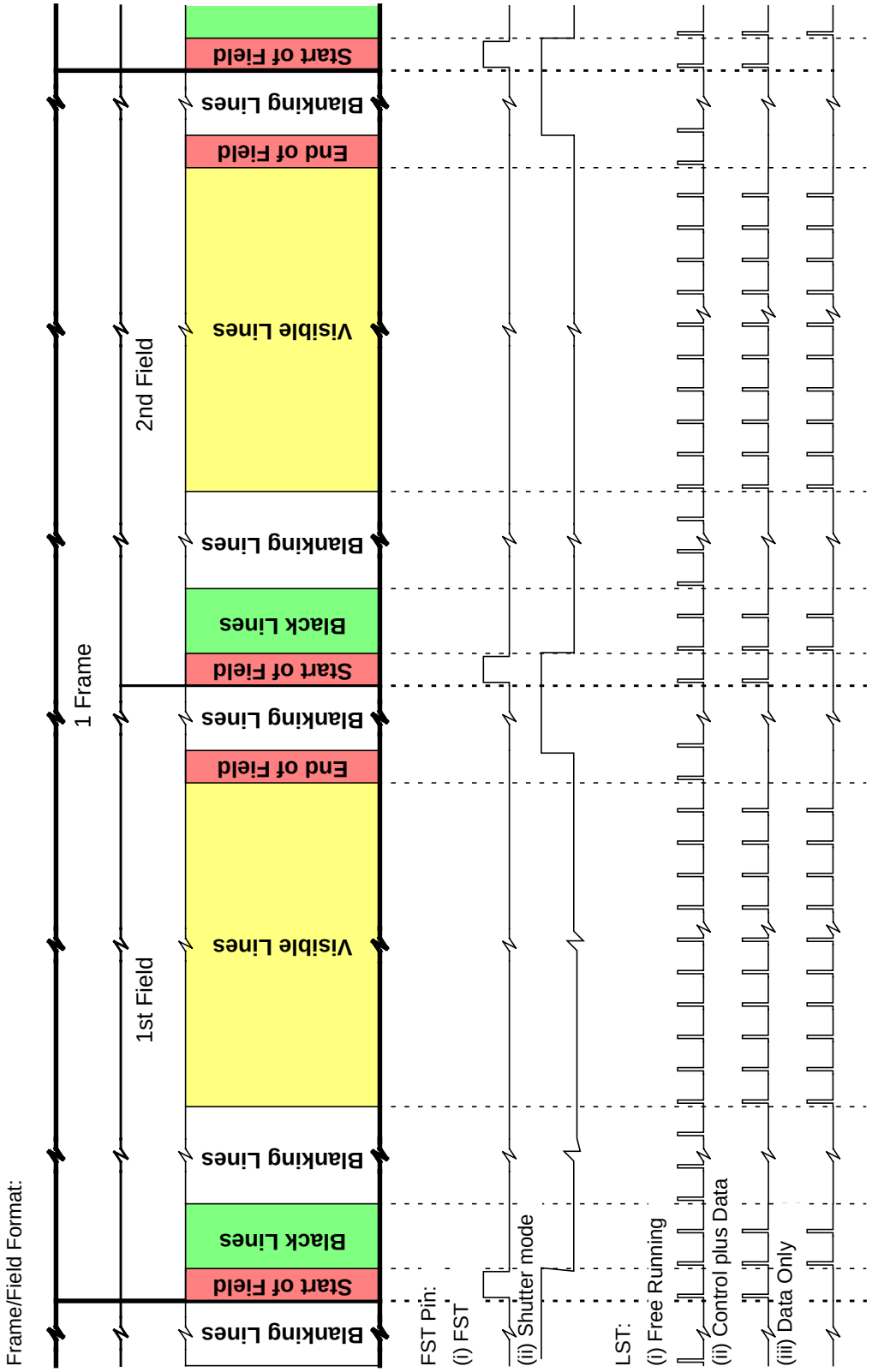


Figure 22 : Frame/Field Level Timings for FST and LST

8.10.5 Line Start Signal, LST

There are 4 modes of operation for the LST pin programmable via the serial interface, (see fg_mode[20]):

1. Disabled (Always Low- Default).
2. Free running - LST signal occurs once at the beginning of every line.
3. All lines except blanking lines are qualified by LST.
4. Only Black and Visible Lines are qualified by LST.

The LST is tri-stated either when OEB is driven high or via the appropriate control bit in the serial interface, (register[22]). Table 18below details the LST timing for the different video modes, (see Figure 33 for specifica

Video Mode	t1		t2
	pck's	us	pck's
CIF	21	5.25	16
QCIF (both pan tilt and sub sampled, 16Mhz clock)	6	6.00	15
QCIF (both pan tilt and sub sampled, 8Mhz clock)	6	6.00	15
PAL	33	4.652	42
NTSC	27	4.714	12

Table 18 : LST Timing

8.10.6 Frame Start Signal, FST

There are 3 modes of operation for the FST pin programmable via the serial interface:

1. Disabled (Always Low- Default).
2. Frame start signal. The FST signal occurs once frame, is high for 356 pixel periods (712 system clock p the data in the start of frame line.
3. Shutter/Electronic Flash Synchronisation Signal - FST rises a the start of the video data in the first blac EOF line and falls at the end of data in the SOF line.

The FST output is tri-stated either when OEB is driven high or via the appropriate control bit in the serial inte data_format register[22]).

The configuration details for FST can be found in fg_mode register[20].

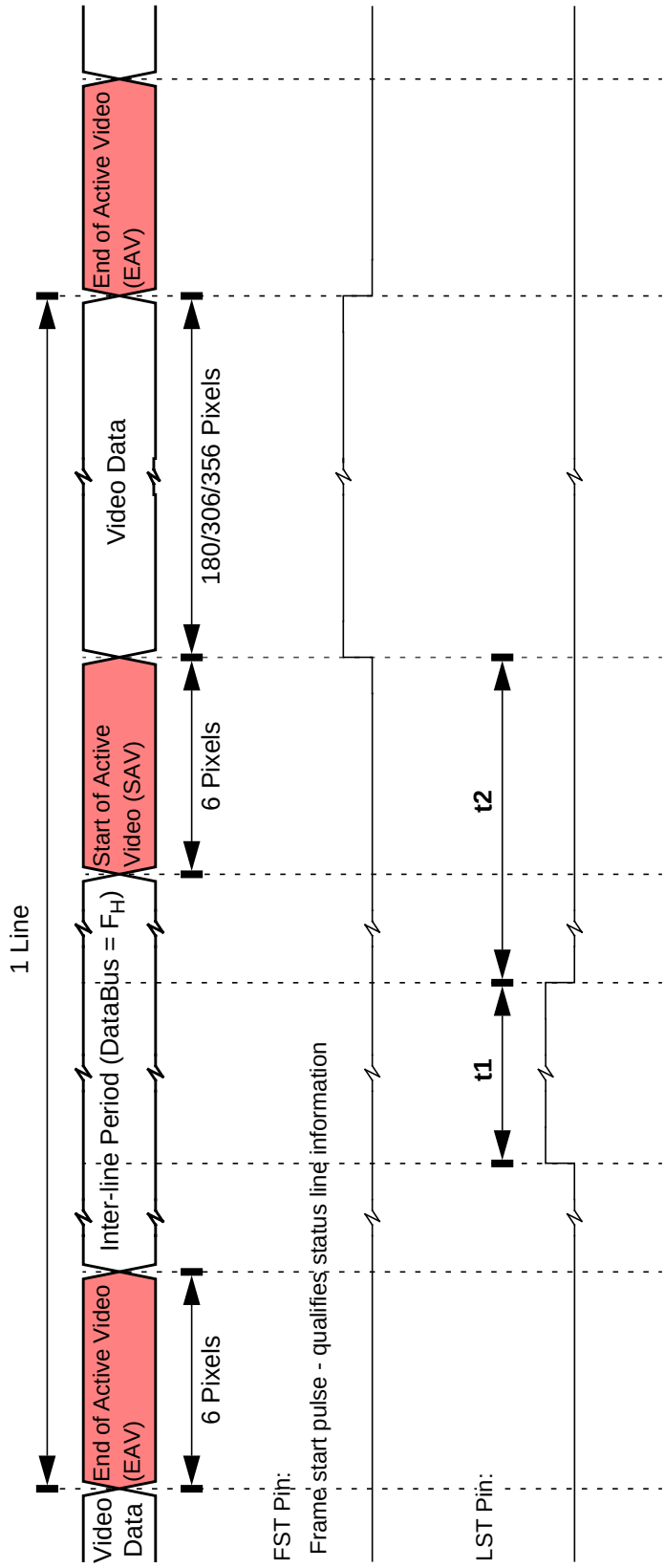


Figure 33 : Line Level Timings for FST and LST.

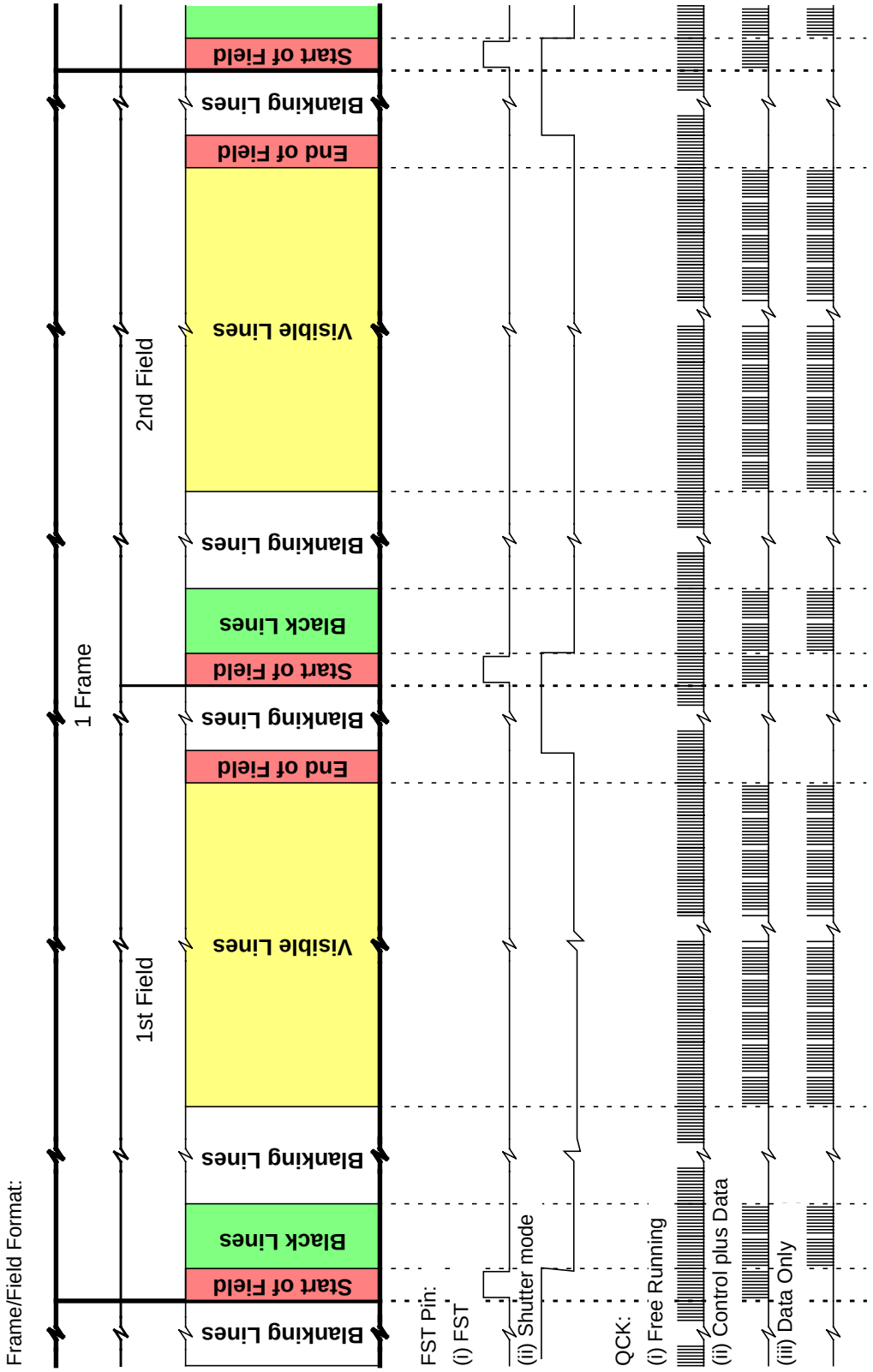


Figure 34 : Frame/Field Level Timings for FST and QCK

9. Serial Control Bus

9.1 General Description

Writing configuration information to the video sensor and reading both sensor status and configuration inform sensor is performed via the 2-wire serial interface.

Communication using the serial bus centres around a number of registers internal to the video sensor. These sensor status, set-up, exposure and system information. Most of the registers are read/write allowing the rec change their contents. Others (such as the chip id) are read only.

The main features of the serial interface include:

- Variable length read/write messages.
- Indexed addressing of information source or destination within the sensor.
- Automatic update of the index after a read or write message.
- Message abort with negative acknowledge from the master.
- Byte oriented messages.

The contents of all internal registers accessible via the serial control bus are encapsulated in each start-of-fie 8.3.5.

9.2 Serial Communication Protocol

The co- processor or host must perform the role of a communications master and the camera acts as either transmitter.The communication from host to camera takes the form of 8-bit data with a maximum serial clock f to 100 kHz. Since the serial clock is generated by the bus master it determines the data transfer rate. Data tr the bus is illustrated in Figure 35.

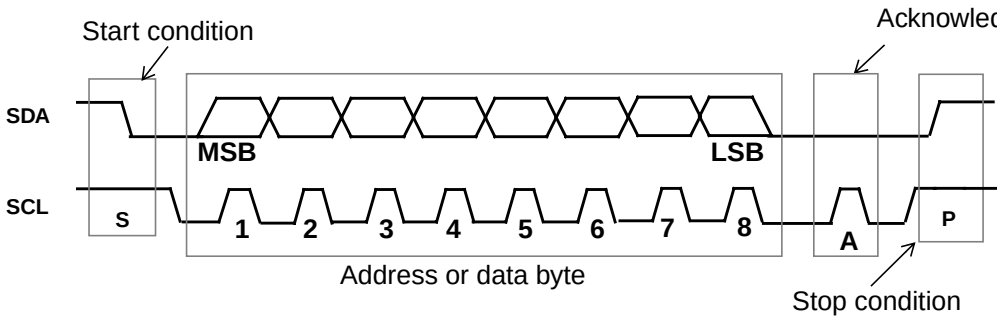


Figure 35 : Serial Interface Data Transfer Protocol

9.3 Data Format

Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit. The internal data is pr *sda* at a rising edge of *scl*. The external data must be stable during the high period of *scl*. The exceptions to *stop* (P) conditions when *sda* falls or rises respectively, while *scl* is high.

A message contains at least two bytes preceded by a *start* condition and followed by either a *stop* or *repeate* by another message.

The first byte contains the device address byte which includes the data direction *read,* (r)*, ~write*, (~w), bit. Th byte indicates the direction of the message. If the lsb is set high then the master will read data from the slave a low then the master will write data to the slave. After the *r, ~w* bit is sampled, the data direction cannot be cha address byte with a new *r, ~w* bit is received.

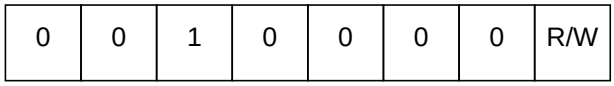


Figure 36 : VV5410/VV6410's Serial Interface Address

The byte following the address byte contains the address of the first data byte (also referred to as the *index*). can address up to 128, byte registers. If the msb of the second byte is set the automatic increment feature of selected.

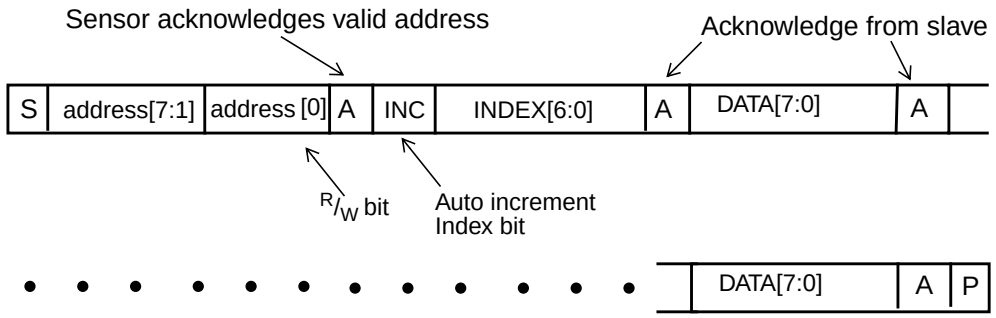


Figure 37 : Serial Interface Data Format

9.4 Message Interpretation

All serial interface communications with the sensor must begin with a *start* condition. If the *start* condition is f address byte then further communications can take place. The sensor will acknowledge the receipt of a valid the *sda* wire low. The state of the *read/~write* bit (lsb of the address byte) is stored and the next byte of data can be interpreted.

During a write sequence the second byte received is an address index and is used to point to one of the inte msbit of the following byte is the *index auto increment* flag. If this flag is set then the serial interface will auto the index address by one location after each slave acknowledge. The master can therefore send data bytes slave until the slave fails to provide an acknowledge or the master terminates the write communication with a sends a *repeated start*, *(Sr).* If the auto increment feature is used the master does *not* have to send indexes data bytes.

As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has be slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current

During a read message, the current index is read out in the byte following the device address byte. The next slave device are the contents of the register addressed by the current index. The contents of this register are into the serial/parallel register and clocked out of the device by *scl.*

At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receivi VV5410/VV6410 is always considered to be a slave device, it acts as a transmitter when the bus master requ sensor.

At the end of a sequence of incremental reads or writes, the terminal index value in the register will be one *g* location read from or written to. A subsequent read will use this index to begin retrieving data from the intern

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start co negative acknowledge after reading a complete byte during a read operation.

9.5 The Programmers Model

There may be up to 128, 8-bit registers within the camera, accessible by the user via the serial interface. The

according to function with each group occupying a 16-byte page of the location address space. There may b groups, although this scheme is purely a conceptual feature and not related to the actual hardware implemen categories are given below:

- Status Registers (Read Only).
- Setup registers with bit significant functions.
- Exposure parameters that influence output image brightness.
- System functions and analog test bit significant registers.

Any internal register that can be written to can also be read from. There are a number of read only registers status information, (e.g. design revision details).

Names that end with H or L denote the most or least significant part of the internal register. Note that unused byte are packed with zeroes.

STMicroelectronics sensors that include a 2-wire serial interface are designed with a common address spac parameter is unused in a design, but has been allocated an address in the generic design model, the locatio ***reserved***. If the user attempts to read from any of these ***reserved or unused*** locations a default byte will be VV5410/VV6410 this data is 19_H. A write instruction to a reserved (but unused) location is illegal and would n the device would not allocate an internal register to the data word contained in the instruction.

A detailed description of each register follows. The address indexes are shown as decimal numbers in brack expressed in decimal and *hexadecimal* respectively.

$Index_{10}$	$Index_{16}$	Name	Length	R/W	Default	Commen
Status Registers - [0-15]						
0	0	deviceH	8	RO	0001_1001_2	Chip identification numb revision indicator
1	1	deviceL	8	RO	1010_0000_2	
2	2	status0	8	RO	0001_0000_2	User can determine wh serial interface data has consumed by interrogat
3	3	line_countH	8	RO	n/a	Current line counter val
4	4	line_countL	8	RO	n/a	
5	5	xendH	1	RO	359	End x coordinate of ima
6	6	xendL	8	RO		
7	7	yendH	1	RO	293	End y coordinate of ima
8	8	yendL	8	RO		
9	9	dark_avgH	4	RO	0	This is the average pixe
10	A	dark_avgL	8	RO	0	returned from the dark l cancellation algorithm (2's complement notatio
11	B	black_avgH	4	RO	0	This is the average pixe
12	C	black_avgL	8	RO	0	returned from the black cancellation algorithm (2's complement notatio
13	D	status1	2	RO	00	Flags to indicate wheth image coordinates have
14-15	E-F	unused				
Setup Registers - [16-31]						

Table 19 : Serial Interface Address Map.

$Index_{10}$	$Index_{16}$	Name	Length	R/W	Default	Commen
16	10	setup0	8	R/W	0000_1001_2	Low-power/sleep mode timing
17	11	setup1	8	R/W	1100_0000_2	Various parameters
18	12	sync_value	8	R/W	0001_1111_2	Contains pixel counter used by external sync
19	13	reserved				
20	14	fg_modes	8	R/W	0000_0000_2	Frame grabbing modes (FST, LST and QCK)
21	15	pin_mapping	7	R/W	000_1000_2	FST and QCK mapping
22	16	data_format	8	R/W	0000_0001_2	Data resolution
23	17	op_format	7	R/W	001_1000_2	Output coding formats
24	18	mode_select	2	R/W	01_2	Various mode select bit
25 - 31	19-1F	unused				
Exposure Registers - [32-47]						
32	20	fineH	2	R/W	0	Fine exposure.
33	21	fineL	8	R/W		
34	22	coarseH	2	R/W	302	Coarse exposure
35	23	coarseL	8	R/W		
36	24	analog gain	8	R/W	1111_0000	Analog gain setting
37	25	clk_div	4	R/W	0	Clock division
38-43	26-2B	reserved				
44	2C	dark offsetH	3	R/W	0	dark line offset cancella
45	2D	dark offsetL	8	R/W		(2's complement notatio
46	2E	dark offset setup	7	R/W	$0110\ 0001_2$	dark line offset cancella
47	2F	reserved				
Colour Registers - [48-79]						
48 - 79	30-4F	reserved	8	R/W		
Video Timing Registers - [80-103]						
80-81	50-51	reserved				
82	52	line_lengthH	2	R/W	415	Line Length (Pixel Cloc
83	53	line_lengthL	8	R/W		
84 - 86	54-56	reserved				
87	57	x-offsetH	1	R/W	5	x-co-ordinate of top left region of interest (x-offs
88	58	x-offsetL	8	R/W		
89	59	y-offsetH	1	R/W	3	y-co-ordinate of top left region of interest (y-offs
90	5A	y-offsetL	8	R/W		
91 - 96	5B-60	reserved				
97	61	field_lengthH	2	R/W	319	Field length (Lines)
98	62	field_lengthL	8	R/W		
99-102	63-66	reserved				
103	67	unused		R/W		
Text Overlay Registers - [104-107]						
104 - 105	68-69	reserved				
106 - 107	6A-6B	unused				

Table 19 : Serial Interface Address Map.

$Index_{10}$	$Index_{16}$	Name	Length	R/W	Default	Commer
Serial Interface Autoload Registers - [108-111]						
108 - 109	6C-6D	reserved				
110 - 111	6E-6F	unused				
System Registers - [112-127]						
112	70	black offsetH	3	R/W	- 64	black offset cancellatio
113	71	black offsetL	8	R/W		(2's complement notati
114	72	black offset setup	6	R/W	$0011\ 0001_2$	black offset cancellatio
115	73	unused				
116	74	reserved				
117	75	cr0	8	R/W	$0000\ 0000_2$	Analog Control Registe
118	76	cr1	8	R/W	$0000\ 0000_2$	Analog Control Registe
119	77	as0	8	R/W	$0101\ 1010_2$	ADC Setup Register
120	78	at0	8	R/W	$0000\ 0000_2$	Analog Test Register
121	79	at1	8	R/W	$0000\ 0001_2$	Audio Amplifier Setup F
122 - 125	7A-7D	unused				
126	7E	reserved				
127	7F	reserved				

Table 19 : Serial Interface Address Map.

9.5.1 Status Registers - [0 - 15],*[0-F]*

[0-1],*[0-1]* - DeviceH and DeviceL

These registers provide read only information that identifies the sensor type that has been coded as a 12bit mask set revision identifier. The device identification number for VV5410/VV6410 is 410 i.e. 0001 1001 1010 revision identifier is 0 i.e. 0000_2.

Bits	Function	Default	Comment
7:0	Device type identifier	$0001\ 1001_2$	Most significant 8 bits of the 12 bit code id chip type.

Table 20 : [0],*[0]* - DeviceH

Bits	Function	Default	Comment
7:4	Device type identifier	1010_2	Least significant 4 bits of the 12 bit code i chip type.
3:0	Mask set revision identifier	0000_2	

Table 21 : [1],*[1]* - DeviceL

[2],*[2]* - Status0

Bit	Function	Default	Comment
0	Fine exposure value update pending	0	Fine exposure value sent but not yet cor sensor

Table 22 : [2],*[2]* - Status0

Bit	Function	Default	Comment
1	Coarse exposure value update pending	0	Coarse exposure value sent but not yet the sensor
2	Gain value update pending	0	Gain value sent but not yet consumed b
3	Clock division update pending	0	Clock divisor sent but not yet consumed
4	Odd/even frame	1	The flag will toggle state on alternate fra
5	Pan image parameters pending	0	Pan image parameters sent but not yet the sensor
6	Tilt image parameters pending	0	Tilt image parameters sent but not yet c the sensor
7	Video timing parameter update pending flag	0	Video timing parameters sent but not ye by sensor

Table 22 : [2],*[2]* - Status0

[3-4],*[3-4]* - Line_countH & Line_countL

Register Index	Bits	Function	Default	Comment
3	0	Current line count MSB	-	Displays current line cour
4	7:0	Current line count LSB	-	

Table 23 : [3-4],*[3-4]* - Current Line Counter Value.

[5-6],*[5-6]* - XendH & XendL

Register Index	Bits	Function	Default	Comment
5	0	Xend msb's	359	These registers contain th coordinate of the read ou (the x offset register conta coordinate)
6	7:0	Xend ls byte		

Table 24 : [5-6],*[5-6]* - Xend

[7-8],*[7-8]* - YendH & YendL

Register Index	Bits	Function	Default	Comment
5	0	Yend ms bits	293	These registers contain th coordinate of the read ou (the y offset register conta coordinate)
6	7:0	Yend ls byte		

Table 25 : [7-8],*[7-8]* - Yend

[9-12],*[9-C]* - Black_Avg & Dark_Avg

Register Index	Bits	Function	Default	Comment
9	3:0	Dark avg ms bits	0	The calculated pixel average o series of dark lines (1,2 or 4 li pixel sample size from each d will be image size dependent maximum of 256 The average value is a signed number
10	7:0	Dark avg ls byte	0	
11	3:0	Black avg ms bits	0	The calculated pixel average o series of black lines (4 or 8 lin pixel sample size from each b will be image size dependent maximum of 256 The average value is a signed number
12	7:0	Black avg ls byte	0	

Table 26 : [9-12],*[9-C]* - Black & Dark Averages

[13],*[D]* - Status1 Register

Bit	Function	Default	Comment
0	X image parameters clipped	0	If this bit is set then the current x offs requested has caused the x coordina clipped
1	Y image parameters clipped	0	If this bit is set then the current y offs requested has caused the y coordina clipped
7:2	unused	000000	

Table 27 : [13],*[D]* - Status1

[14-15],*[E-F]* - unused

9.5.2 Setup Registers - [16 - 31],*[10-1F]*

[16],*[10]* - Setup0

[

Bit	Function	Default	Comment
0	Low Power Mode: Off / **On**	1	Powers down the sensor array. The out goes to F_H. On power-up the sensor ent mode.
1	Sleep Mode: **Off** / On	0	Puts the sensor array into reset. The ou goes to F_H.

Table 28 : [16],*[10]* - Setup0

Bit	Function	Default	Comment
2	Soft Reset **Off** / On	0	Setting this bit resets the sensor to its p defaults. This bit is also reset.
3	Frame/Field Rate select: 25 fps (PAL) / **30 fps (NTSC)**	1	
5:4	reserved	00	
7:6	Video Timing Mode Select	00	**00 - CIF Timing Modes** 01 - PAL/NTSC 3.2 fsc Timing Modes 10 - pan/tilt/QCIF Timing Modes *If this mode is selected a QCIF size output. The coordinates which define corner of the QCIF portion of the array are defined by the parameters in reg inclusive. By default the x- and y-sizes image are180 & 148 respectively.* 11 - sub-sampled QCIF Timing Modes *If this mode is selected a QCIF size output. The CIF image is sub-sampled to preserve the Bayer pattern with every of pixels & lines skipped.*

Table 28 : [16],*[10]* - Setup0

Video Mode	setup0 [7:6]	setup0 [3]	System Clock Divisor	Video Data	Line Length	Field Length	Data Format (default)	Comment
1	00	0	4	356 x 292	500	320	5-wire	CIF 25fps
2		1	4	356 x 292	416	320	5-wire	CIF 30fps
3	01	0	2	356 x 292	454	312/313	5-wire	PAL (3.2 fs
4		1	2	306 x 244	364	262/263	5-wire	NTSC (3.2
5	10	0	8	180 x 148	250	160	5-wire	pan/tilt QC
6		1	8	180 x 148	208	160	5-wire	pan/tilt QC
7	11	0	8	180 x 148	250	160	5-wire	sub-sampl
8		1	8	180 x 148	208	160	5-wire	sub-sampl

Table 29 : Video Timing Modes

[17],*[11]* - Setup1

Bit	Function	Default	Comment
2:0	reserved	000	
3	Enable immediate clock division update. **Off**/On	0	Allow manual change to clock divis applied immediately
4	Enable immediate gain update. **Off**/On	0	Allow manual change to gain to be immediately

Table 30 : [17],*[11]* - Setup1

Bit	Function	Default	Comment
5	Enable additional black lines (lines 3-8) **Off**/On	0	If enabled this bit will also enable t immediately following the end of fra bit can only set/reset if the VP3 mo been selected. In VP3 mode (OFF) possible black lines are always ou
6	reserved	1	
7	Pixel read-out order (hshuffle) Unshuffled or **Shuffled**	1	It is strongly recommended to use horizontal read-out with VV6410 s

Table 30 : [17],*[11]* - Setup1

[18],*[12]* - sync_reset

Bit	Function	Default	Comment
7:0	Pixel counter reset value	31	During synchronisation the pixel co reset to the known value or offset pck's into the pixel count sequence.

Table 31 : [18],*[12]* - sync_reset

[19],*[13]* - reserved

[20],*[14]* - fg_modes

Bits [3:2] of the fg_mode register are mode dependent. If the NTSC or PAL video modes are selected then th mode will be selected. The slow QCK is selected by default, regardless of the video mode.

Bit	Function	Default	Comment
1:0	FST/QCK pin modes	00	Selection of FST, QCK pin data
3:2	QCK modes	00	00 - if CIF & QCIF mode selected 01 - if NTSC and PAL mode selecte
5:4	LST modes	00	See Table 35 below for details
7:6	FST modes	00	See Table 36 below for details

Table 32 : [20],*[14]* - fg_modes

fg_mode[1:0]		FST pin	QCK pin
0	0	FST	Slow QCK
0	1	FST	Fast QCK
1	0	Fast QCK$_{\textbf{note1}}$	Slow QCK
1	1	Invert of Fast QCK$_{\textbf{note1}}$	Fast QCK

Table 33 : FST/QCK Pin Selection

note1: The FST pin will always output the free running version of QCK (either inverted or normal)

fg_mode[3:2]		QCK state
0	0	Off
0	1	Free Running
1	0	Valid during data and control period of line
1	1	Valid only during data period of line

Table 34 : QCK Modes

fg_mode[5:4]		LST pin
0	0	Off
0	1	Free Running
1	0	Output for black, video data and status lines
1	1	Output only for black and video data lines.

Table 35 : LST Modes

.

fg_mode[7:6]		FST pin
0	0	Off
0	1	Normal behaviour, FST will qualify the visible pixe the status line
1	x	Special digital stills mode. FST will be asserted at beginning of valid data on the line following the E line. FST will be cleared at the end of the visible p els in the following status line.

Table 36 : FST Modes

The option to enable the qclk during the data and control period of the line ***must not be selected if monoch unshuffled) video has been selected.***

[21],*[15]* - pin_mapping

Bit	Function	Default	Comment
0	Map serial interface register bits values on to the QCK and FST pins **Off**/On	0	
1	Serial Interface Bit for QCK pin	0	
2	Serial Interface Bit for FST pin	0	
4:3	Output driver strength select	00	Default setting selects 2mA driver

Table 37 : [21],*[15]* - pin_mapping

Bit	Function	Default	Comment
5	Enable RESETB pin as SIN **Off** / On	0	On power up the RESETB pin is co active low system reset which will sy video timing logic and reset all seri their default state. Setting this bit RESETB pin as an active synchronisation signal (SIN) synchronise the video timing but will serial registers.
7:6	unused	0	

Table 37 : [21],*[15]* - pin_mapping

Mapping Enable	FST pin	QCK pin
0	FST	QCK
1	pin_mapping[2]	pin_mapping[1]

Table 38 : FST/QCK Pin Selection

oeb_composite	pin_map[4]	pin_map[3]	Comments
0	0	0	Drive strength = 2mA (Default)
0	0	1	Drive strength = 4mA
0	1	0	Drive strength = 6mA
0	1	1	unallocated
1	x	x	Outputs are not being driven th driver strength is irrelevant

Table 39 : Output driver strength selection

[22],*[16]* - data_format

Bit	Function	Default	Comment
1:0	Unused	1	
2	Line read-out order (vertical) **Unshuffled** or Shuffled	0	If the line read out is shuffled then all the e rows will be read out first followed by all th address rows
3	Pixel read-out order (hmirror) **Normal** or Mirrored	0	If the pixel read out is horizontally mirrore columns are read out in reverse order, tha column on the right of the sensor array wi the left of the displayed image and vice ve
4	Line read-out order (vertical flip) **Normal** or Mirrored	0	If the line read out is vertically mirrored th are read out in reverse order, that is the ro bottom of the array will appear at the top o displayed image and vice versa.

Table 40 : [22],*[16]* - data_format

Bit	Function	Default	Comment
5	FST/LST **Enable**/Tri-state	0	The FST/LST digital outputs can be tri-s enabled as outputs by default. The enab of FST/LST can be retimed to a field b state of this control bit is always availabl interface read, i.e. it does not have to w state at a field boundary
6	QCK **Enable**/Tri-state	0	The QCK output can be tri-stated indepe enabling/disabling of QCK can be retim boundary. The state of this control bit is a ble via a serial interface read, i.e. it does wait to change state at a field boundary.
7	Pre clock generator divide On/**Off**	0	The CIF and QCIF video modes expe mended set of input clock frequencies, acceptable range of clock frequencies can if this bit is set. If this bit is set then the clock will be divided down by 1.5 prior to t erator, thus if the expected clock input is can set this bit and accept 24 MHz and same final frame rate.

Table 40 : [22],*[16]* - data_format

OEB pin	data_format[5]	oeb_composite	Comments
0	0	0	FST/LST outputs enabled.
0	1	1	FST/LST outputs are tri-stated b data_format[5]
1	0	1	FST/LST outputs are tri-stated b
1	1	1	FST/LST outputs are tri-stated.

Table 41 : FST/LST output control

OEB pin	data_format[6]	oeb_composite	Comments
0	0	0	QCK output enabled.
0	1	1	QCK output is tri-stated by op_f
1	0	1	QCK output is tri-stated by OEB
1	1	1	QCK output is tri-stated.

Table 42 : QCK output control

[23],*[17]* - op_format

Bit	Function	Default	Comment
1:0	Data format select.	0	**00 - 5 wire parallel output** 01 - 4 wire parallel output 1x - 8 wire parallel output *Note: If the 8 wire output option has been the FST and LST pins will output data respectively, normal FST and LST fu available*
2	Embedded SAV/EAV Escape Sequences[1] **On /** Off	0	**0 - Insert Embedded Control Sequenc and End of Active Video into Output Vi** 1 - Pass-through mode. Output Video data data.
4:3	reserved	11	
5	Tri-state output data bus **Enabled** / Tri-state	0	On power up the data bus pads are enable This bit is OR'ed with the OEB pin to gene enable signal for the data pins as detailed
6	Re-time tri-state update. **Off** / On	0	Re-time new tri-state value to a field boun affects the updating of the op_format[5] as data_format[6:5]
7	unused	0	

Table 43 : [23],*[17]* - op_format

1. **Please note that if the embedded coding sequences are disabled then the FST signal is also disable output will continue to function IF the free running option has been selected. The LST functionality is by the state of this bit.**

OEB pin	op_format[5]	oeb_composite	Comments
0	0	0	Data outputs enabled.
0	1	1	Data outputs are tri-stated by op_
1	0	1	Data outputs are tri-stated by OE
1	1	1	Data outputs are tri-stated.

Table 44 : Data bus output control

Note: oeb_composite is the logical OR of op_format[5] and the OEB pin.

[24],*[18]* - mode_select

This register allows the user to configure the sensor to operate with the present generation of coprocessors a future devices.

Bit	Function	Default	Comment
0	Coprocessor device is VP3 No/**Yes**	1	By default the sensor expects the coproc VP3 device. If the sensor is not being use device then this bit should be reset. Thi the arrangement of black/dark/visible lin field. It does not alter timing. Please see

Table 45 : [24],*[18]* - Mode Select

Bit	Function	Default	Comment
1	Retro mode for gain application **Off**/On	0	The gain passed to the CAB comprises 2 IDAC[3:0] and CDAC[5:0]. If the user sel mode then the IDAC value will be the inv gain nibble. The user is barred from writi gain nibble. In the non retro mode all 8 bi ble to program. The 2 ls bits of CDAC[5:0 2'b11.
2	Select log CDAC ramp **Off**/On	0	By default the same CDAC value is ap duration of every line of every field. Se causes the CDAC value to be varied durin
7:3			

Table 45 : [24],*[18]* - Mode Select

[25-31],*[19-1F]* - unused

9.5.3 Exposure Control Registers [32 - 47],*[20-2F]*

There is a set of programmable registers which controls the sensitivity of the sensor. The registers are as fol

1. Fine exposure.
2. Coarse exposure.
3. Analog gain.
4. Clock division

Note*:* As we know from an explanation earlier in this document (see Section 6. for further details) the registers are not updated immediately, rather they are timed to be updated at a precise point in the fi

The range of some parameter values is limited and any value programmed out-with this range will be clipped currently permitted, (the fine and coarse maximum allowable settings are set by the current line and field len

$Index_{10}$	$Index_{16}$	Bits	Function	Default	Comm
32	20	0	Fine MSB exposure value	0	The maximum fine ex length dependent. Th used to calculate the exposure for each of video modes, that ca via Setup0 register, a NTSC = line length - PAL = line length - 86 CIF = line length - 51 QCIF = line length - 2
33	21	7:0	Fine LSB exposure value		

$Index_{10}$	$Index_{16}$	Bits	Function	Default	Comm
34	22	0	Coarse MSB exposure value	302	The maximum allowa exposure setting is fi dependent. We provi maximum coarse exp for each of the standa modes. NTSC = 260 PAL = 310 CIF (25 & 30 fps) = 3 QCIF (25 & 30 fps) =
35	23	7:0	Coarse LSB exposure value		
36	24	7:0	Analog gain value	1111_0000	Bits [7:4] CDAC gain CDAC default = 63 (1 CDAC default = 31 (9 Bits[3:0] IDAC maxim recommended IDAC
37	25	3:0	Clock divisor value	0	The user can opt to s clocks down form the settings. Table 47 de range of clock divisor selected.

Table 46 : Exposure Related Registers

Clock Divisor Setting	Pixel Clock Divisor
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14
1110	15

Table 47 : Clock Divisor Values

Clock Divisor Setting	Pixel Clock Divisor
1111	16

Table 47 : Clock Divisor Values

[38-43],*[26-3B]* - reserved

[44 - 45],*[3C-3D]* - Dark Pixel Offset

Bit	Function	Default	Comment
2:0	MS Dark line pixel offset	0	This register contains a fixed offs be applied to the digitised pixels i ital output coding block. The offse complement number, giving an of -1024,+1023. If this external offset cancellation applied then it register[46], bits[1: be reprogrammed to 2'b1x.
7:0	LS Dark line pixel offset		

Table 48 : [44 - 45],*[3C-3D]* - Dark Pixel Offset

[46],*[3E]* - Dark Pixel Cancellation Setup Register

Bit	Function	Default	Comment
1:0	Dark line offset cancellation	01	x0 - Accumulate dark pixels, ca pixel average and report, but d anything to data stream **01** - Accumulate dark pixels, ca pixel average and report and a internally calculated offset to da 11 - Accumulate dark pixels, ca pixel average and report, but a externally calculated offset
2	Number of dark lines used **All dark lines**/Use half the number of dark lines.	0	The dark line offset cancellatio can opt to only use pixels from that are preceeded by another line choose only line 306 from line 306.
5:3	reserved		
6	Use narrow dark offset deadband **Yes**/No	1	The deadband describes a ran pixel averages that will force th integrator algorithm to hold it's value. 0 - Target +/- 4 codes 1 - Target +/- 2 codes
7	unused	0	

Table 49 : [46],*[3E]* - Dark Pixel Cancellation Setup Register

[47],*[3F]* - reserved

[48-79],*[30-4F]* - reserved

9.5.4 Video Timing Registers [80 - 103],*[50-67]*

Indexes in the range [80 - 103] control the generically named video timing registers, including the image pan
line & field length of the sensor. The registers are as follows:

1. line length.
2. x-offset of region of interest.

3. y-offset of region of interest.
4. frame length.

The length of a line is specified in a number of pixel clocks, whereas the length of a field is specified in a nur

The range of some parameter values is limited and any value programmed out-with this range will be clipped allowed. The x-offset and y-offset are only programmable if the user has selected the pan tilt QCIF mode. If t modes are selected then the x-offset and y-offset registers will have pre-programmed values applied, but the changed. The x-offset and y-offset default values are chosen such that the output image, regardless of video be centered within the pixel array, (see Section 3.2 for details).

$Index_{10}$	$Index_{16}$	Bit	Function	Default	Commen
80-81	50-51		reserved		
82	52	1:0	Line Length MSB value	415	Minimum mode dependen
83	53	7:0	Line Length LSB value		Maximum = 1023 Actual line duration in pixe line length programmed +
84 - 86	54-56		reserved		
87	57	0	x-offset MSB value	5	Minimum (positive) value
88	58	7:0	x-offset LSB value		
89	59	0	y-offset MSB value	3	Minimum (positive) value
90	5A	7:0	y-offset LSB value		
91 - 96	5B-60		reserved		
97	61	1:0	Field Length MSB value	319	Minimum mode dependen
98	62	7:0	Field Length LSB value		Maximum = 1023 Actual field duration in line field length programmed +
99-102	63-66		reserved		

Table 50 : Video Timing Registers

[103],*[67]* - unused

[104-105],*[68-69]* - reserved

[106-107],*[6A-6B]* - unused

[108-109],*[6C-6D]* - reserved

[110-111],*[6E-6F]* - unused

9.5.5 System Registers -Addresses [112 - 127],*[70-7F]*

This page of the serial interface I2C address space comprises a wide range of registers including the register the black offset cancellation algorithm, enable test modes and also control various aspects of the analogue b sensor.

[112 - 113],*[70-71]* - Black Pixel Offset

Bit	Function	Default	Comment
2:0	MS Black line pixel offset	- 64	This register contains a fixed offset that ca the digitised pixels in the digital output coc offset is a 2's complement number, giving -1024,+1023. If this external offset cancellation is to be a register[114], bits[1:0] should be reprogran
7:0	LS Black line pixel offset		

Table 51 : [112 - 113],*[70-71]* - Black Pixel Offset

[114],*[72]* - Black Pixel Cancellation Setup Register

Bit	Function	Default	Comment
1:0	Black line offset cancellation	01	x0 - Accumulate black pixels, c black pixel average and report, apply anything to data stream **01** - Accumulate black pixels, c black pixel average and report internally calculated offset to da 11 - Accumulate black pixels, c black pixel average and report, externally calculated offset
4:2	reserved	100	The time constant controls the a change in the black level is c
5	Use narrow black offset deadband **Yes**/No	1	The deadband describes a rang averages that will cause the lea algorithm to hold it's current va 0 - Target +/- 4 codes 1 - Target +/- 2 codes
7:6	unused	00	

Table 52 : [114],*[72]* - Black offset cancellation setup

[115],*[73]* - unused

[116],*[74]* - reserved

[117 - 118],*[75-76]* - Control Registers 0 and 1- CR0 and CR1

Although we give the user access to the following 5registers it is not anticipated that the contents of these regi altered. If the user does wish to alter any of the register bits then they are strongly advised to contact VIBU b

Bit	Function	Default	Comment
0	Enable bit line clamp **Off**/On	0	
1	Enable bit line test **Off**/On	0	

Table 53 : [117],*[75]* - Control Register CR0

Bit	Function	Default	Comment
3:2	Bit line white reference **0.7 V** / 1.1 V / 1.5V / Ext.	00	00 - 0.7V 01 - 1.1V 10 - 1.5V 11 - External
4	Enable anti blooming **Off**/On	0	
5	Power Down - LVDS input comparator **Off**/On	0	Powers down LVDS input. Cl input may still be used.
6	Power Down - SRAM **Off**/On	0	Powers down SRAM compar
7	Power Down - VCCS **Off**/On	0	Powers down voltage control source

Table 53 : [117],*[75]* - Control Register CR0

Bit	Function	Default	Comment
0	Stand-by **Off**/On	0	Powers down ALL analog cir exception of the band gap
1	Power Down - Internal Ramp Generator **Off**/On	0	
2	Power Down - Column ADC **Off**/On	0	Powers down preamp and co
3	Power Down - CAB regulator **Off**/On	0	Referred to in figures as pd_
4	Power Down - Audio Amplifier regulator **Off**/On	0	Referred to in figures as pd_
5	Power Down - VRT Amplifier **Off**/On	0	Allows external VRT to be ap
6	Ramp common mode voltage **VRT-vtn**/1.5V	0	0 - VRT-vtn ramp common m 1- 1.5V ramp common mode
7	Current boost to column comparator **75uA**/50uA	0	0 - 75uA 1- 50uA

Table 54 : [118],*[76]* - Control Register CR1

[119]*[77]* - ADC Setup Register AS0

Bit	Function	Default	Comment
1:0	reserved	10	

Table 55 : [119],*[77]* - ADC Setup Register AS0

Bit	Function	Default	Comment
2	Enable voltage doubler **Off**/On	0	It is recommended that this bit is is being used in a 3.3V supply e
3	Differential ramp enable Off/**/On**	1	Ramp generator signal bpramp
4	view column/view vcmtcas **vcmtcas**/column	1	0 - view column voltage Vx[363] 1- view vcmtcas
5	ramp viewing/column comparator test **ramps**/test comparator	0	0 -view ramps on CPOS/CNEG 1- input to test comparator 364
6	Stepped Ramp Enable Off**/On**	1	Setting this bit enables a steppe Clearing this bit enables a contir
7			

Table 55 : [119],*[77]* - ADC Setup Register AS0

[120],*[78]* - Analog Test Register AT0

Bit	Function	Default	Comment
0	SRAM test enable **Off**/On	0	
2:1	VRT Voltage **2.2V** / 2.5V / 2.8V / Ext.	00	**00** - VRT = 2.2V 01 - VRT = 2.5V 10 - VRT = 2.8V 11 - reserved
4:3	LineInt & ReadInt phasing	00	**00**- 0 degree phase delay 01 - 90 degree phase delay 10 - 180 degree phase delay 11 - 270 degree phase delay
7:5	unused	000	

Table 56 : [120],*[78]* - Analog Test Register AT0

[121],*[79]* - Audio Amplifier Setup Register AT1

Bit	Function	Default	Comments
0	First stage gain	1	0 - 0dB 1 - 30dB
1	Second stage gain[1]	0	gain[1] gain[0] - gain(dB)
2	Second stage gain[0]	0	0 0 - 0dB 0 1 - 6dB 1 0 - 12dB 1 1 - 18dB
3	Power Down	1	0 - Powered up 1 - Power down
4	Output Select	0	0 - Single ended 1 - Differential
5	Current Boost	0	0 - 1mA output drive in output buffers 1 - 2mA output drive in output buffers
7:6	Unused	00	

Table 57 : [121],*[79]* - Audio Amplifier Setup Register AT1

[122-125],*[7A-7D]* - unused

[126-127],*[7E-7F]* - reserved

9.6 Types of messages

This section gives guidelines on the basic operations to read data from and write data to the serial interface.

The serial interface supports variable length messages. A message may contain no data bytes, one data byt bytes. This data can be written to or read from common or different locations within the sensor. The range of available are detailed below.

- Write no data byte, only sets the index for a subsequent read message.
- Single location data write or read for monitoring (real time control)
- Multiple location read or write for fast information transfers.

Examples of these operations are given below. A full description of the internal registers is given in the previ examples the slave address used is 32_{10} for writing and 33_{10} for reading. The write address includes the rea set to zero while this bit is set in the read address.

9.6.1 Single location, single data write.

When a random value is written to the sensor, the message will look like this:

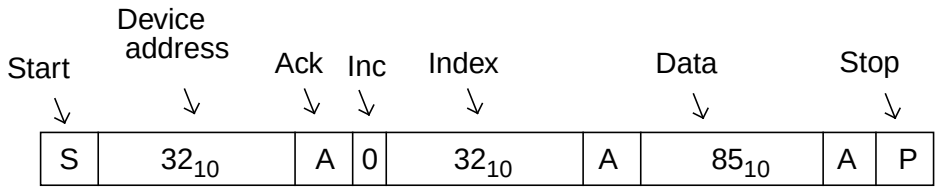


Figure 38 : Single location, single write.

In this example, the *fineH* exposure register (index = 32_{10}) is set to 85_{10}. The r/w bit is set to zero for writing a of the index byte) is set to zero to disable automatic increment of the index after writing the value. The addres and may be used by a subsequent read. The write message is terminated with a stop condition from the mas

9.6.2 Single location, single data read.

A read message always contains the index used to get the first byte.

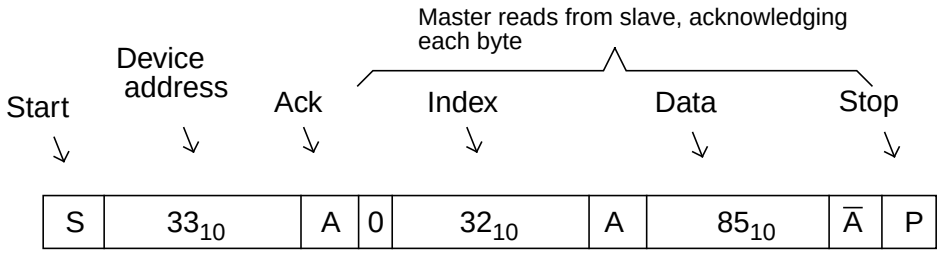


Figure 39 : Single location, single read.

This example assumes that a write message has already taken place and the residual index value is 32_{10}. A v from the *fineH* exposure register. Note that the read message is terminated with a negative acknowledge ($\overline{A}$) f not guaranteed that the master will be able to issue a stop condition at any other time during a read messag the data sent by the slave is all zeros, the *sda* line cannot rise, which is part of the stop condition.

9.6.3 No data write followed by same location read.

When a location is to be read, but the value of the stored index is not known, a write message with no data b first, specifying the index. The read message then completes the message sequence. To avoid relinquishing another master a repeated start condition is asserted between the write and read messages, i.e. no stop con this example, the *gain* value (index = 36_{10}) is read as 15_{10}:

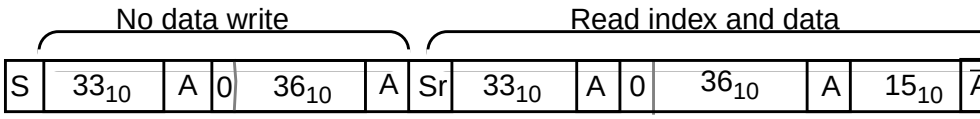


Figure 40 : No data write followed by same location read.

As mentioned in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) fro

9.6.4 Same location multiple data write.

It may be desirable to write a succession of data to a common location. This is useful when the status of a bi must be toggled.

The message sequence indexes *sf_setup* register 108. If bit 0 is toggled high, low this will initiate a fresh aut achieved by writing two consecutive data bytes to the sensor. There is no requirement to re-send the register data byte.

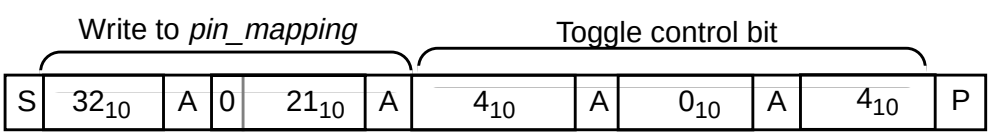


Figure 41 : Same location multiple data write.

9.6.5 Same location multiple data read

When an exposure related value (*fineH, fineL, coarseH, coarse L*, *gain or clk_div*) is written, it takes effect on beginning of the next video frame, (remember that the application of the *gain* value is a frame later than the parameters). To signal the consumption of the written value, a flag is set when any of the exposure or gain re and is reset at the start of the next frame. This flag appears in *status0* register and may be monitored by the speed up reading from this location, the sensor will repeatedly transmit the current value of the register, as lo acknowledges each byte read.

In the below example, a *fineH* exposure value of 0 is written, the status register is addressed (no data byte) a read until the master terminates the read message.

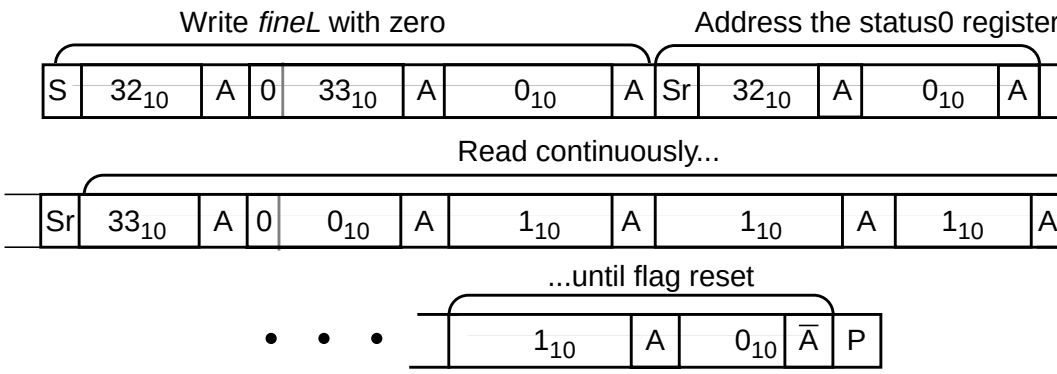


Figure 42 : Same location multiple data read.

9.6.6 Multiple location write

If the automatic increment bit is set (msb of the index byte), then it is possible to write data bytes to consecuti registers, (i.e. 23,24,25,26 etc), without having to send explicit indexes prior to sending each data byte. An aut the exposure registers with their default values is shown in the following example, where we write 17_{10} to the register[21] and 193_{10} to the data format register[22].

.

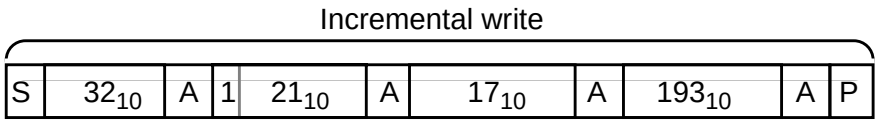


Figure 43 : Multiple location write.

9.6.7 Multiple location read

In the same manner, multiple locations can be read with a single read message. In this example the index is ensure the exposure related registers are addressed and then all six are read.

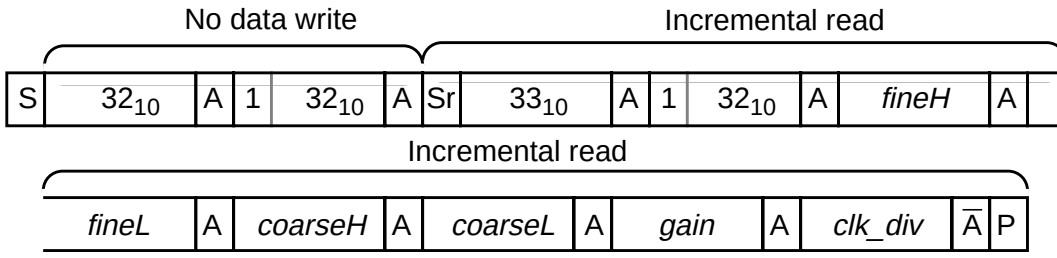


Figure 44 : Multiple location read.

Note: a stop condition is not required after the final negative acknowledge from the master, the sensor will te communication upon receipt of the negative acknowledge from the master.

9.7 Serial Interface Timing

Parameter	Symbol	Min.	Max.
SCL clock frequency	fscl	0	100
Bus free time between a ***stop*** and a ***start***	tbuf	2	-
Hold time for a repeated ***start***	thd;sta	80	-
LOW period of SCL	tlow	320	-
HIGH period of SCL	thigh	160	-
Set-up time for a repeated ***start***	tsu;sta	80	-
Data hold time	thd;dat	0	-
Data Set-up time	tsu;dat	0	-
Rise time of SCL, SDA	tr	-	300
Fall time of SCL, SDA	tf	-	300
Set-up time for a ***stop***	tsu;sto	80	-
Capacitive load of each bus line (SCL, SDA)	Cb	-	200

Table 58 : Serial Interface Timing Characteristics

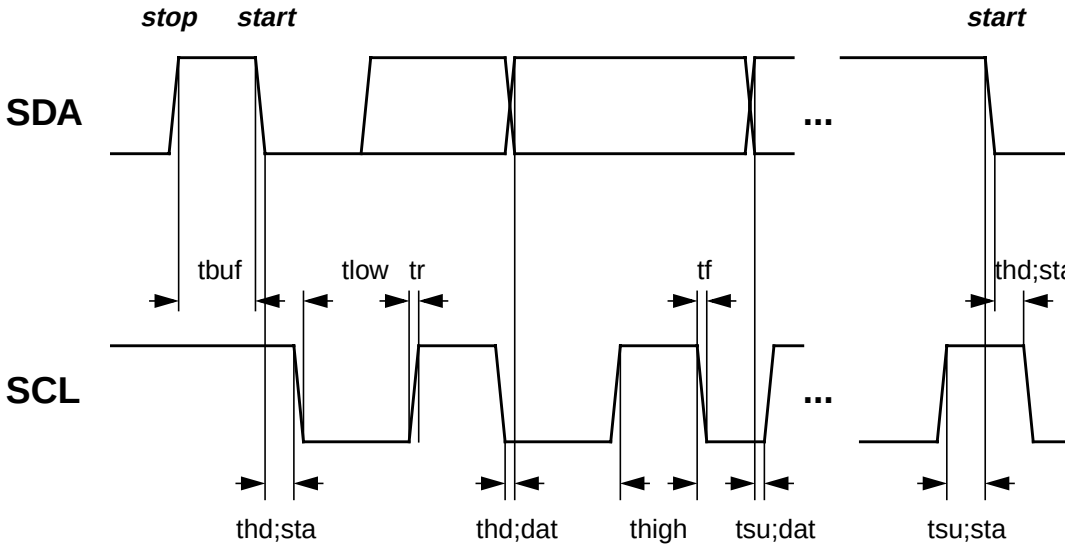


Figure 45 : Serial Interface Timing Characteristics

10. Clock Signal

VV5410/VV6410 system clock is supplied from an external clock source directly driving the CLKI pin. The clo
integral Schmitt buffer to filter noise from the clock source. Please note that there is no support for an extern

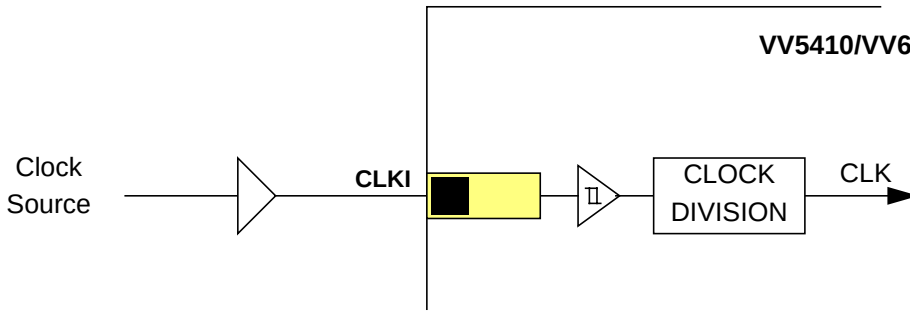


Figure 46 : CMOS Clock Source

The clock signal must be a square wave with, ideally a 50% (10%) mark:space ratio, although a non-ideal m
be tolerated, please contact STMicroelectronics for details. The maximum input clock frequency for the modu
the 24MHz crystal is preferred then the user must select the pre-clock divide by 1.5 option such that the bulk
is driven by a 16MHz clock, see serial interface, register 16_{10}, data_format.

11. Other Features

11.1 Audio Amplifier

VV5410/VV6410 contains an on-chip audio amplifier which can be configured via the serial interface. The am
powered down via the serial interface.

The following document outlines the implementation of audio circuitry on the VV5410/VV6410 sensor.

11.1.1 Audio Amplifier Configuration

The audio circuit is controlled through a single eight bit register on the VV5410/VV6410. This includes bits for
select, first and second stage gains and current boosting. Table 59 describes the functionality of the control

The first stage provides a gain of 0dB or 30dB using a low noise amplifier design.

The reference is provided from the on-chip bandgap voltage. This is buffered by a cut down version of the lo
used in the first gain stage.

Bit	Function	Default	Comments
0	First stage gain	1	0 - 0dB 1 - 30dB
1	Second stage gain[1]	0	gain[1] gain[0] - gain(dB)
2	Second stage gain[0]	0	**0 0 - 0dB** 0 1 - 6dB 1 0 - 12dB 1 1 - 18dB
3	Power Down	0	**0 - Powered up** 1 - Power down
4	Output Select	0	**0 - Single ended** 1 - Differential
5	Current Boost	0	**0 - 1mA output drive in output buffers** 1 - 2mA output drive in output buffers
7:6	Unused		

Table 59 : Control register summary for VV5410/VV6410 audio circuit.

The output of the first gain stage is fed to two output amplifiers. These can be configured with a 1mA or 2mA
The inverting gain stage provides an additional gain between 0dB and 18dB.

The output of the inverting gain stage may be routed through the other output buffer to provide two single en
Otherwise, the inverted and non-inverted outputs provide a fully differential output signal.

Some more circuit specifications may be found in Table 60.

11.1.2 AUD3V3 (Audio Supply Regulator)

Symbol	Parameter	Min	Typical	Max
AUD3V3	Regulated supply (No external load)	3.13	3.3	3.46
AUD3V3_Ld	Regulated supply Vdrop (Current Load 20mA)		-50	
AUD3V3_sus	Regulated supply (Suspend mode)		Off	
ZAUD3V3_sus	Output impedance in Suspend mode		TBC	
PSRR	Power Supply Rejection versus Vin		-48	

Table 60 : Audio Circuit Specification

11.1.3 Audio Amplifier Parameters

Symbol	Parameter	Min	Typical	Max
VAin	Audio Regulator Input Voltage		V_{bg}	
R_{IN}	Input impedance		100	
Gain1	Ist stage (28dB) gain accuracy		+/-0.5	
Gain2	2nd stage (0,6,12,18dB) gain accuracy[1]		+/-0.2	
Gmatch	Differential output mode gain matching (0dB) (28dB)(		 0.2 0.5	
Out_max	Output Clipping Level[2]	1.6	2.2	
OUT_DC	Output DC Voltage	1.1	1.22	1.3
D-OUT_DC	Differential DC Offset (AoutN-AoutP)		20	100
Rout	Output Impedance		2	
THD	THD (includes noise) Vin = 20mVpp, f-1KHz, Gain =28dB		0.2	
SNR	Signal to Noise ratio (1KHz) (10KHz)[3]		 65 75	
PSRR	Power supply rejection ratio from Vin		-55	
LFc	Low frequency cutoff (Cin=100nF)		15	
Xtalk	Video crosstalk to audio outputs (gain = 28dB)		-56	

Table 61 : Audio Amplifier Parameters

1. **2nd stage gain is only available on AoutN with the audio amplifier in differential mode**

2. **Minimum dynamic range includes dcout (i.e. Vclip- OUT_DC is greater than Vppmin/2)**
3. **Assumes 10μF bypass capacitors on all supplies and well separated supplies and grounds**

11.1.4 Audio Amplifier Bandwidth[1]

The audio circuit can be bandwidth limited to a first order, through the use of minimum external circuitry. The and AoutN, require compensation capacitors that may also be used to define the bandwidth of the circuit.

Compensation Capacitor (nF)	3dB Bandwidth	Units
1	175	kHz
10	41	kHz
100	4.2	kHz

Table 62 : Compensation capacitor values

In addition, the inclusion of a resistor (microphone biasing) and decoupling capacitor at the input allows a firs filter to be realised. This can easily be designed to remove frequencies below 50Hz/60Hz (mains electricity r

11.2 Voltage Regulators

VV5410/VV6410 contains three on-chip voltage regulators, two of which are capable of being powered-down interface. The third regulator, controlling the band gap references is never powered down. The band gap circu power consuming only 30μA.

11.2.1 Regulator for Digital System

The output of the regulator, Reg3V3, powers the digital logic and can power an external co-processor. The r up by default. The regulator has its own discrete power supply and can source a load of 300μA -> 150mA ar 3.0V 10% from an input range of 4-6V. When VV5410/VV6410 is in the USB compatible suspend mode, the logic are removed to limit power consumption to approximately 80μA. If an external 3.3V supply is available, be overdriven by an external 3.3V supply to directly power the logic. This voltage regulator is never powered

11.2.2 Regulator for Audio Amplifier

The output of the regulator for the audio amplifier, Aud3V3, drives the load resistor for the microphone and th amplifier. As this regulator is capable of being powered-down via the serial interface, all control signals from low during low power/standby. This regulator will be powered up by default.

11.2.3 Regulator for Video Supply/Analogue Core

The output of the regulator for the video supply,Vid3V3, powers the analog core. This regulator is capable of down via the serial interface but will be powered up by default. Note that the sensor will be in low power mod therefore

11.3 Valid Supply Voltage Configurations

The power supplies to the VV5410 and VV6410 sensors can be configured such that the sensor will operate systems:

- USB system (sensor will regulate the nominal 5V supply to 3V3 internally) with optional BJT to provide po chip.
- Direct drive the sensor with 3V3 (internal voltage regulators will be powered down in this mode).

The next 2figures will detail the options described above:

1. Each audio output must have a capacitor (Ccomp) connected to ground to avoid any oscillation

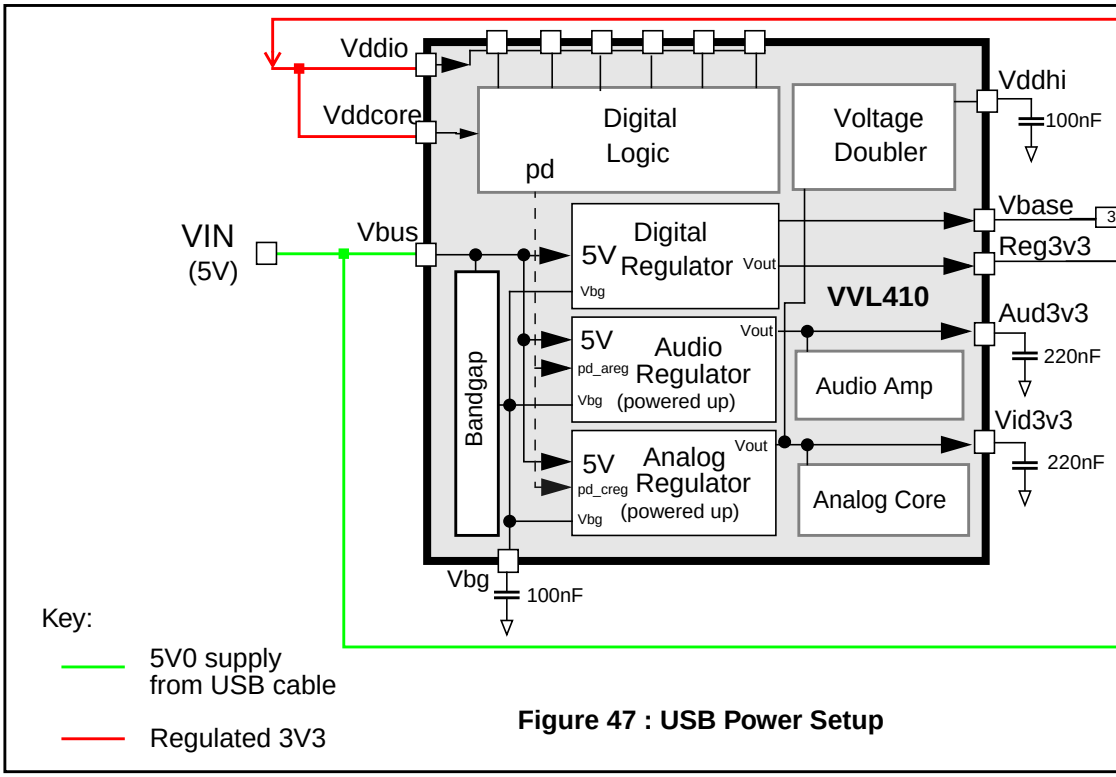


Figure 47 : USB Power Setup

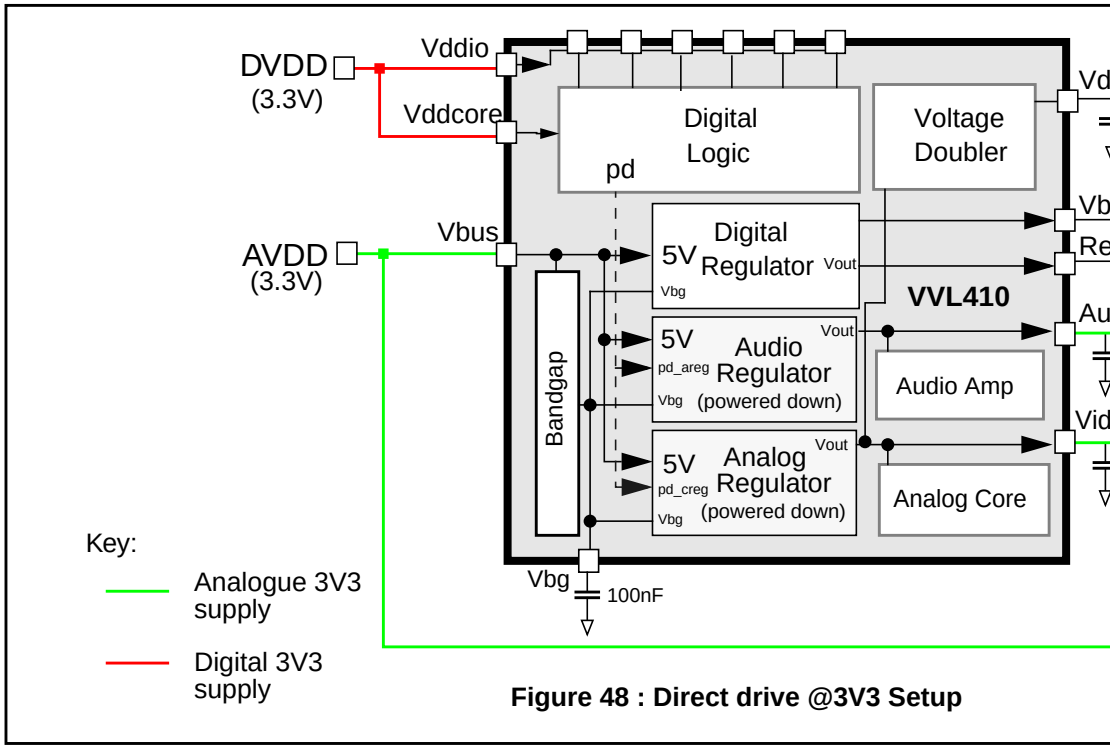


Figure 48 : Direct drive @3V3 Setup

Supply	USB System	3.3V-only System
Vbus	Supply from USB cable	3.3V direct drive
Vddio	connect to Vreg3v3	3.3V direct drive
Vddcore	connect to Vreg3v3	3.3V direct drive
Vreg3v3	optionally populate external BJT for added drive	BJT not populated
Vid3v3	generated by internal regulator	internal regulator powered down
Aud3v3	generated by internal regulator	internal regulator powered down

Table 63 : Sensor Voltage Supply summary

11.4 Programmable Pins

The FST and QCK pins can be re-configured to follow the values of bits 1 and 2 in the serial interface.registe
is to allow remote control of a electro-mechanical system, maybe two different crop settings, in a remote can
serial interface.

12. Characterisation Details

12.1 VV5410/VV6410 AC/DC Specification

Parameter	Comment	Uni
Image Format	356 x 292 pixels (PAL/CIF) 306 x 244 pixels (NTSC) 180 x 148 pixels (QCIF)	-
Pixel Size	7.5 x 6.9	µm
Technology	0.5µm 3 level metal CMOS	-
Array Format	CIF	-
Exposure control range	81 (minimum exposure period 3µs and maximum exposure period is 33ms)[1]	db
Supply Voltage	3.0-6.0 DC +/-10%	V
Operating Temp. range	0 - 40	^{o}C
V_{OL_max}[2]	0.512	V
V_{OH_min}[3]	2.054	V
V_{I_maxL}[4]	0.683	V
V_{IH_min}[5]	2.237	V
Serial interface frequency range	0-100kHz	

1. **We assume CIF (30fps) mode, input clock of 16MHz and internal clock divisor of 1.**
2. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduce**
3. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduce**
4. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduce**
5. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduce**

Table 64 : VV5410/6410 DC specification

12.2 VV5410/VV6410 Optical Characterisation Data

Optical Parameter	Min	Typical	Max	
Dark Current	-	46	-	
Average Sensitivity	-	2.1	-	V
Fixed Pattern Noise (FPN)	-	1.74	-	
Vertical Fixed Pattern Noise (VFPN)	-	1.2	-	
Random Noise	-	1.17	-	
Sensor SNR	-	c.56	-	
Shading (Gross)	-	0.9	-	

Table 65 : VV5410/VV6410 Optical Characterisation Data

12.2.1 Noise Parameters and Dark Current

Various noise parameters are measured on the 410 device as follows:

- Fixed Pattern Noise (FPN)
- Vertical Fixed Pattern Noise (VFPN)
- Random Noise
- Fine Shading
- Gross Shading

The parameters will be described in more detail below along with the data produced by the characterisation

12.2.2 Blooming

Blooming is a phenomenon that does not affect CMOS sensors in the same way as CCD imagers are afflicte blooming can cause an entire column/columns to flood and saturate.

CMOS imagers are however affected by a different type of saturation. If an intense light source, (e.g. Maglite very close proximity to the image sensor the pixel sampling mechanism will break down and rather than disp white light a black image will occur.

The 410 pixel architecture uses Correlated Double Sampling (CDS) to help reduce noise in the system. The p first, yielding the true integrated signal information, then the pixel is reset and very quickly read for a second yields black information - as the pixel has had no exposure time - that can be subtracted from the signal from subtraction will remove much of the noise from the pixel leaving only the useful signal information.

In an example where a pixel has saturated in both the first and the second reads due to an intense light sour cancellation subtraction operation is then performed the result is close to zero signal from the pixel therefore displayed black image.

We do not perform any test measurements for this phenomenon.

12.2.3 Dark Current

This is defined as the rate at which the average pixel voltage increases over time with the device not illuminat will be measured at a gain setting of 4 and a clock divisor of 16 at a fixed temperature and will be expressed

12.2.4 Fixed Pattern Noise

The FPN of an image sensor is the average pixel non-temporal noise divided by the average pixel voltage. T source will be white light that has been IR filtered, producing a diffuse uniform illumination at the surface of t The FPN will be calculated at coarse exposure settings of 0,10,150,250 and 302 with gain set to 1. 10 frame averaged to produce a temporally independent frame before each calculation. FPN will be expressed in mV.

12.2.5 Vertical Fixed Pattern Noise

VFPN describes the spatial noise in an image sensor related to patterns with a vertical orientation. The VFP standard deviation over all columns of the average pixel voltage for each column determined at zero exposu illumination. VFPN will be expressed in mV.

12.2.6 Random Noise

Random noise is the temporal noise component within the image. Random noise will be expressed in mV.

12.2.7 Shading

This describes how average pixel values per “block” change across the image sensor array. For fine shading image sensor array is split into 30 pixel by 30 pixel blocks. An average value is then calculated for each bloc are then compared across the whole device. The blocks are increased in size to 60 pixels by 60 pixels for th calculation. Shading will be expressed in mV.

12.3 VV5410/VV6410 Power Consumption

Operating Condition	Current Consumption
Low power mode current consumption	5.6mA
Sleep mode current consumption[1]	18mA
Suspend mode current consumption (with CLKIP disabled)	85uA
Normal operating mode current consumption[2]	26.2mA

1. **Estimated figures - this parameter was not measured during final characterisation**
2. **Measured while device is clocked at 16MHz and streaming CIF video at 30fps**

Table 66 : VV5410/6410 Current consumption in different modes

12.4 Digital Input Pad Pull-up and Pull-down Strengths

Pad Type	Pads	Min current	Max Current
Library pulldown	suspend	35uA	52uA
Library pullup	scl, sda, oeb	25uA	42uA
Custom pullup	resetb	66uA	250uA

Table 67 : Pad Pull-up/Pull-down Strengths

13. Pixel Defect Specification

13.1 Pixel Fault Definitions

Please find the pixel notation described in Figure 49 below. For the purposes of the test the 3x3 array describ
a common colour, i.e. ALL the pixels will either be Red, Green or Blue. The pixel under test is **X**.

[0]	[1]	[2]
[7]	**X**	[3]
[6]	[5]	[4]

Figure 49 : Pixel Numbering Notation

13.2 Stuck at White Pixel Fault

A pixel is said to be “stuck at white” - it can also be referred to as “hot” - if it is saturated (pixel output at maxi
incident light and exposure set to zero.

13.3 Stuck at Black Pixel Fault

A pixel is said to be “stuck at black” - it can also be referred to as “dead” - if the pixel output is zero even if th
exposed to incident light.

13.4 Column / Row Faults

A line of continuous pixel fails of length > 3 will be described as a row fault in the x-direction and a column fa

If the array contains more than 1 row or column fault and the defective pixels overlap as shown in Figure 50
described as a double row or double column fault respectively. The minimum overlap is 1 pixel. A defective pi
and a good pixel by ‘p’.

n	n+1
X	‘p’
X	‘p’
X	p
X	**X**
‘p’	**X**
‘p’	**X**
‘p’	**X**

Figure 50 : Double Column Fault

In Figure 51 there are 2 column faults however there is no overlap between the 2 columns therefore there ar
faults but no double column faults.

n	n+1
X	‘p’
X	‘p’
X	p
X	‘p’
‘p’	**X**
‘p’	**X**
‘p’	**X**
‘p’	**X**

Figure 51 : Single Column Faults

13.5 Image Array Blemishes

The automatic test programme rejects any sensors that contain blemishes referred to as blobs and clusters (p definitions of these terms) as they cannot be successfully defect corrected by ST coprocessor devices. Up to faults can be corrected and sensors meeting this criteria will PASS this part of the test programme.

13.5.1 Cluster Definition

A failing pixel at **X** with a failing pixel at position [0] or [1] or [2] or [3] or [4] or [5] or [6] or [7] or any combinati positions except the case where all positions are defective. This is a special case and is described below. In Figure 52 there are additional pixel fails in positions [3] and [7].

[0]	[1]	[2]
[**X**]	**X**	[**X**]
[6]	[5]	[4]

Figure 52 : Cluster Example

Blob (special case of cluster):- a failing pixel at position **X** with failing pixels at position [0],[1],[2],[3],[4],[5],[6] 53 below:

[**X**]	[**X**]	[**X**]
[**X**]	**X**	[**X**]
[**X**]	[**X**]	[**X**]

Figure 53 : Blob Example

Single pixel:- a failing pixel with no immediate failing same colour neighbours. Pixels at position [0],[1],[2],[3],[
all valid pixels. Please see Figure 54 below.

[0]	[1]	[2]
[7]	**X**	[3]
[6]	[5]	[4]

Figure 54 : Isolated pixel fail

13.5.2 Summary Pass Criteria

Clusters	Blobs	Row Fails (inc doubles)	Column Fails (inc doubles)	Single pixel
0	0	0	0	<=120

Table 68 : Sensor Pixel Defect Pass Criteria

1. **If there is a non-zero number of clusters, blobs or row/column faults and greater than 120 single pixel defe device will be rejected and classed as a fail.**

14. Pinout and pin descriptions

14.1 36pin CLCC Pinout Map

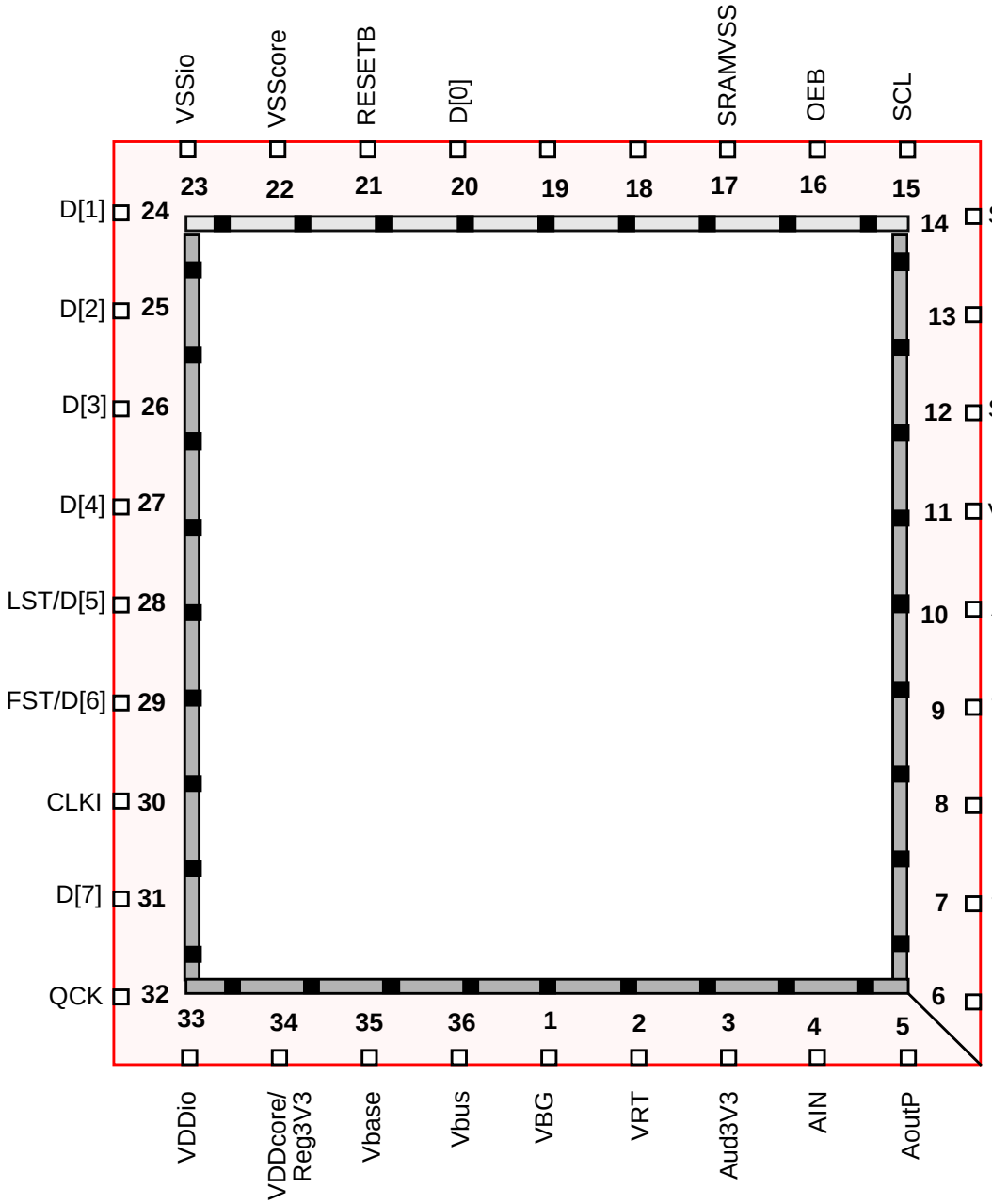


Figure 55 : 36 pin CLCC package pin assignment

Name	Pin Number	Type	Description
POWER SUPPLIES			
AVSS	10	GND	Core analog ground and reference supplies.

Name	Pin Number	Type	Description
SRAMVSS	17	GND	In-column SRAM analog ground.
VDDcore/ Reg3V3	34	PWR	Digital logic power.
VDDio	33	PWR	Digital pad ring power.
VSScore	22	GND	Digital logic ground.
VSSio	23	GND	Digital pad ring ground.
Vid3V3	11	PWR	On-chip Video Supply Voltage Regulator Output
Aud3V3	3	PWR	On-chip Audio Amplifier Voltage Regulator Output
ANALOG SIGNALS			
VBG	1	OA	Internally generated bandgap reference voltage 1.22V
VDDHI	9	IA	Voltage doubler output, 4.6V -> 4.8V
VBase	35	OA	Drive for base of external bipolar
Vbus	36	IA	Incoming power supply 3.3 -> 6V
AIN	4	IA	Analog input to Audio Amplifier
AOutP	5	OA	Analog output of Audio Amplifier (positive)
AOutN	6	OA	Analog output of Audio Amplifier (negative)
PORB	13	OD	Power-on Reset (Bar) Output.
DIGITAL VIDEO INTERFACE			
D[4] D[3] D[2] D[1] D[0]	27 26 25 24 20	ODT	Tri-stateable 5-wire output data bus. - D[4] is the most significant bit. - D[4:0] have programmable drive strengths 2, 4 and 6 m
QCK	32	ODT	Tri-stateable data qualification clock.
LST/D[5]	28	ODT	Tri-stateable Line start output May be configured as tri-stateable output data bit 5 D[5].
FST/D[6]	29	ODT	Tri-stateable Frame start signal. May be configured as tri-stateable output data bit 6 D[6].
D[7]	31	ODT	Tri-stateable Data wire (ms data bit). May be configured as tri-stateable output data bit 6 D[6].
OEB	16	ID↓	Digital output (tri-state) enable.
DIGITAL CONTROL SIGNALS			

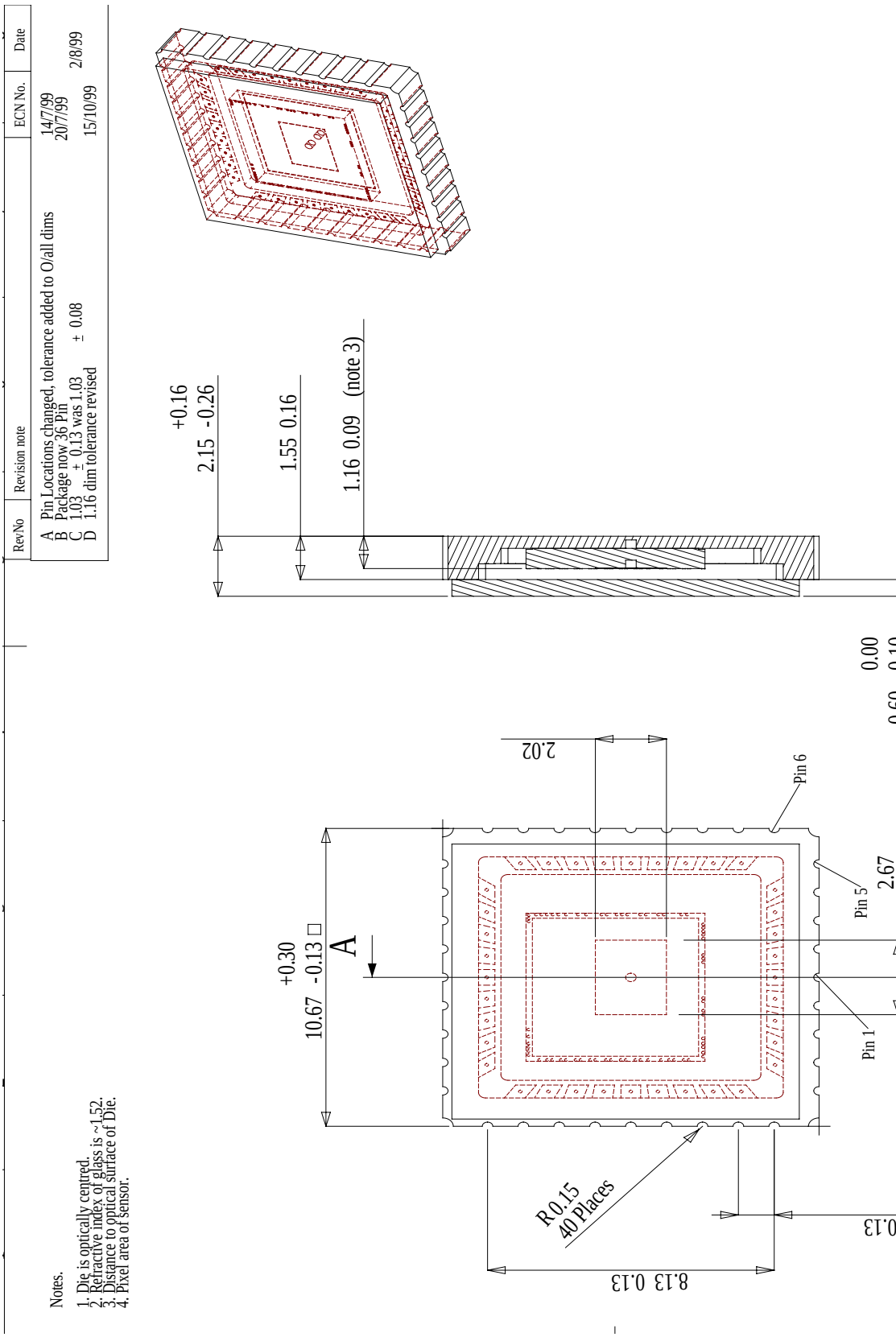
Name	Pin Number	Type	Description
RESETB	21	ID↑	System Reset. Active Low. May be configured as System Sync. Active Low.
SUSPEND	12	ID↑	USB Suspend Mode Control signal. Active High If this feature is not required then the support circuit must ground. The combination of an active high signal and pul chosen to limit current drawn by the device while in susp
SERIAL INTERFACE			
SCL	15	BI↑	Serial bus clock (input only).
SDA	14	BI↑	Serial bus data (bidirectional, open drain).
SYSTEM CLOCKS			
CLKI	30	ID↓	Schmitt Buffered Clock input or LVDS positive Clock inpu

Key			
A	Analog Input	D	Digital Input
OA	Analog Output	ID↑	Digital input with internal pull-up
BI	Bidirectional	ID↓	Digital input with internal pull-do
BI↑	Bidirectional with internal pull-up	OD	Digital Output
BI↓	Bidirectional with internal pull-down	ODT	Tri-stateable Digital Output

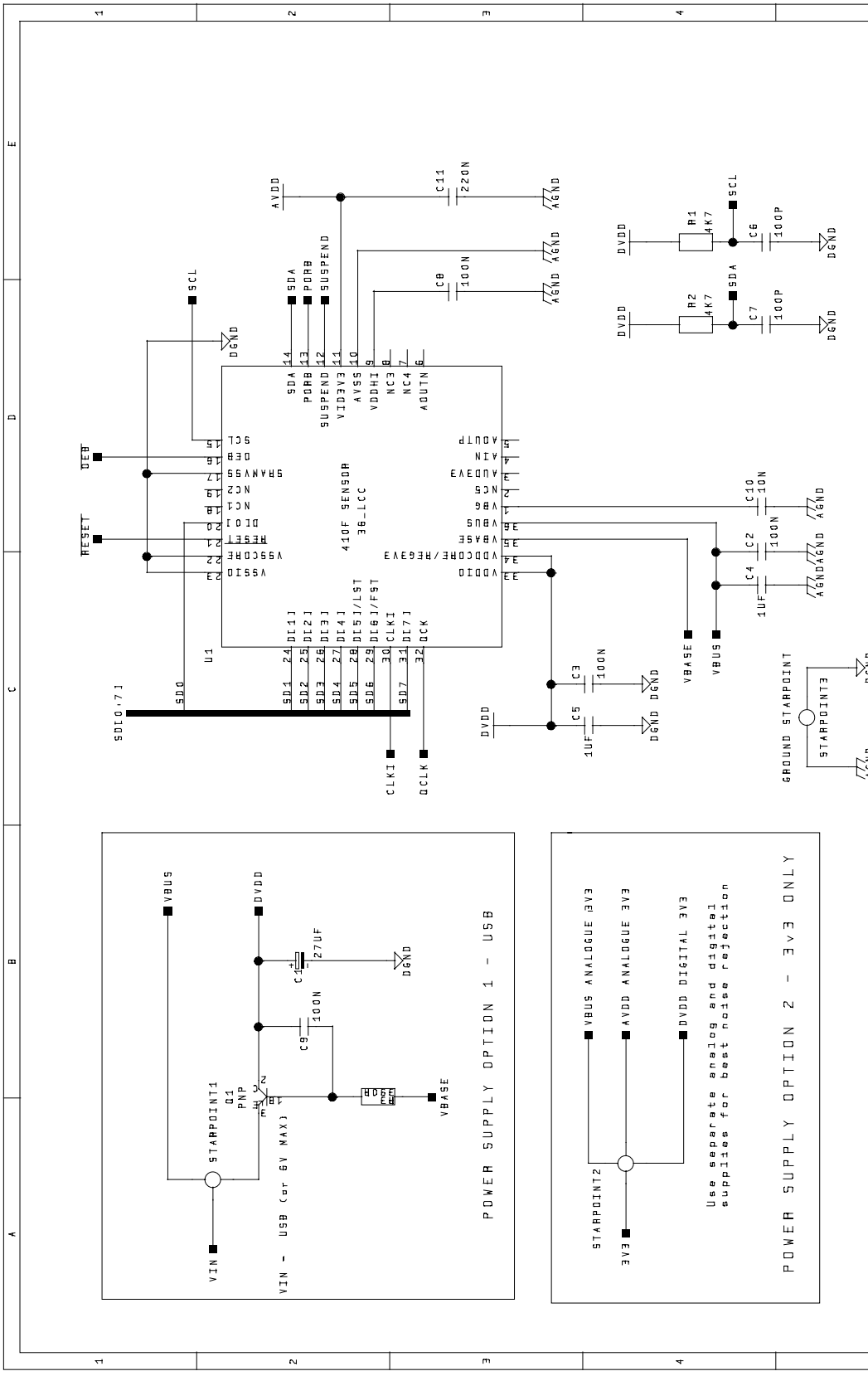
Name	Pin	Type	Description
ANALOG SIGNALS			
Vbloom	8	OA	Anti-blooming pixel reset voltage[1]
VBLTW	7	OA	Bitline test white level reference [2]
VRT	2	IA	Pixel reset voltage[3]

1. **This pin has been removed from the production bonding diagram**
2. **This pin has been removed from the production bonding diagram**
3. **This pin has been removed from the production bonding diagram**

15. Package Details (36pin CLCC)



16. Recommended VV5410/6410 support circuit



17. Evaluation kits (EVK's)

It is highly recommended that an Evaluation Kit (EVK) is used for initial evaluation and design-in of the VV54
VV6410 evaluation kit can now be ordered. Please contact STMicroelectronics for details.

18. Ordering details

Part Number	Description
VV5410C036	36pin CLCC packaged, microlensed CIF monochrome se
VV6410C036	36pin CLCC packaged, microlensed CIF ColourMOS ser
STV0657	YUV/RGB CoProcessor
STV0672	USB companion CoProcessor
STV0680B-001	Digital stills companion CoProcessor
STV-5410-R01	Reference design board for VV6410C036
STV-6410-R01	Reference design board for VV6410C036
STV-USB/CIF-R01	Reference design board for VV6410C036 & STV0672
STV-YUV/CIF-R02	Reference design board for VV6410C036 & STV0657-0
STV-DCA/CIF-R01	Reference design board for VV6410C036 & STV0680B-0
STV-5410/5500-E01	Sensor only evaluation kit for VV6410C036 & VV6500-C0
STV-6410/6500-E01	Sensor only evaluation kit for VV6410C036 & VV6500-C0

Table 69 : VV6410/VV5410 Ordering Details

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