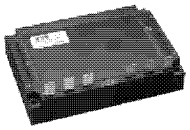
ILC DATA DEVICE CORPORATION®

PW-82351

50 AMP 3-PHASE MOTOR DRIVE



DESCRIPTION

The PW-82351 is a 50 amp, 3-phase motor drive designed to operate with 270 volt motors for use in servo current/torque loop control systems. The PW-82351 has six logic inputs that control the high power transistor switches in the output drive stage. Motor commutation is determined by the switching sequence of the logic inputs. The output power switches enable the motor to rotate by connecting the motor to V_{CC} power and return. Motor current is sensed internally and provided as an isolated scaled output voltage proportional to the motor current for current loop control.

The PW-82351 has a ground isolation barrier between the logic input control stage and output power drive stage. This isolation barrier provides ground noise attenuation from output-to-input and allows the PW-82351 to operate from unipolar or bipolar power supplies.

The output stage has protection from short circuit and over voltage (bus pump-up) conditions. Both protection features have a status flag that is set when a fault condition is detected. The Disable/$\overline{\text{Enable}}$ control input can be used to shut down the drive stage when a flag is detected or to ensure against an uncommanded motion condition.

FEATURES

- ***600 Vdc Drive For 270 V Motors***
- ***Disable / $\overline{\text{Enable}}$ Control***
- ***Internal Commutation Logic***
- ***Ground Isolation Input to Output***
- ***Floating Output Stage***
- ***Motor Current Sense Output***
- ***Output Drive Protection For:***
  - ***Short Circuit***
  - ***Regeneration***

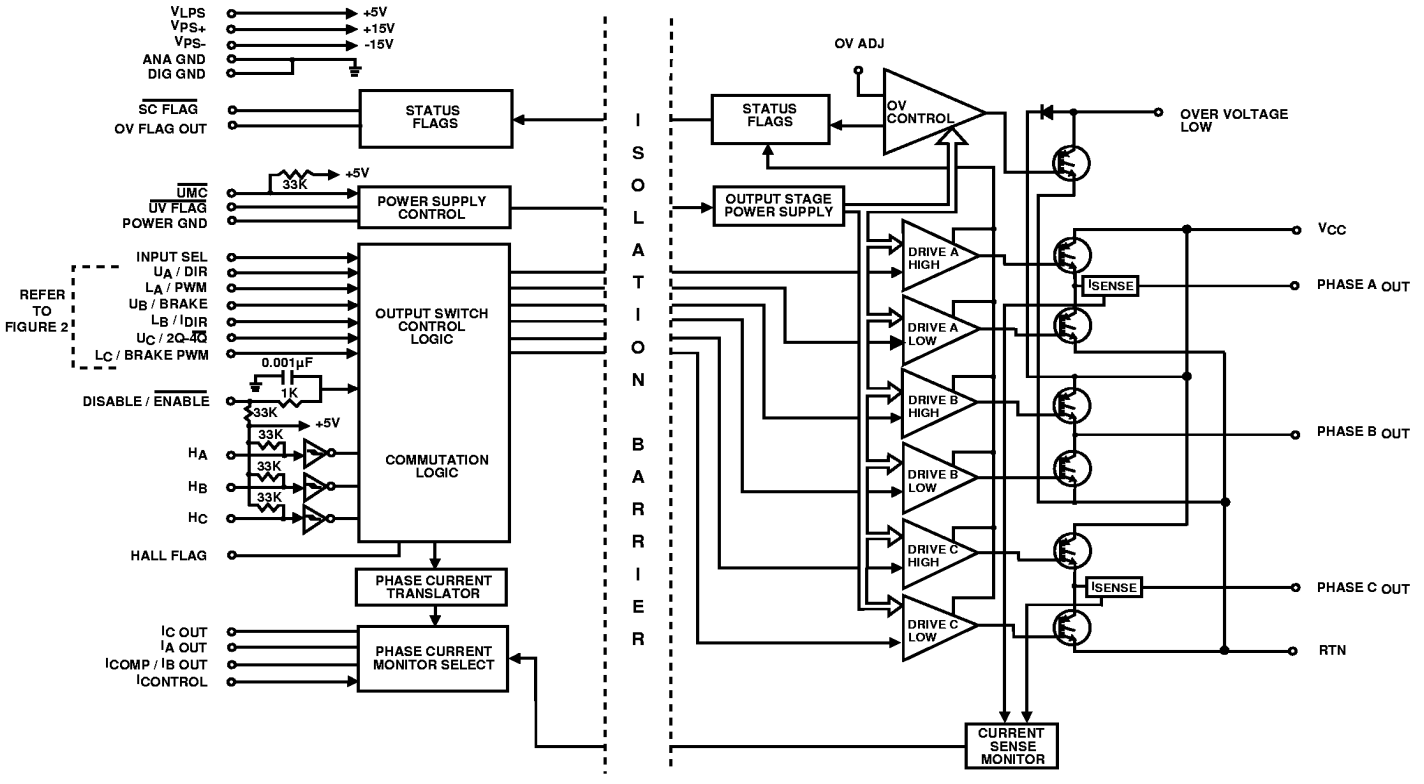


FIGURE 1. PW-82351P6 BLOCK DIAGRAM

TABLE 1. PW-82351 ABSOLUTE MAXIMUM RATINGS
(TC = +25°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	VALUE	UNITS
Drive Supply Voltage	Vcc	600	Vdc
Signal Supply Voltage	V_{PS}	±18	Vdc
Logic Power-In Supply Voltage	V_{LPS}	7.0	Vdc
Input Logic Voltage	U_A/DIR, L_A/PWM, U_B/BRAKE, L_B/I_{DIR}, UC/2Q-4Q, L_C/BRAKE PWM, INPUT SEL, $I_{CONTROL}$, UMC, DISABLE/ENABLE	V_{LPS} + 0.3	Vdc
Continuous Output Current	I_O	75	A
Peak Output Current (10 ms)	I_{PEAK}	150	A
Storage Temperature Range	Tcs	-65 to +150	°C
Case Operating Temperature	Tc	-55 to +125	°C
Junction Temperature	Tj	+150	°C
Ground Isolation Voltage	V_{ISO}	1000	Vdc

TABLE 2. PW-82351 SPECIFICATIONS
(TC = +25°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT STAGE						
Output Switch Transistors (each)						
Continuous Current Drive	Io	+25°C Case	75			A
		+85°C Case	50			A
Peak Current	I_{PEAK}	+85°C Case, 15 ms	120			A
Short Circuit Trip Current[1]	I_{SC}	≤10µs		250		A
Short Circuit Timeout/Reset[1]	I_{SCTO}	Io		16	25	ms
Output Voltage Drop (IGBT)	$V_{CE\ (SAT)}$	Io = 50A		2	2.7	Vdc
Instant Forward Voltage (flyback diode)	V_F	50A		1.7		Vdc
Reverse Recovery Time (flyback diode)	trr			35		ns
Reverse Leakage Current @ Tc = +25°C	Ir	350 Vdc		100	750	µA
Reverse Leakage Current @ Tc = +125°C	Ir	350 Vdc		14	15	mA
Over Voltage Transistor						
Continuous Current Drive	Io	+25°C Case			35	A
		+85°C Case			30	A
Peak Current	I_{PEAK}	+85°C Case, 15 ms			60	A
Output Voltage Drop (IGBT)	$V_{CE\ (SAT)}$			2	3	Vdc
Reverse Leakage Current @ Tc = +25°C	Ir	400 Vdc		50	200	µA
Reverse Leakage Current @ Tc = +125°C	Ir	400 Vdc		0.5	2	mA
Over Voltage Flyback Diode						
Reverse Leakage Current @ Tc = +25°C	Ir	400 Vdc		20	50	µA
Reverse Leakage Current @ Tc = +125°C	Ir	400 Vdc		1	7	mA
Over Voltage Trip	OV ADJ	No external adjustments	400			Vdc
Drive Supply Voltage (motor)[1]	Vcc		0	270	350	Vdc
PHASE AND COMPOSITE CURRENT OUTPUTS						
Phase A and Phase C Output Currents						
Gain Error		+25°C	-5	0.5	5	%
	$I_{A\ OUT}$, $I_{C\ OUT}$	-55°C to +105°C	-7	0.5	7	%
Linearity Error		+25°C	-0.2	0.15	0.2	%
		-55°C to +105°C	-0.4	0.2	0.4	%
Offset		+25°C	-0.625	0.125	0.625	A
		-55°C to +105°C	-1.5	0.4	1.5	A
Phase B Output / Composite Currents						
Gain Error		+25°C	-6	0.7	6	%
	$I_{B\ OUT}$/I_{COMP}	-55°C to +105°C	-8	0.7	8	%
Linearity Error		+25°C	-0.3	0.25	0.3	%
		-55°C to +105°C	-0.8	0.4	0.8	%
Offset		+25°C	-0.8	0.35	0.8	A
		-55°C to +105°C	-2	0.75	2	A
Current Output Transfer Ratio	I_A, I_B, I_C, I_{COMP}			40		mV/A

TABLE 2. PW-82351 SPECIFICATIONS (CONTINUED)
(TC = +25°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
INPUT LOGIC FOR:						
Logic Inputs,	U_A/DIR, L_A/PWM, U_B/BRAKE					
Input Select,	L_B/I_{DIR},U_C/2Q-4Q, L_C/BRAKE PWM					
Input Control,	INPUT SE, $I_{CONTROL}$					
Disable/Enable,	DISABLE/$\overline{\text{ENABLE}}$					
High Level Input Voltage	V_{IH}		2.0			Vdc
Low Level Input Voltage	V_{IL}				0.8	Vdc
Logic Input Currents	I_I				200	µA
Input Rise	tr				40	ns
Input Fall	tf				40	ns
Hall Inputs	H_A, H_B, H_C					
Positive Going Threshold Voltage	V_{T+}		3.0	3.6	4.3	Vdc
Negative Going Threshold Voltage	V_{T-}		0.7	1.4	2.0	Vdc
Hysteresis	V_{T+} - V_{T-}		1.0	2.2	3.6	Vdc
Logic Input Current	I_I				±1.0	µA
Uncommanded Motion Control	$\overline{\text{UMC}}$					
High Level Input Voltage	V_{IH}		2.0			Vdc
Low Level Input Voltage	V_{IL}				0.8	Vdc
Logic Input Currents	I_I				200	µA
Input Rise	tr	see note 2				
POWER SUPPLY						
Positive						
Supply Voltage	V_{PS+}		+14.25	+15	+15.75	Vdc
Supply Current	I_{PS+}				200	mA
Negative						
Supply Voltage	V_{PS-}		-14.25	-15	-15.75	Vdc
Supply Current	I_{PS-}				16	mA
Logic Supply Voltage	V_{LPS}		4.5	5	5.5	Vdc
Logic Supply Current	I_{LPS}				20	mA
FLAG OUTPUT THRESHOLD						
Short Circuit Flag,	$\overline{\text{SC FLAG}}$,					
Over Voltage Flag Out,	OV FLAG OUT,					
Under Voltage Flag,	$\overline{\text{UV FLAG}}$,					
Hall Flag	HALL FLAG					
High Level TTL Output Voltage		I_{OH} = -4 mA	2.4			Vdc
Low Level TTL Output Voltage		I_{OL} = +8 mA			0.45	Vdc
UNDER VOLTAGE FLAG	$\overline{\text{UV FLAG}}$,	Tc = -55°C to+125°C				
Trip Levels						
+5V Supply	VLPS input		3.95	4.15	4.35	Vdc
+15V Supply	VPS+ input		12.0	12.50	13.0	Vdc
OUTPUT SWITCHING CHARACTERISTICS						
Upper Drive:						
Turn-on Propagation Delay	td (on)	150 Ω resistive load		450		ns
Turn-off Propagation Delay	td (off)	(V_{CC}=+270Vdc)		2400		ns
Shut-down Propagation Delay	tsd	see note 3, 4		2250		ns
Turn-on Rise Time	tr			350		ns
Turn-off Fall Time	tf			120		ns
Lower Drive:						ns
Turn-on Propagation Delay	td (on)	150 Ω resistive load		450		ns
Turn-off Propagation Delay	td (off)	(V_{CC}=+270Vdc)		2400		ns
Shut-down Propagation Delay	tsd	see note 3, 4		2250		ns
Turn-on Rise Time	tr			350		ns
Turn-off Fall Time	tf			120		ns

TABLE 2. PW-82351 SPECIFICATIONS (CONTINUED) (TC = +25°C UNLESS OTHERWISE SPECIFIED)						
PARAMETER	**SYMBOL**	**TEST CONDITION**	**MIN**	**TYP**	**MAX**	**UNITS**
SWITCHING FREQUENCY	f		5		25	kHz
THERMAL						
Maximum Thermal Resistance	θjc	Each Output Switch Over Voltage Switch		0.5 0.7	0.55 0.85	°C/W °C/W
Junction Temperature Range Case Operating Temperature Case Storage Temperature	Tj Tc Tcs		-55 -55 -65		+150 +125 +150	°C °C °C
MECHANICAL						
Maximum Lead Soldering Temperature Mounting Torque Weight	Ts		 2		+250 3 14 (399)	°C in-lbs oz (gr)

Notes: 1. V_{CC} to RTN. V_{CC} to RTN must be ≥ 10V for short circuit protection to operate.
2. t_r is ≥ rise time of the +5V power supply. See description of the uncommanded motion control operation.
3. For output switching t_r and t_f are measured from 10% - 90% of output voltage.
4. For output switching t_d on and off and tsd are measured from 50% of the input voltage to 10% of the output voltage.

INTRODUCTION

The PW-82351 is a complete 3-phase motor drive intended for use with brushless dc motors in aerospace applications. The PW-82351 can be used with either analog or digital servo control systems and provides the interface between the power stage and control electronics.

The isolation barrier, which separates the power and control stage, attenuates the ground noise generated from high speed, high power switching. All signals from the control to the power sections are isolated from power and ground of the other section. This eliminates false triggering of the input signals and the need for creative grounding schemes. The isolation barrier also allows the user to operate the output stage from either unipolar or bipolar power supplies without level shifting the input signals.

A built in DC-DC power supply located in the control stage provides power to all electronics in the power stage. This eliminates the need for refresh cycles or external power supplies to power the gate drive circuitry and allows switching duty cycles from 0 - 100%. The PW-82351 has no power supply sequencing requirement.

Motor Current is measured in the output of the PW-82351 and is available as a composite current or individual phase current signal. This current signal can be used as a feedback signal in a servo drive to create a torque loop.

The output power transistors are protected from a short circuit or overvoltage condition applied to the output pins. When a short circuit condition is detected, the output transistor is shut down and a flag is set indicating a short has occurred. The PW-82351 will continue to restart until a short is removed or the user disables the drive. When an overvoltage condition is detected, the overvoltage switch is enabled and a load is applied to the high voltage bus. A status flag is set indicating an overvoltage condition has occurred.

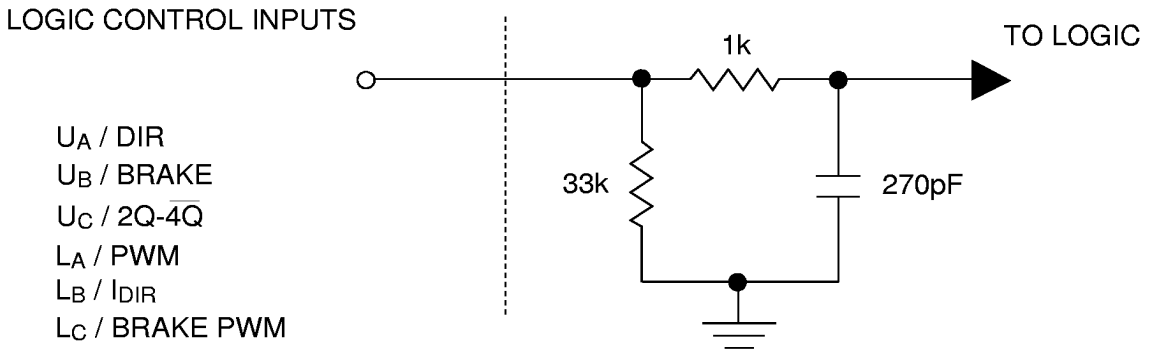


FIGURE 2. INTERNAL INPUT LOGIC NOISE FILTERING

TABLE 3. DESCRIPTION OF DUAL FUNCTION PINS		
MAIN FUNCTION	**ALTERNATE FUNCTION**	**DESCRIPTION**
U_A	DIR	CONTROLS THE SWITCHING OF THE PHASE A (UPPER) TRANSISTOR
		CHANGES THE POLARITY OF THE APPLIED VOLTAGE ACROSS THE MOTOR
L_A	PWM	CONTROLS THE SWITCHING OF THE PHASE A (LOWER) TRANSISTOR
		DUTY CYCLE INPUT
U_B	BRAKE	CONTROLS THE SWITCHING OF THE PHASE B (UPPER) TRANSISTOR
		SELECTS THE BRAKE MODE
L_B	I_{DIR}	CONTROLS THE SWITCHING OF THE PHASE B (LOWER) TRANSISTOR
		INVERTS THE POLARITY OF ICOMP SIGNAL OUTPUT
U_C	2Q-$\overline{4Q}$	CONTROLS THE SWITCHING OF THE PHASE C(UPPER) TRANSISTOR
		2-QUADRANT AND 4-QUADRANT MODULATION
L_C	BRAKE PWM	CONTROLS THE SWITCHING OF THE PHASE C(LOWER) TRANSISTOR
		BRAKE CURRENT CONTROL DUTY CYCLE INPUT

LOGIC CONTROL INPUTS/COMMUTATION LOGIC (UA / DIR, UB / BRAKE, UC / 2Q-$\overline{4Q}$) (LA / PWM, LB / IDIR, LC / BRAKE PWM)

The logic control inputs are dual function inputs that allow the user to select external or internal control for the switching of the output transistors. When INPUT SEL is a logic low (0), the six logic inputs, (U_A, U_B, U_C, L_A, L_B, L_C) control the switching of the output transistors. As shown in TABLE 4, a logic high (1) turns on the output transistor, and a logic low (0) turns the transistor off. The PW-82351 outputs PHASE A_{OUT}, PHASE B_{OUT} and PHASE C_{OUT} are either a H (V_{CC}), L (RTN), or Z (OFF), depending on the logic input. However, when INPUT SEL is a logic high (1), it enables the alternate input functions, DIR, PWM, BRAKE, I_{DIR}, 2Q-$\overline{4Q}$, and BRAKE PWM as shown in TABLE 3. All 6 logic control inputs have built-in noise filtering as shown in FIGURE 2.

START UP LOGIC INITIALIZATION

When powering up the PW-82351, the DISABLE/$\overline{\text{ENABLE}}$ input should be in the disable condition and the Uncommanded Motion Control ($\overline{\text{UMC}}$) input signal should be delayed (see description on $\overline{\text{UMC}}$ operation). This will allow time for the internal circuitry to reach operating voltage before input signals are applied. During power up the internal under voltage circuitry is activated until the +15 V power supplies reaches +12 V. This feature is necessary to prevent damage to the IGBT's when the voltage powering the gate drivers drops below a point that insures normal operation. Once normal operation is obtained (within 1 ms) the PW-82351 can be enabled and all outputs will switch properly.

TABLE 4. PW-82351 INPUT-OUTPUT TRUTH TABLE												
CONTROLS			**INPUTS**						**OUTPUTS**			
$\overline{\text{UMC}}$	**INPUT SEL**	DIS/$\overline{\text{EN}}$	**UPPERS**			**LOWERS**			**PHASE A OUT**	**PHASE B OUT**	**PHASE C OUT**
			UA	**UB**	**UC**	**LA**	**LB**	**LC**			
0	0	0	1	0	0	0	1	0	H	L	Z
0	0	0	1	0	0	0	0	1	H	Z	L
0	0	0	0	1	0	0	0	1	Z	H	L
0	0	0	0	1	0	1	0	0	L	H	Z
0	0	0	0	0	1	1	0	0	L	Z	H
0	0	0	0	0	1	0	1	0	Z	L	H
0	0	0	0	0	1	1	1	0	L	L	H
0	0	0	0	1	0	1	0	1	L	H	L
0	0	0	0	1	1	1	0	0	L	H	H
0	0	0	1	0	0	0	1	1	H	L	L
0	0	0	1	0	1	0	1	0	H	L	H
0	0	0	1	1	0	0	0	1	H	H	L
1	0	X	X	X	X	X	X	X	Z	Z	Z
0	0	1	X	X	X	X	X	X	Z	Z	Z
1	0	1	X	X	X	X	X	X	Z	Z	Z

H = V_{CC}, L = RETURN, X = IRRELEVANT, Z = HIGH IMPEDANCE (OFF)

DIR

A logic '0' or '1' at this input would establish the load voltage as in TABLE 6.

I_{DIR}

A logic '0' at this input will generate an Icomp signal to match TABLE 7 representative current, whereas a logic '1' will generate I_{COMP} signal of opposite polarity.

PWM

An external fixed frequency square wave with varying duty cycle is applied to this input. The signal can vary from 0% to 100% for similar voltage variation at the output.

BRAKE

The BRAKE input controls dynamic braking of the motor. A logic '1' at this pin will select the brake mode. In this mode, the alternate inputs (DIR, I_{DIR}, PWM, 2Q-$\overline{4Q}$) will be ignored and only the Brake PWM input will be used to PWM the lower switches in the 3-phase bridge. The $\overline{\text{UMC}}$ input must be at a logic low (0) when the brake mode is used.

BRAKE PWM

When operating in the brake mode, the BRAKE PWM input is used to control the duty cycle of the lower switches in the 3-phase bridge during braking. This input requires an external fixed frequency square wave with varying duty cycle. It is important to monitor the current returning from the load, and provide an external current limit that sets the PWM BRAKE signal to a logic '0' when currents higher than the PW-82351 ratings are detected. A logic '0' on this input will turn off all the lower switches while a logic '1' will turn on all the lower switches simultaneously.

TWO-QUADRANT OR FOUR-QUADRANT (2Q - $\overline{4Q}$)

A logic '1' on this input will select the Two-Quadrant modulation mode. When operating in the Two-Quadrant mode, the PWM signal is applied to the upper output transistor while the commutation signal is applied to the lower output transistor of the different phase. A logic '0' at the input will select the Four-Quadrant modulation mode. Operation in the Four-Quadrant mode is the same as the Two-Quadrant except that the PWM signal is applied to the upper transistor and a complementary signal is applied to the lower transistor in the same phase, while the commutation signal is applied to the lower transistor of the different phase.

DISABLE / $\overline{\text{ENABLE}}$ (DIS/$\overline{\text{EN}}$)

The DISABLE / $\overline{\text{ENABLE}}$ input will shut down the output stage when in the disable mode, logic high (1). The input is internally pulled high and must be tied to a logic low (0) in order to be enabled. When disabled, switching on the logic inputs will not switch the output transistors, see TABLE 4. When redundant shutdown of the output transistors are required, the disable input and the $\overline{\text{UMC}}$ input can be used.

INPUT SEL

The input select pin (INPUT SEL) controls the dual function logic inputs. As shown in TABLE 5, a logic '1' enables the internal commutation logic for operation in the self commutated mode. A logic '0' enables the six parallel inputs for individual output transistor control. The input select pin is a logic high input.

TABLE 5. DUAL FUNCTION INPUTS		
INPUT SEL	**FUNCTION**	**ACTIVE INPUT PINS**
1	Internal Commutation Logic	DIR, PWM, BRAKE, I_{DIR}, 2Q-$\overline{4Q}$, BRAKE PWM,
0	Six Parallel Inputs	U_A, L_A, U_B, L_B, U_C, L_C

UNDER VOLTAGE FLAG ($\overline{\text{UV FLAG}}$)

There are two conditions which will cause the $\overline{\text{UV FLAG}}$ to be set. The $\overline{\text{UV FLAG}}$ output will go low (logic 0) when the +5V and/or the +15V power supply inputs to the PW-82351 drop below the internally set low supply levels. The nominal undervoltage levels are +4.35V for the +5V supply and +13V for the +15V supply. The -15V supply has no effect on the $\overline{\text{UV FLAG}}$ signal. The $\overline{\text{UV FLAG}}$ will also go low when the $\overline{\text{UMC}}$ input is a logic 1 (disabled).

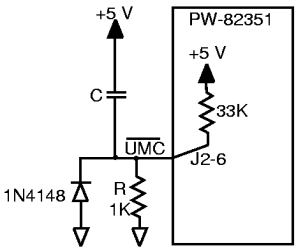


FIG 3A. $\overline{\text{UMC}}$ TIED LOW

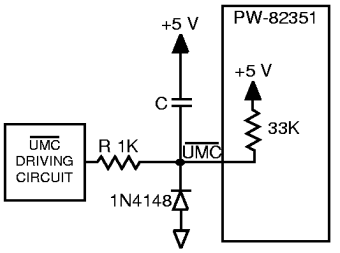


FIG 3B. $\overline{\text{UMC}}$ CONTROLLED BY EXTERNAL CIRCUIT

FIGURE 3. $\overline{\text{UMC}}$ DELAY CIRCUIT

TABLE 6. PW-82351P6
COMMUTATION TRUTH TABLE (USING INTERNAL COMMUTATION LOGIC)

CONTROLS			INPUTS				HALLS			OUTPUTS		
$\overline{\text{UMC}}$	INPUT SEL	DISABLE / $\overline{\text{ENABLE}}$	DIR	BRAKE	ICONTROL	BRAKE PWM	H_A	H_B	H_C	PHASE A OUT	PHASE B OUT	PHASE C OUT
0	1	0	1	0	0	X	0	1	1	L	Z	H
0	1	0	1	0	0	X	0	1	0	L	H	Z
0	1	0	1	0	0	X	1	1	0	Z	H	L
0	1	0	1	0	0	X	1	0	0	H	Z	L
0	1	0	1	0	0	X	1	0	1	H	L	Z
0	1	0	1	0	0	X	0	0	1	Z	L	H
0	1	0	0	0	0	X	1	1	0	Z	L	H
0	1	0	0	0	0	X	0	1	0	H	L	Z
0	1	0	0	0	0	X	0	1	1	H	Z	L
0	1	0	0	0	0	X	0	0	1	Z	H	L
0	1	0	0	0	0	X	1	0	1	L	H	Z
0	1	0	0	0	0	X	1	0	0	L	Z	H
0	1	0	X	1	0	1	X	X	X	L	L	L
0	1	0	X	1	1	0	X	X	X	Z	Z	Z

TABLE 7. PW-82351 CURRENT DE-COMMUTATION TRUTH TABLE					
INPUTS				PHASE CURRENT OUTPUTS I_{COMP} / I_B	
CONTROL	HALLS			DERIVED CURRENT	REPRESENTATIVE CURRENT
$I_{CONTROL}$	H_A	H_B	H_C		
1	X	X	X	$-I_A - I_C$	I_B
0	1	0	0	$-I_C$	I_A
0	1	1	0	$-I_C$	$-I_C$
0	0	1	0	$-I_A$	I_B
0	0	1	1	$-I_A$	$-I_A$
0	0	0	1	I_C	I_C
0	1	0	1	I_A	$-I_B$
0	0	0	0	$-I_A - I_C$	I_B
0	1	1	1	$-I_A - I_C$	I_B

UNCOMMANDED MOTION CONTROL ($\overline{UMC}$)

The $\overline{UMC}$ (Uncommanded Motion Control) input operates the internal DC-DC power supply. This power supply provides all the operating power for the high voltage side (power stage) of the isolation barrier. When the $\overline{UMC}$ input is a logic low (0), the DC-DC power supply is enabled and power is supplied to the power stage. When tied to a logic high (1), the DC-DC power supply and the input logic is disabled. The power supply for the power stage electronics is turned off even when the high voltage is present on the V_{CC} terminals. The $\overline{UMC}$ input is completely independent of the V_{CC} and no output switching can occur when the input is disabled, see TABLE 4.

The $\overline{UMC}$ input works in conjunction with the internal undervoltage detection circuitry. To insure that all internal circuitry is properly reset during power up or power reset of the +5V and/or +15V supplies, the $\overline{UMC}$ signal must be delayed even if this input is not actively used (tied low). The amount of delay is related to the rise time of the +5V power supply at J2-10, VLPS. The rise time should take into account all local decoupling. The $\overline{UMC}$ signal delay can be accomplished as shown in FIGURE 3 (3a and 3b) or with external logic. Whatever method of delay is used, the RC time constant (RC = 1000C) should be ≥ the time it takes for the +5V supply to reach 4.5V. The value of R should be set at 1kΩ and the capacitor varied to adjust the time constant.

MOTOR CURRENT SENSING OUTPUTS (I_{SENSE})

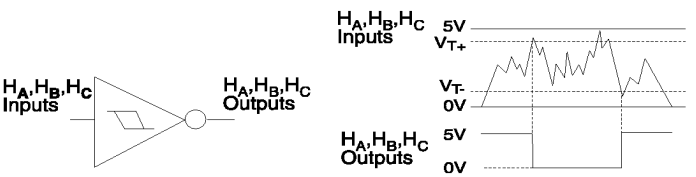
The motor current is sensed by two internal resistors located in the Phase A and Phase C outputs. The voltage developed across the resistor is conditioned, scaled and transmitted across the isolation barrier to the current mode selector. The current mode selector, process the current signals into individual phase currents or a composite current signal.

INDIVIDUAL PHASE CURRENT MODE ($I_{A\ OUT}$, $I_{B\ OUT}$, $I_{C\ OUT}$)

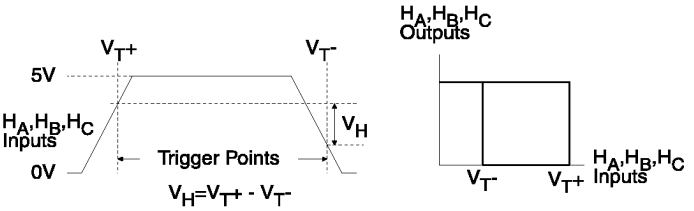
When individual phase current is required, the current mode selector processes the phase A and phase C currents to derive the phase B current. These currents are converted into a voltage and presented as individual phase currents I_{AOUT}, I_{BOUT}, and I_{COUT}. The sign of the voltage indicates the direction of the motor current. A positive voltage indicates current into the motor and a negative voltage indicates current from the motor. When individual phase current mode is used, the $I_{CONTROL}$ input must be tied high (logic 1), see TABLE 7.

COMPOSITE PHASE CURRENT MODE (I_{COMP})

When a single output signal current is desired, the composite phase current output (I_{COMP}) should be used. The composite current is derived from the Phase A and Phase C currents, internally processed, and presented as a single bipolar voltage. The sign of the composite voltage indicates motor torque. A positive voltage indicates clockwise (CW) rotation and a negative voltage indicates counter clockwise (CCW) rotation. When composite phase current mode is used, the $I_{CONTROL}$ must be tied low (logic 0).



TYPICAL SCHMITT RESPONSE TO NOISE INPUT



HA,HB,HC ARE INTERNAL PW-82351 RESPONSES

FIGURE 4. HYSTERESIS DEFINITION AND CHARACTERISTICS

HALL SENSOR INPUTS (H_A, H_B, H_C)

The H_A, H_B, H_C inputs are connected to the Hall effect sensors from the motor. A, B, C, correspond to the hall phasing. These inputs are Schmitt triggered with hysteresis for noise immunity as shown in FIGURE 4.

The hall sensors are used to translate the motor current sense signals to the proper phase for the I_A, I_C, and I_{COMP} outputs, see TABLE 7.

HALL FLAG

The Hall Flag in normal operation will drop low (logic 0). The Hall Flag will set high (logic 1) when it detects the Hall sensor inputs, H_A, H_B and H_C to be either all highs or all lows.

V_{CC}, RTN

The V_{CC} and RTN (return) should be connected to the high current system power supply. These pins are directly connected to the output transistors and supply the power to the motor. A capacitor should be placed between V_{CC} and RTN as a reservoir for instantaneous high current switching (See DDC's Application Note AN/H-6, *PW-82351 Motor Drive Power Supply*). This capacitance should be located directly adjacent to the motor drive to minimize the interconnect effects from line inductance and resistance.

V_{LPS}, V_{PS+}, V_{PS-}, DIG GND, ANA GND, POWER GND

The V_{LPS} is the logic power supply input for the control section. This point is connected to the +5 volt power supply. The V_{LPS} should have external decoupling.

The V_{PS+} and V_{PS-} are the analog power supply inputs for the control section. These inputs are connected to the ±15 volt power supplies. Power for the internal DC-DC power supply is also derived from the V_{PS+} input. The V_{PS+} and V_{PS-} should have external decoupling.

The ANA GND and DIG GND connection is a single point power supply return for the V_{LPS}, V_{PS+}, and V_{PS-}. POWER GND is the return for internal DC-DC power supply. These ground points must be tied together externally.

The PW-82351 will be fully functional within 1 ms after all power supply voltages are applied.

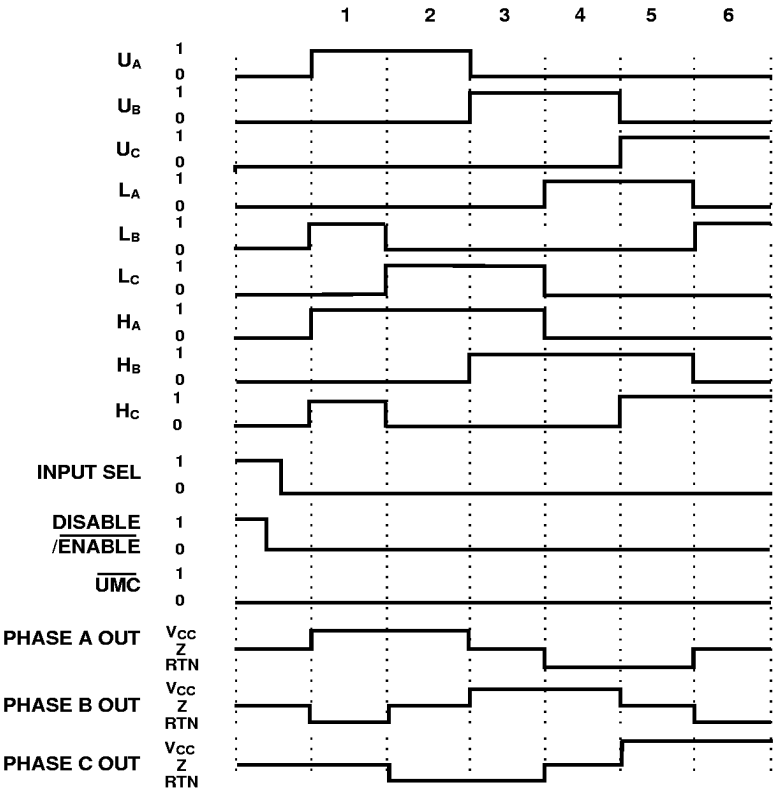


FIGURE 5. PW-82351 INPUT TIMING DIAGRAM

POWER ON SEQUENCE

When power is applied, the motor drive starts a power on sequence prior to accepting any control signals on the logic inputs U_A, L_A, U_B, L_B, U_C, L_C or the internal commutation logic.

The cycle lasts for 1 ms and is activated by the low state of the UV FLAG. When a low state is detected the following occurs:

1. Internal gate drive signals are set to a low state.
2. All user supplied signals to the logic inputs are ignored.

During the power sequencing procedure the internal logic shall:

1. Cycle each gate drive one at a time from a logic low to a logic high and will keep repeating this sequence.
2. All user supplied signals to the logic inputs are ignored.
3. Set the SC FLAG to a high state and ignore any desatu ration condition.

After 1 ms the logic will:

1. Set all gate drive inputs to a logic low.
2. Enable the logic inputs and set the gate drive accordingly.
3. Resume normal operation.

PHASE A_{OUT}, B_{OUT}, C_{OUT}

The motor is connected between the three output terminals Phase Aout, Phase Bout, and Phase Cout. These outputs switch between Vcc and RTN. FIGURE 8 shows the output current capability.

SHORT CIRCUIT OPERATION

The PW-82351 outputs are completely short-circuit-protected from either a hard or soft short to the V_{CC} or RTN lines. Each output transistor is individually short-circuit-protected by circuitry that detects the desaturation voltage for that transistor when a short is occurring. Once a short circuit condition is detected, all the output transistors are shutdown and the drive is disabled for 16 ms to allow the transistor time to cool down. After the 16 ms period the drive is enabled and power is re-applied to the output pins to see if the short has cleared. If the short is still present, the shutdown process is repeated. The PW-82351 will continue operating in this mode (detect a short, disable for 16 ms, enable) until the short is cleared or the drive is permanently disabled by the system through the DISABLE / $\overline{\text{ENABLE}}$ control input.

SHORT-CIRCUIT FLAG ($\overline{\text{SC FLAG}}$)

The $\overline{\text{SC FLAG}}$ output will drop to a logic low when a short has been detected. The $\overline{\text{SC FLAG}}$ output will be latched low until the internal short circuit detection circuitry has timed out for 16 ms. The $\overline{\text{SC FLAG}}$ will then be reset high. If the short is still present the flag will be set low again and the cycle will be repeated. By counting the number of times the $\overline{\text{SC FLAG}}$ drops low, the user can determine how many restart cycles are appropriate before permanently disabling the drive.

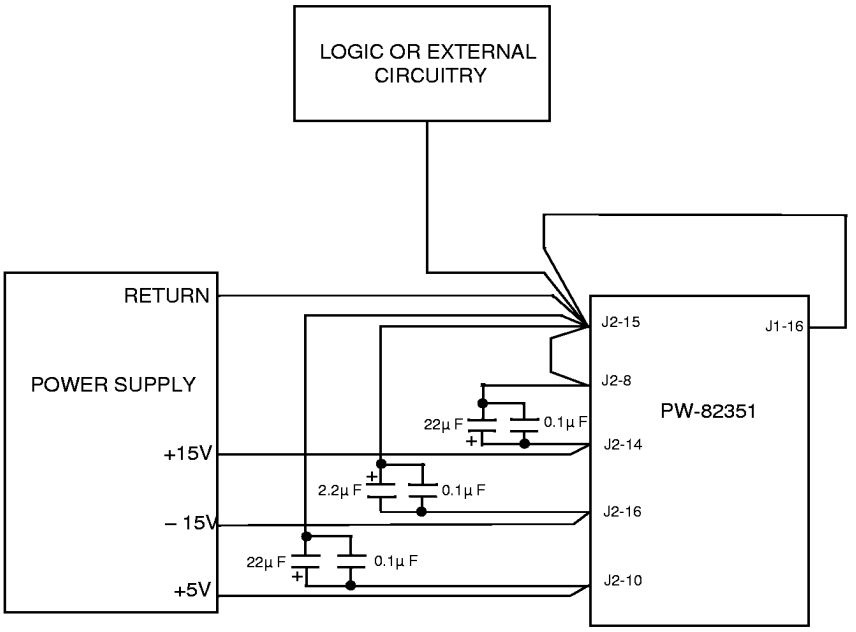


FIGURE 6. ROUTING FOR POWER SUPPLY / INTERCONNECT GROUND POINTS

OVER VOLTAGE LOW, OV ADJ, OV FLAG OUT

The over voltage (OV) feature monitors the V_{CC} supply voltage to RTN to detect a bus pump-up condition and prevent it from damaging the drive. When an over voltage condition (Vmax) is detected, the OV switch is turned on allowing current to bleed off the supply and the OV flag OUT is set high (logic 1).

An external bleed resistor is placed between V_{CC} and the OVER VOLTAGE LOW terminal. The OV switch will turn off and the OV FLAG OUT will return low (logic 0) once the V_{CC} voltage is below the Vmin trip point.

The PW-82351 is set internally for a trip voltage of 400 V. To set a different trip voltage an external resistor is connected from the OV ADJ terminal to either RTN or V_{CC} (see FIGURES 9a and 9b). This resistor should be selected for the voltage Vmax you want the OV switch to turn on.

ISOLATION BARRIER

The isolation barrier maintains electrical isolation between the control side ground and power side return. All signals are isolated and the power section is completely floating from the control section.

HEATSINK MOUNTING

The PW-82351 must be mounted on a heatsink to remove the power dissipated inside the unit when driving the load. The PW-82351 should have a thermally conductive interface, like a thermal joint compound between the heatsink and motor drive module. The base plate of the PW-82351 is not electrically connected to the internal circuitry and does not require an isolated thermal interface. The PW-82351 should be mounted with #6 self-locking screws and torqued to specifications in TABLE 2.

ASSEMBLY CLEANING INSTRUCTIONS

The PW-82351 is encapsulated with silicones and organic coatings which cannot be exposed to solvents for extended periods of time. Exposure to solvent vapors during vapor degreasing should be limited to the minimum process times required for flux residue removal. The maximum exposure to solvent vapors should be limited to 10 minutes. The PW-82351 cannot be submerged in solvent fluids. If cleaning of assembled modules in a fluid is anticipated, DDC must be contacted before any modules are exposed to the fluid in order to mantain the product warranty.

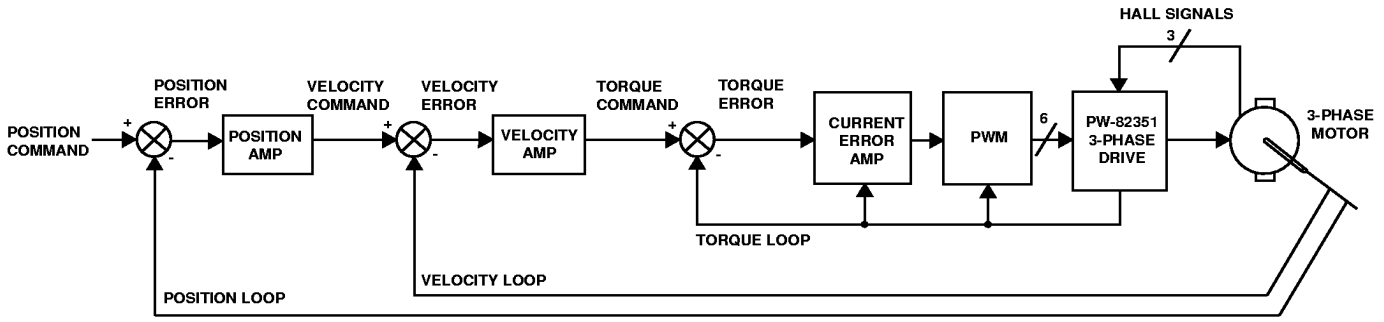


FIGURE 7. TYPICAL POSITION AND VELOCITY CONTROL LOOP

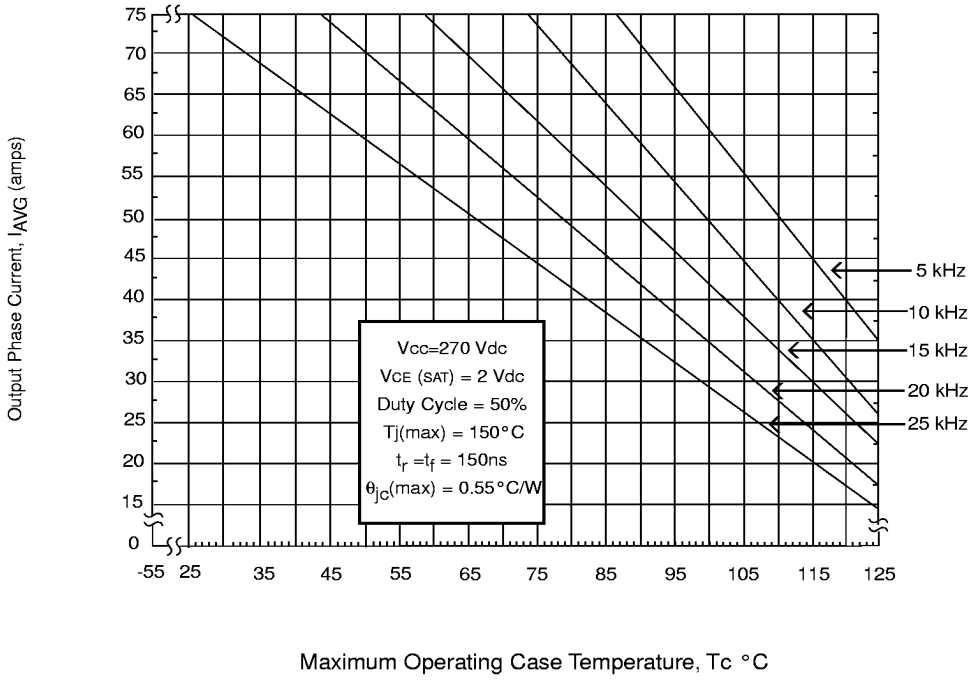
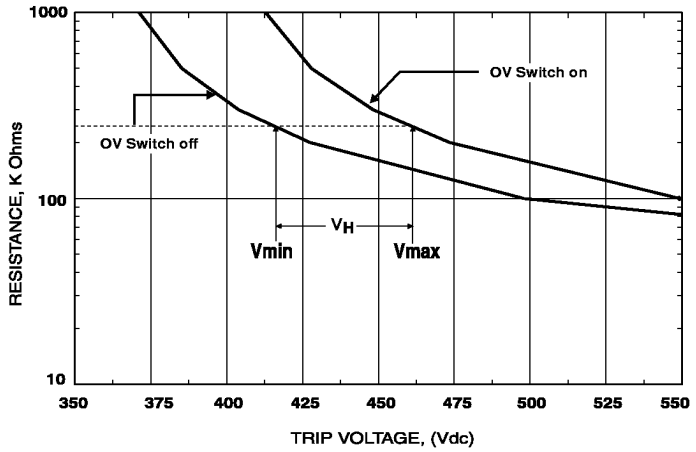
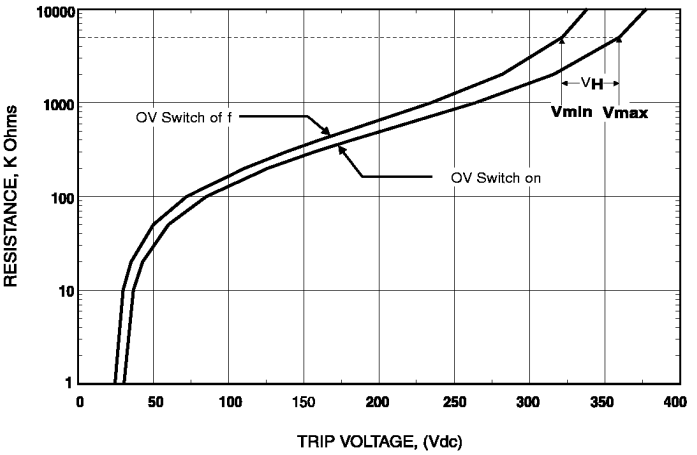


FIGURE 8. PW-82351 OUTPUT PHASE CURRENT VS. MAXIMUM OPERATING CASE TEMPERATURE



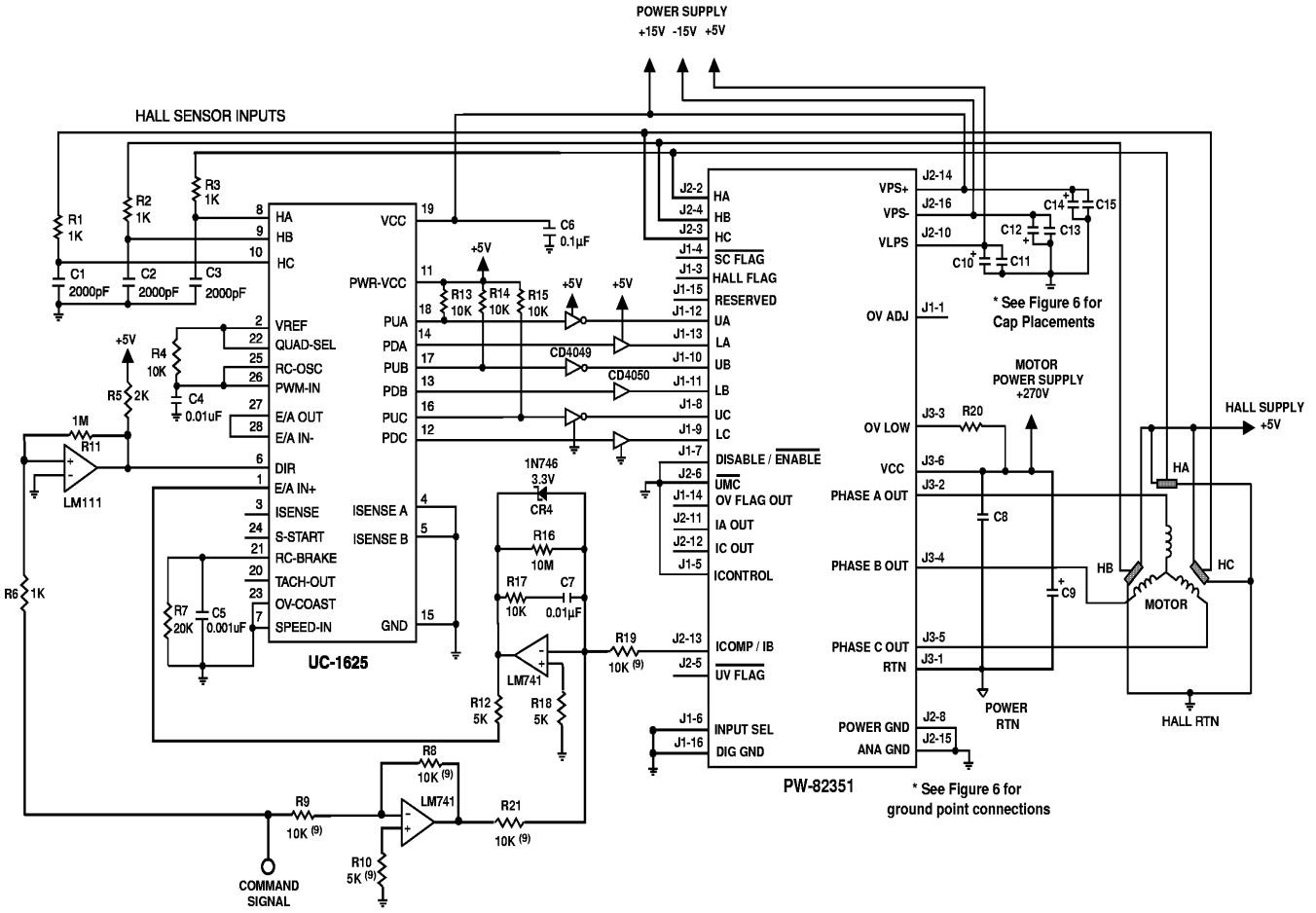
NOTE: V_H = HYSTERESIS VOLTAGE

FIGURE 9a. PW-82351 TYPICAL OVER VOLTAGE TRIP Vs. OV ADJUST SETTING WITH EXTERNAL RESISTOR CONNECTED TO RTN



NOTE: V_H = HYSTERESIS VOLTAGE

FIGURE 9b. PW-82351 TYPICAL OVER VOLTAGE TRIP Vs. OV ADJUST SETTING WITH EXTERNAL RESISTOR CONNECTED TO V_{CC}



NOTES:
1. C8 is a ceramic capacitor and should be selected per DDC Application Note AN/H-6, *PW-82351 Motor Drive Power Supply*, equation 1.
2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/H-6, *PW-82351 Motor Drive Power Supply*, equation 1.
3. C10, C12, C14 are electrolytic capacitors where C10 is 22 µF, 15 V; C12 is 2.2 µF, 50 V; and C14 is 22 µF, 50 V.
4. C11, C13, C15 are 0.1 µF, 50 V ceramic capacitors.
5. Resistance and power of R20 is application specific.
6. All resistors have a tolerance of ±10%, unless otherwise specified.
7. The CD4050 converts the +15V logic output of the UC-1625 to +5V logic signals.
8. The CD4049 (or equivalent) inverts the upper signal from the UC-1625.
9. 1% or better, depending on required accuracy.

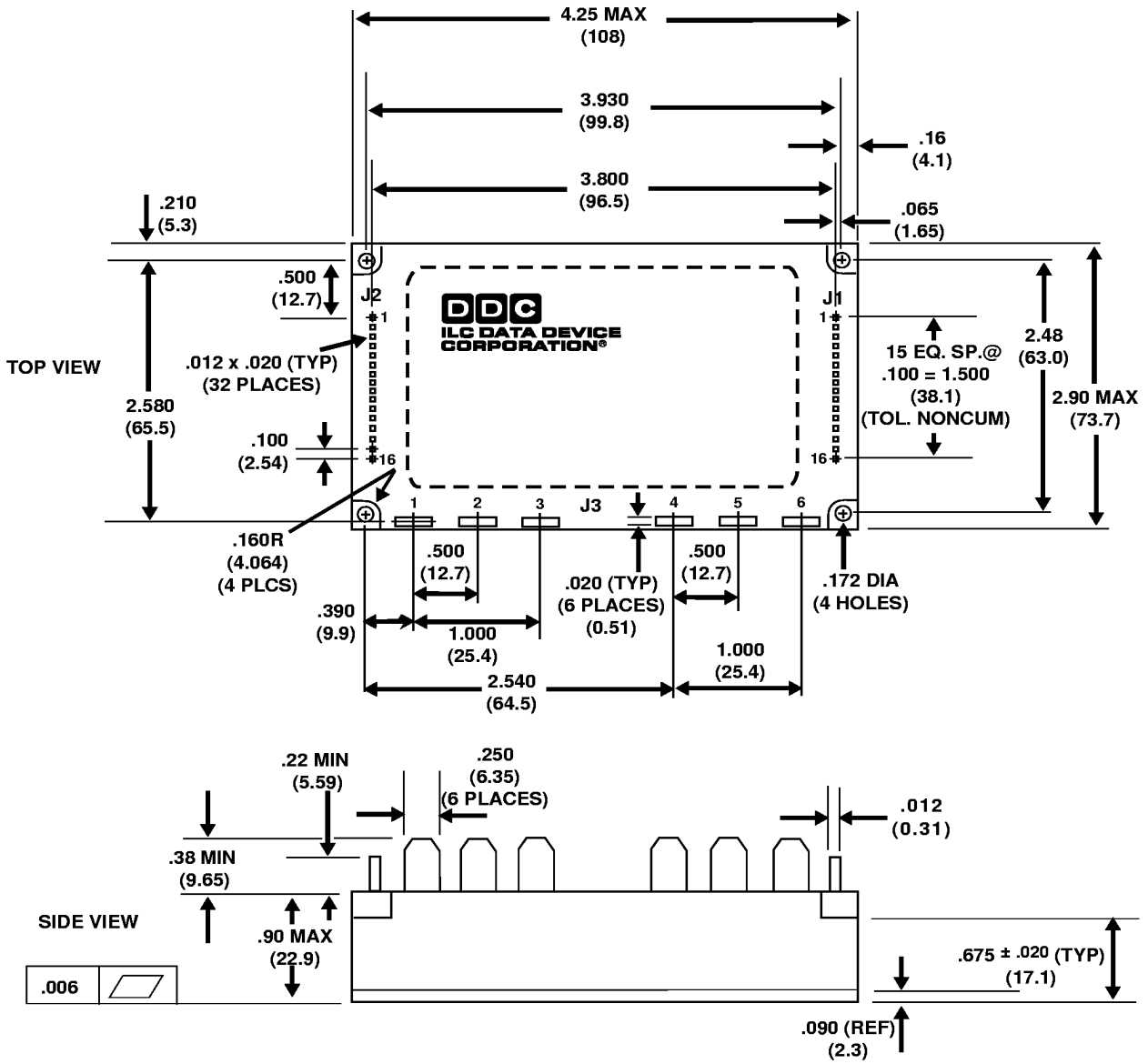
FIGURE 10. PW-82351P6 TORQUE HOOK-UP USING UC-1625 MOTOR CONTROLLER

TABLE 8. PW-82351 PIN ASSIGNMENT AND FUNCTION DESCRIPTION

J1 PIN	J1 PIN FUNCTION	J1 DESCRIPTION
J1-1	OV ADJ	An external resistor connected to this input from OV ADJ V_{CC} or OV ADJ RTN sets the over voltage trip level.
2	N/C	
3	HALL FLAG	A logic high indicates an illegal input on H_A, H_B, H_C.
4	$\overline{\text{SC FLAG}}$	A logic low output indicates that a short has occurred.
5	$I_{CONTROL}$	An active high logic input that is tied low for composite phase current mode or tied high for individual phase current mode.
6	INPUT SEL	Controls the operation of the dual function input pins U_A /DIR, L_A /PWM, U_B / BRAKE, L_B /I_{DIR}, U_C/2Q-4Q, L_C / BRAKE PWM. A logic low enables the input control logic to operate each of the output switches independently U_A, L_A, U_B, L_B, U_C, L_C. A logic high enables the self-commutated mode.
7	DISABLE / $\overline{\text{ENABLE}}$	This is an active high input and must be tied low to activate the input control logic.
8	U_C / 2Q-$\overline{4Q}$	Dual function pin controlled by INPUT SEL. A logic '0' on Input Sel enables U_C and a logic '1' on Input Sel activates 2Q-$\overline{4Q}$
9	L_C / BRAKE PWM	Dual function pin controlled by INPUT SEL. A logic '0' on Input Sel enables L_C and a logic '1' on Input Sel activates Brake PWM.
10	U_B / BRAKE	Dual function pin controlled by INPUT SEL. A logic '0' on Input Sel enables U_B and a logic '1' on Input Sel activates Brake.
11	L_B / I_{DIR}	Dual function pin controlled by INPUT SEL. A logic '0' on Input Sel activates L_C and a logic '1' on Input Sel activates I_{DIR} pin.
12	U_A / DIR	Dual function pin controlled by INPUT SEL. A logic '0' on Input Sel activates U_A and a logic '1' on Input Sel activates DIR.
13	L_A / PWM	Dual function pin controlled by INPUT SEL. A logic '0' on Input Sel activates L_A and a logic '1' on Input Sel activates PWM.
14	OV FLAG OUT	A logic high output indicates that over voltage condition has occurred.
15	N/C	
16	DIG GND	Return for logic power supply. (see FIGURE 6, page 9)

J2 PIN	J2 FUNCTION	J2 DESCRIPTION
J2-1	N/C	
2	H_A	This input is connected to the motor shaft HALL sensors and is set for 120° commutation.
3	H_C	This input is connected to the motor shaft HALL sensors and is set for 120° commutation
4	H_B	This input is connected to the motor shaft HALL sensors and is set for 120° commutation.
5	$\overline{\text{UV FLAG}}$	This output goes low when an under voltage condition occurs on the +15 V or +5 V power supplies or when UMC is disabled.
6	$\overline{\text{UMC}}$	A logic low or high on this pin enables or disables the internal DC-DC power supply respectively.
7	N/C	
8	POWER GND	This is the return for the internal DC-DC power supply. (see FIGURE 6, page 9)
9	N/C	
10	+5V	A +5 V logic supply voltage for the control section. (see FIGURE 6, page 9)
11	$I_{A\ OUT}$	Phase A current obtained from motor current sensing output (I_{SENSE}) in Phase A.
12	$I_{C\ OUT}$	Phase C current obtained from motor current sensing output (I_{SENSE}) in Phase C.
13	I_{COMP} / I_{OUTB}	Dual function pin. Composite current (derived from Phase A & Phase C currents processed internally) or Phase B current.
14	+15V	Positive power supply input for +15 V power. (see FIGURE 6, page 9)
15	ANA GND	Return for ±15 V power. (see FIGURE 6, page 9)
16	–15V	Negative power supply input for -15 V power. (see FIGURE 6, page 9)

J3 PIN	J3 FUNCTION	J3 DESCRIPTION
J3-1	RTN	Supply power return for output stage.
2	PHASE A_{OUT}	Phase A output.
3	OVER VOLTAGE LOW	An external resistor is connected between this pin and VCC to allow flyback current to bleed off the supply.
4	PHASE B_{OUT}	Phase B output.
5	PHASE C_{OUT}	Phase C output.
6	V_{CC}	Supply power for output stage.



NOTES:
1. Dimensions are in inches (millimeter).
2. Tolerances are ±.01 (.25) for XX decimal places, and ±.005 (.130) for XXX decimal places.
3. J1, J2 pins are 0.012 x 0.020 (0.31 x 0.51).
4. J3 pins are 0.25 x 0.02 (6.35 x 0.51).

FIGURE 11. PW-82351 MODULE