NEC

MOS INTEGRATED CIRCUIT

μPD78F4225Y

16/8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78F4225Y is a product in the μPD784225Y subseries in the 78K/IV series.

The μPD78F4225Y has a flash memory in the place of the internal ROM of the μPD784225Y. Data can be written to or erased from the flash memory of the μPD78F4225F with the microcontroller mounted on a printed wiring board.

The μPD78F4225Y is based on the μPD78F4225 with an I^2C bus control function appended, and is ideal for applications in audio visual.

The functions are explained in detail in the following user's manuals. Be sure to read this manual when designing your system.

μPD784225, 784225Y Subseries User's Manual - Hardware : Planned
78K/IV Series User's Manual - Instruction : U10905E

FEATURES

- I^2C bus serial interface supporting multi task
- Pin-compatible with mask ROM model (except V_{PP} pin)
- Flash memory: 128K bytes
- Internal RAM : 4352 bytes
- Same operating voltage as mask ROM model: V_{DD} = 1.8 to 5.5 V

ORDERING INFORMATION

Part Number	Package
μPD78F4225YGC-8BT	80-pin plastic QFP (14 × 14 mm)
μPD78F4225YGK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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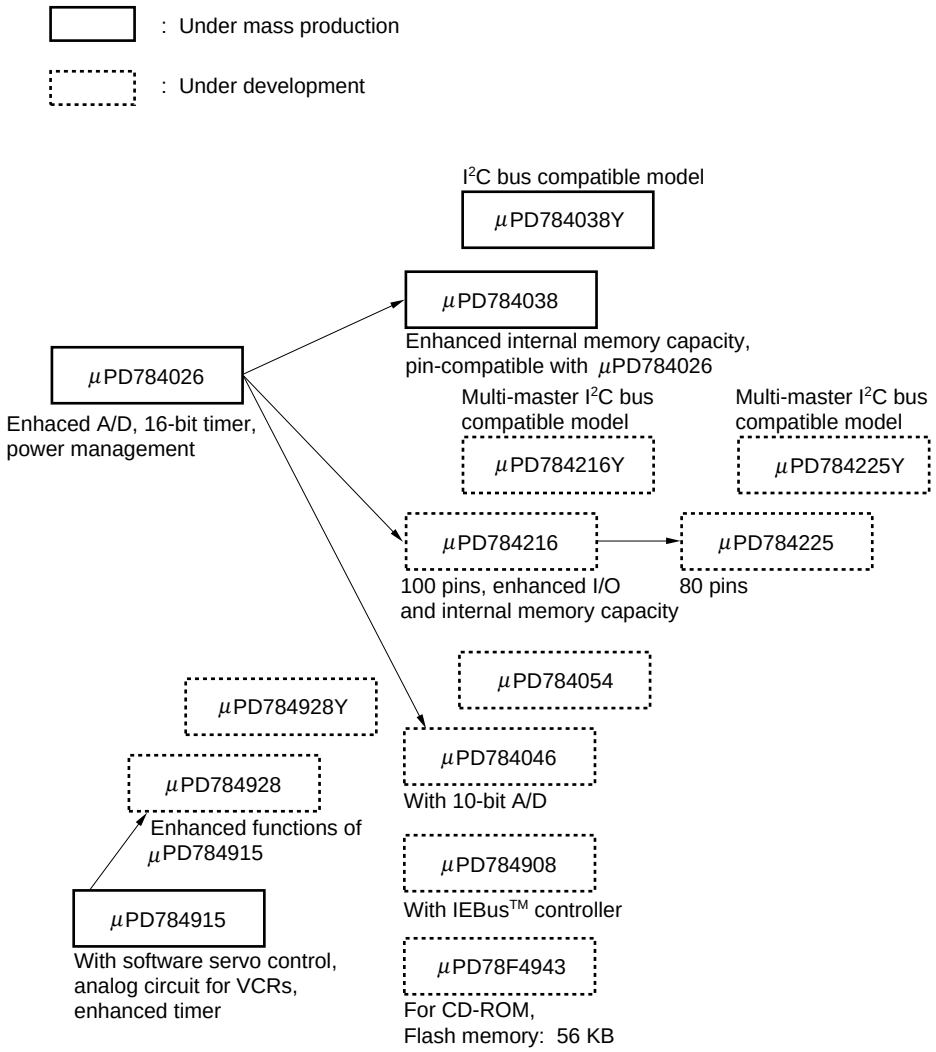
78K/IV Series Product Development



FUNCTIONS

Item		Function
Number of basic instructions (mnemonics)		113
General-purpose register		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)
Minimum instruction execution time		• 160 ns/320 ns/640 ns/1280 ns/2560 ns (main system clock: f_{XX} = 12.5 MHz) • 61 μs (subsystem clock: f_{XX} = 32.768 KHz)
Internal memory	Flash memory	128 KBytes
	RAM	4352 Bytes
Memory space		1 MB with program and data spaces combined
I/O port	Total	67
	CMOS Input	8
	CMOS I/O	59
Pins with ancillary functions[Note]	Pins with pull-up resistor	57
	LEDs direct drive output	16
Real-time output port		4 bits × 2, or 8 bits × 1
Timer/counter		16-bit timer/counter : timer register × 1, Capture/compare register × 2 — Pulse output: • PWM/PPG output • Square wave output • One-shot pulse output
		8-bit timer/counter 1 : timer register × 1, Compare register × 1 — Pulse output: • PWM output • Square wave output
		8-bit timer/counter 2 : timer register × 1, Compare register × 1 — Pulse output: • PWM output • Square wave output
		8-bit timer/counter 5 : timer register × 1, Compare register × 1
		8-bit timer/counter 6 : timer register × 1, Compare register × 1
Serial interface		UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) CSI (3-wire serial I/O, I^2C bus supporting multi master): 1 channel
A/D converter		8-bit resolution × 8 channels
D/A converter		8-bit resolution × 2 channels
Clock output		Selectable from f_{XX}, $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT}
Buzzer output		Selectable from $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$
Watch timer		1 channel
Watchdog timer		1 channel
Standby		• HALT/STOP/IDLE mode • In power-saving mode (with subsystem clock): HALT/IDLE mode
Interrupt	Hardware	25 (internal: 18, external: 7)
	Software	BRK instruction, BRKCS instruction, operand error
	Non-maskable	Internal: 1, external: 1
	Maskable	Internal: 17, external: 6
		• 4 programmable priority levels • 3 service modes: vectored interrupt/macro service/context switching
Supply voltage		V_{DD} = 1.8 to 5.5 V
Package		• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Note The pins with ancillary functions are included in the I/O pins.

CONTENTS

1. DIFFERENCES AMONG MODELS IN μPD784225Y SUBSERIES

The only difference among the μPD784224Y and 784225Y lies in the internal memory capacity.

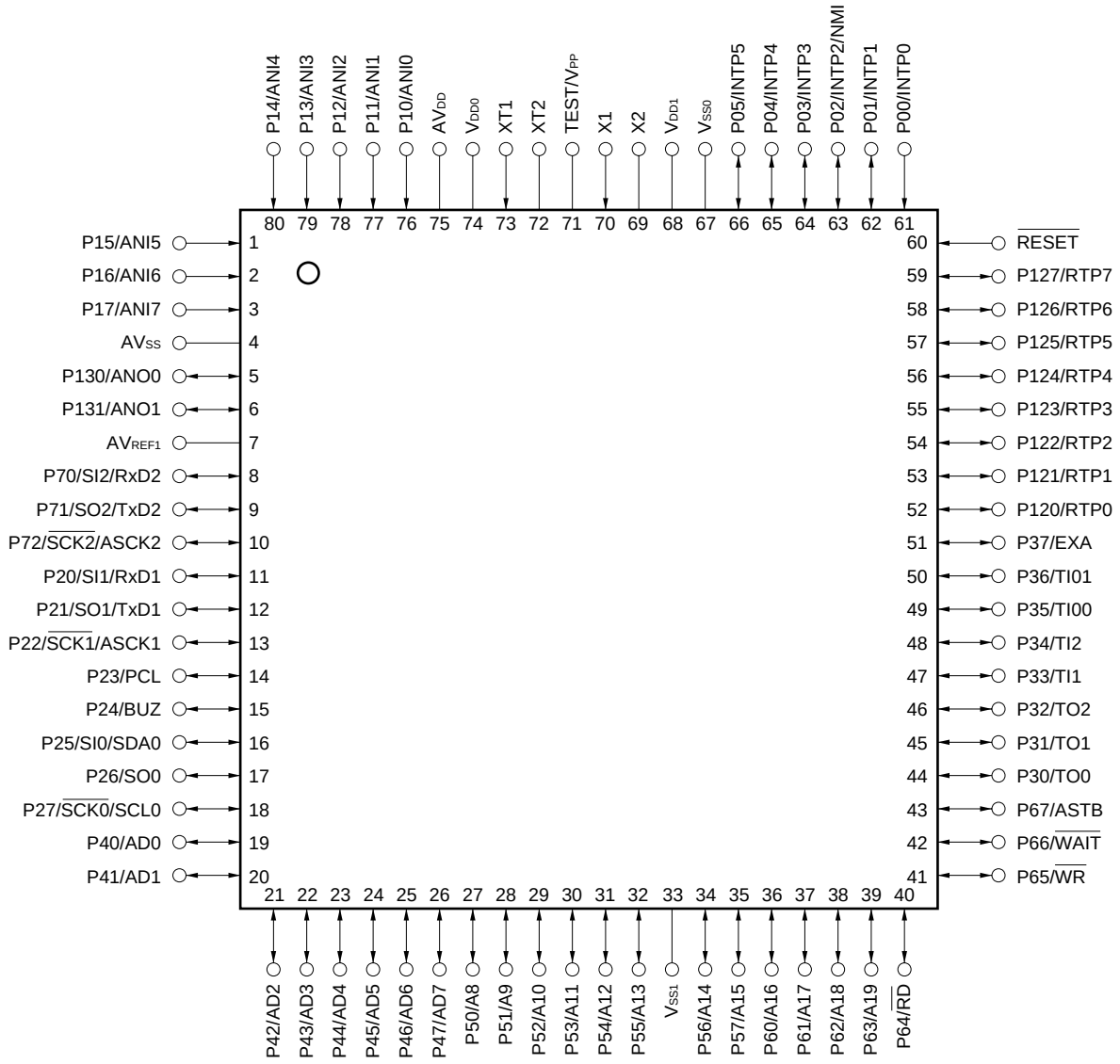
The μPD78P4225Y is provided with a 128-KB flash memory instead of the mask ROM of the above models. These differences are summarized in Table 1-1.

Table 1-1. Differences among Models in μPD784225Y Subseries

Item \ Part Number	μPD784224Y	μPD784225Y	μPD78F4225Y
Internal ROM	96 KBytes (mask ROM)	128 KBytes (mask ROM)	128 KBytes (flash memory)
Internal RAM	3584 Bytes	4352 Bytes	
Internal memory size switching register (IMS)	None		Provided
V_{PP} pin	None		Provided

2. PIN CONFIGURATION (Top View)

- **80-pin plastic QFP (14 × 14 mm)**
  μPD78F4225YGC-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm)**
  μPD78F4225YGK-BE9



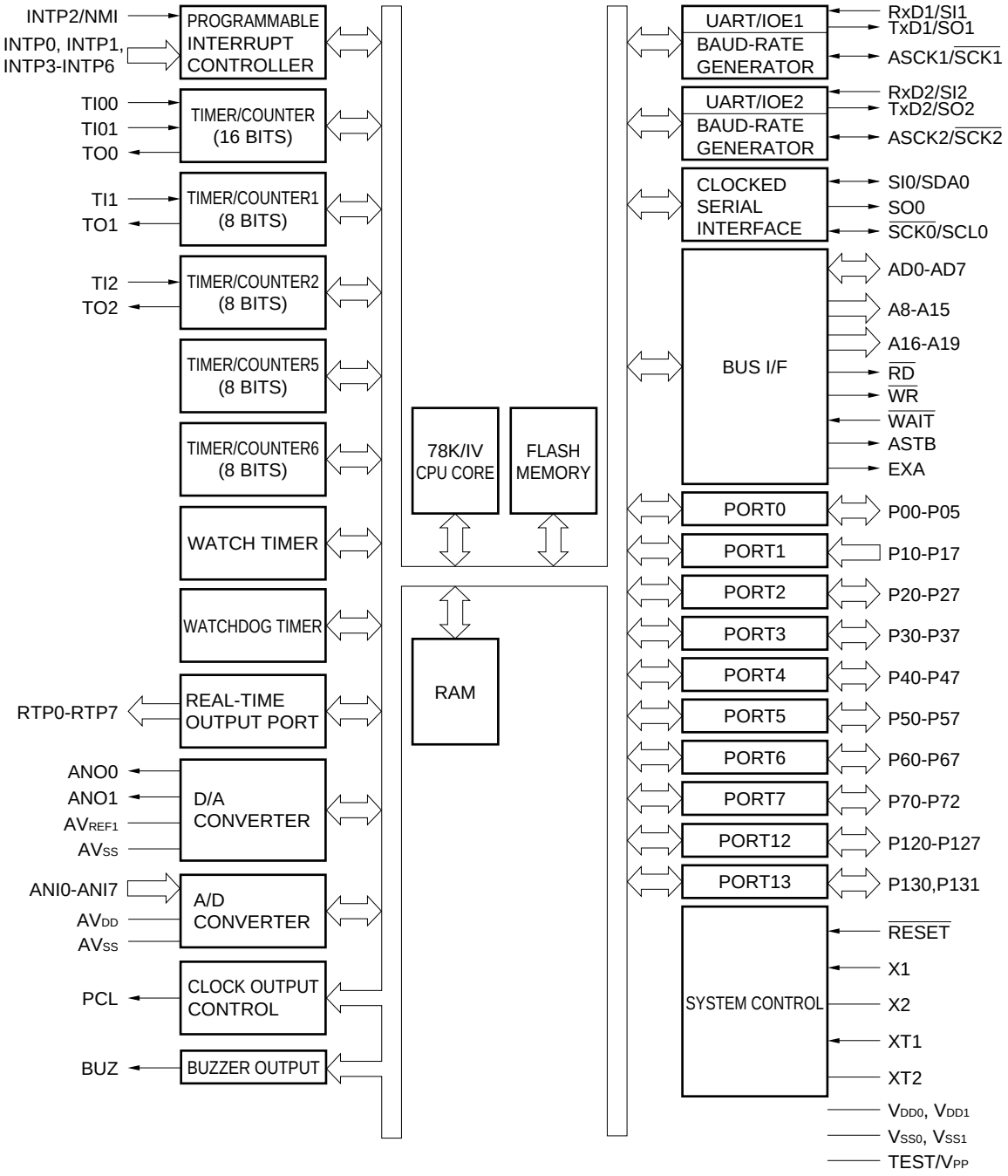
Notes 1. Directly connect the TEST/V_{PP} pin to V_{SS0} in normal operation mode.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When using in applications where noise from inside the microcomputer has to be reduced, it is recommended to take countermeasures against noise such as supplying power to V_{DD0} and V_{DD1} independently, and connecting V_{SS0} and V_{SS1} to different ground lines.

A8-A19	:	Address Bus	P130, P131	:	Port13
AD0-AD7	:	Address/Data Bus	PCL	:	Programmable Clock
ANI0-ANI7	:	Analog Input	$\overline{RD}$	:	Read Strobe
ANO0, ANO1	:	Analog Output	$\overline{RESET}$	:	Reset
ASCK1, ASCK2	:	Asynchronous Serial Clock	RTP0-RTP7	:	Real-time Output Port
ASTB	:	Address Strobe	RxD1, RxD2	:	Receive Data
AV_{DD}	:	Analog Power Supply	$\overline{SCK0}$-$\overline{SCK2}$	:	Serial Clock
AV_{REF1}	:	Analog Reference Voltage	SCL0	:	Serial Clock
AV_{SS}	:	Analog Ground	SDA0	:	Serial Data
BUZ	:	Buzzer Clock	SI0-SI2	:	Serial Input
EXA	:	External Access Status Output	SO0-SO2	:	Serial Output
INTP0-INTP5	:	Interrupt from Peripherals	TEST	:	Test
NMI	:	Non-maskable Interrupt	TI00, TI01, TI1-TI2	:	Timer Input
P00-P05	:	Port0	TO0-TO2	:	Timer Output
P10-P17	:	Port1	TxD1, TxD2	:	Transmit Data
P20-P27	:	Port2	V_{DD0}, V_{DD1}	:	Power Supply
P30-P37	:	Port3	V_{PP}	:	Programming Power Supply
P40-P47	:	Port4	V_{SS0}, V_{SS1}	:	Ground
P50-P57	:	Port5	$\overline{WAIT}$	:	Wait
P60-P67	:	Port6	$\overline{WR}$	:	Write Strobe
P70-P72	:	Port7	X1, X2	:	Crystal (Main System Clock)
P120-P127	:	Port12	XT1, XT2	:	Crystal (Subsystem Clock)

3. BLOCK DIAGRAM



4. PIN FUNCTION

4.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00	I/O	INTP0	Port 0 (P0): • 6-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P01		INTP1	
P02		INTP2/NMI	
P03		INTP3	
P04		INTP4	
P05		INTP5	
P10-P17	Input	ANI0-ANI7	Port 1 (P1): • 8-bit input port
P20	I/O	RxD1/SI1	Port 2 (P2): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P21		TxD1/SO1	
P22		ASCK1/$\overline{\text{SCK1}}$	
P23		PCL	
P24		BUZ	
P25		SI0/SDA0	
P26		SO0	
P27		$\overline{\text{SCK0}}$/SCL0	
P30	I/O	TO0	Port 3 (P3): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P31		TO1	
P32		TO2	
P33		TI1	
P34		TI2	
P35		TI00	
P36		TI01	
P37		EXA	
P40-P47	I/O	AD0-AD7	Port 4 (P4): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.
P50-P57	I/O	A8-A15	Port 5 (P5): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.

4.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P60	I/O	A16	Port 6 (P6): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software.
P61		A17	
P62		A18	
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$	
P67		ASTB	
P70	I/O	RxD2/SI2	Port 7 (P7): • 3-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise.
P71		TxD2/SO2	
P72		ASCK2/$\overline{SCK2}$	
P120-P127	I/O	RTP0-RTP7	Port 12 (P12): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise.
P130, P131	I/O	ANO0, ANO1	Port 13 (P13): • 2-bit I/O port • Can be set in input or output mode bit-wise.

4.2 Pins Other Than Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
TI00	Input	P35	External count clock input to 16-bit timer register
TI01		P36	Capture trigger signal input to capture/compare register 00
TI1		P33	External count clock input to 8-bit timer register 1
TI2		P34	External count clock input to 8-bit timer register 2
TO0	Output	P30	16-bit timer output (shared by 14-bit PWM output)
TO1		P31	8-bit timer output (shared by 8-bit PWM output)
TO2		P32	
RxD1	Input	P20/SI1	Serial data input (UART1)
RxD2		P70/SI2	Serial data input (UART2)
TxD1	Output	P21/SO1	Serial data output (UART1)
TxD2		P71/SO2	Serial data output (UART2)
ASCK1	Intput	P22/$\overline{SCK1}$	Baud rate clock input (UART1)
ASCK2		P72/$\overline{SCK2}$	Baud rate clock input (UART2)
SI0	Input	P25/SDA0	Serial data input (3-wire serial clock I/O0)
SI1		P20/RxD1	Serial data input (3-wire serial clock I/O1)
SI2		P70/RxD2	Serial data input (3-wire serial clock I/O2)
SO0	Output	P26	Serial data output (3-wire serial I/O0)
SO1		P21/TxD1	Serial data output (3-wire serial I/O1)
SO2		P71/TxD2	Serial data output (3-wire serial I/O2)
SDA0	I/O	P25/SI0	Serial data input/output (I^2C bus)
$\overline{SCK0}$	I/O	P27/SCL0	Serial clock input/output (3-wire serial I/O0)
$\overline{SCK1}$		P22/ASCK1	Serial clock input/output (3-wire serial I/O1)
$\overline{SCK2}$		P72/ASCK2	Serial clock input/output (3-wire serial I/O2)
SCL0		P27/$\overline{SCK0}$	Serial clock input/output (I^2C bus)
NMI	Input	P02/INTP2	Non-maskable interrupt request input
INTP0		P00	External interrupt request input
INTP1		P01	
INTP2		P02/NMI	
INTP3		P03	
INTP4		P04	
INTP5		P05	
PCL	Output	P23	Clock output (for trimming main system clock and subsystem clock)
BUZ	Output	P24	Buzzer output
RTP0-RTP7	Output	P120-P127	Real-time output port that outputs data in synchronization with trigger
AD0-AD7	I/O	P40-P47	Low-order address/data bus when external memory is connected
A8-A15	Output	P50-P57	Middle-order address bus when external memory is connected
A16-A19		P60-P63	High-order address bus when external memory is connected
$\overline{RD}$	Output	P64	Strobe signal output for read operation of external memory
$\overline{WR}$		P65	Strobe signal output for write operation of external memory

4.2 Pins Other Than Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
$\overline{WAIT}$	Input	P66	To insert wait state(s) when external memory is accessed
ASTB	Output	P67	Strobe output to externally latch address information output to ports 4 through 6 to access external memory
EXA	Output	P37	External access status output
$\overline{RESET}$	Input	—	System reset input
X1	Input	—	To connect main system clock oscillation crystal
X2	—		
XT1	Input	—	To connect subsystem clock oscillation crystal
XT2	—		
ANI0-ANI7	Input	P10-P17	Analog voltage input for A/D converter
ANO0, ANO1	Output	P130, P131	Analog voltage output for D/A converter
AV_{REF1}	—	—	To apply reference voltage for D/A converter
AV_{DD}			Positive power supply for A/D converter. Connected to V_{DD0}.
AV_{SS}			GND for A/D converter and D/A converter. Connected to V_{SS0}.
V_{DD0}			Positive power supply for port block
V_{SS0}			GND potential for port block
V_{DD1}			Positive power supply (except port block)
V_{SS1}			GND potential (except port block)
TEST		V_{PP}	Directly connect this pin to V_{SS} (this pin is for IC test).
V_{PP}		TEST	Sets flash memory programming mode. To apply a high voltage when program is written or verified.

4.3 I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins

Table 4-1 shows symbols indicating the I/O circuit types of the respective pins and the recommended connection of unused pins.

For the circuit diagram of each type of I/O circuit, refer to **Figure 4-1**.

Table 4-1. I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins (1/2)

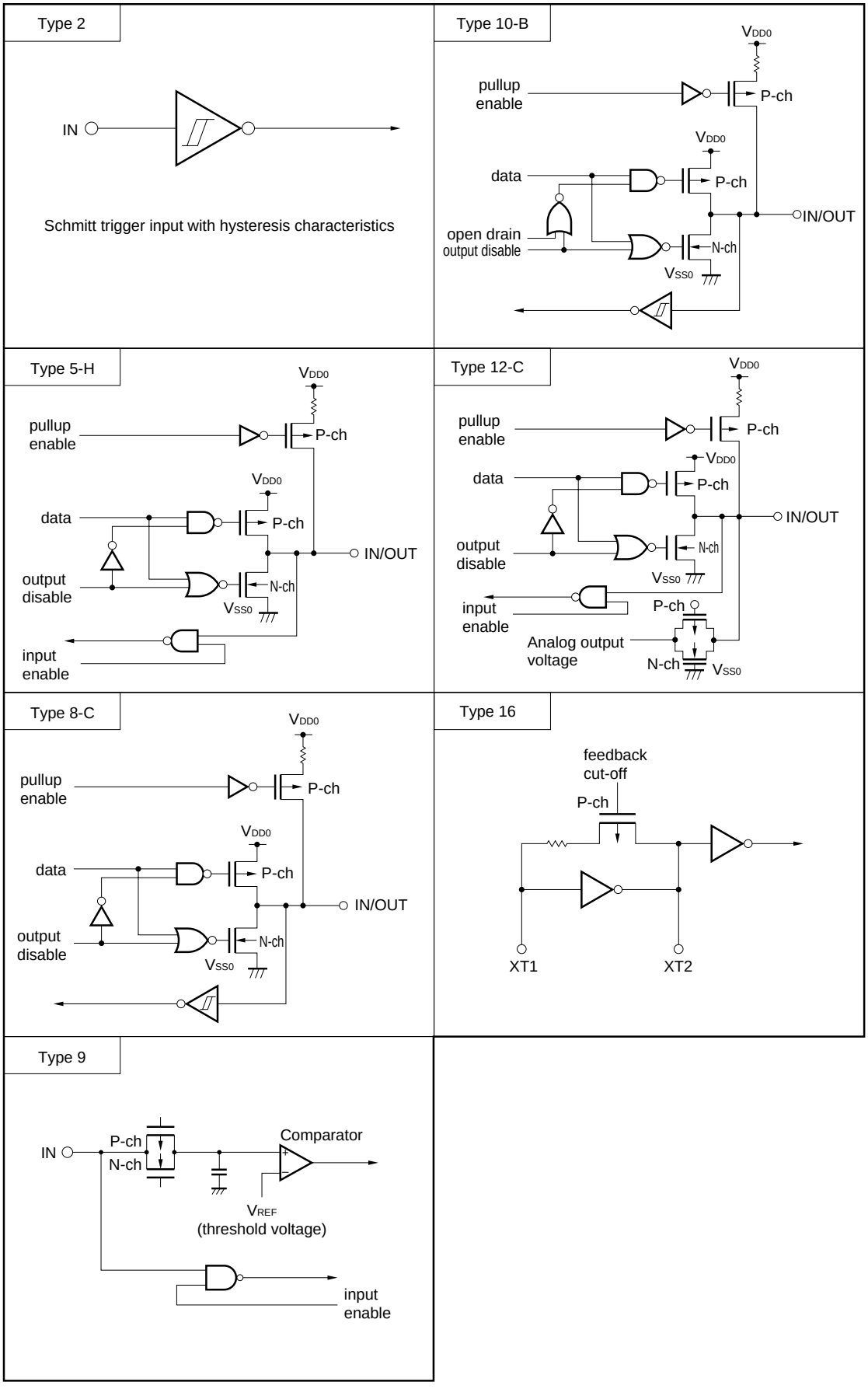
Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	8-C	I/O	Input : Individually connected to V_{SS0} via resistor Output: Open
P01/INTP1			
P02/INTP2/NMI			
P03/INTP3-P05/INTP5			
P10/ANI0-P17/ANI7	9	Input	Connected to V_{SS0} or V_{DD0}
P20/RxD1/SI1	10-B	I/O	Input : Individually connected to V_{SS0} via resistor Output: Open
P21/TxD1/SO1			
P22/ASCK1/$\overline{SCK1}$			
P23/PCL			
P24/BUZ			
P25/SDA0/SI0			
P26/SO0			
P27/SCL0/$\overline{SCK0}$			
P30/TO0-P32/TO2	8-C		
P33/TI1, P34/TI2			
P35/TI00, P36/TI01			
P37/EXA			
P40/AD0-P47/AD7	5-H		
P50/A8-P57/A15			
P60/A16-P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/RxD2/SI2	8-C		
P71/TxD2/SO2			
P72/ASCK2/$\overline{SCK2}$			
P120/RTP0-P127/RTP7			
P130/ANO0, P131/ANO1	12-C		

Table 4-1. I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
$\overline{\text{RESET}}$	2	Input	—
XT1	16		Connected to V_{SS0}
XT2		—	Open
AV_{REF1}	—		Connected to V_{DD0}
AV_{DD}			
AV_{SS}			Connected to V_{SS0}
TEST/V_{PP}			Directly connected to V_{SS0}

Remark Because the circuit type numbers are standardized among the 78K series products, they are not sequential in some models (i.e., some circuits are not provided).

Figure 4-1. Types of Pin I/O Circuits



5. INTERNAL MEMORY SIZE SELECT REGISTER (IMS)

The IMS is a register that prevents by software a part of the internal memory from being used. By using this register, the memory of the μPD78F4225Y can be mapped in the same manner as a mask ROM model with different internal memory (ROM and RAM) capacity.

This register is set by using an 8-bit memory manipulation instruction.

Its value is set to FFH by $\overline{\text{RESET}}$ input.

Figure 5-1. Format of Internal Memory Size Select Register (IMS)

Address: 0FFFCH At reset: FFH W

	7	6	5	4	3	2	1	0
IMS	1	1	ROM1	ROM0	1	1	RAM1	RAM0

ROM1	ROM0	Selects internal ROM capacity
0	0	48K bytes
0	1	64K bytes
1	0	96K bytes
1	1	128K bytes

RAM1	RAM0	Selects peripheral RAM capacity
0	0	1536 bytes
0	1	2304 bytes
1	0	3072 bytes
1	1	3840 bytes

Caution IMS is not provided on the mask ROM models (μPD784224Y and 784225Y).

The value to be set to the IMS to map the memory of the μPD78F4225Y in the same manner as the mask ROM model is shown in Table 5-1.

Table 5-1. Set Value of Internal Memory Size Select Register (IMS)

Mask ROM Model	Set Value of IMS
μPD784225Y	EEH
μPD784226Y	FFH

6. PROGRAMMING FLASH MEMORY

The flash memory can be written with the μPD78F4225Y mounted on the target board (on-board). To do so, connect a dedicated flash writer (Flashpro II) to the host machine and target system.

Remark Flashpro II is a product of Naito Densei Machida Mfg. Co., Ltd.

6.1 Selecting Communication Mode

To write the flash memory, use Flashpro II and serial communication. Select a serial communication mode from those listed in Table 6-1 in the format shown in Figure 6-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 6-1.

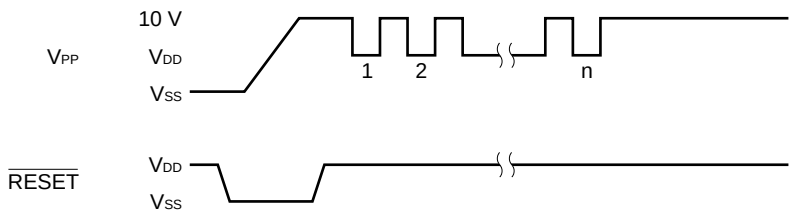
Table 6-1. Communication Modes

Communication Mode	Number of Channels	Pins Used	Number of V_{PP} Pulses
3-wire serial I/O	3	$\overline{SCK0}$/SCL0/P27 SO0/P26 SI0/SDA0/P25	0
		$\overline{SCK1}$/ASCK1/P22 SO1/TxD1/P21 SI1/RxD1/P20	1
		$\overline{SCK2}$/ASCK2/P72 SO2/TxD2/P71 SI2/RxD2/P70	2
I^2C bus	1	SCL0/$\overline{SCK0}$/P27 SDA0/SI0/P25	4
UART	2	TxD1/SO1/P21 RxD1/SI1/P20	8
		TxD2/SO2/P71 RxD2/SI2/P70	9
Psendo-3-wire serial I/O[Note]	1	P32/TO2 (serial clock I/O) P31/TO1 (serial data output) P30/TO0 (serial data output)	12

Note Performs serial transfer by controlling port by software.

Caution Be sure to select a communication mode with the number of V_{PP} pulses shown in Table 6-1.

Figure 6-1. Communication Mode Selecting Format



6.2 Flash Memory Programming Function

The flash memory is written by transferring or receiving commands and data in a selected communication mode. The major functions of flush memory programming are listed in Table 6-2.

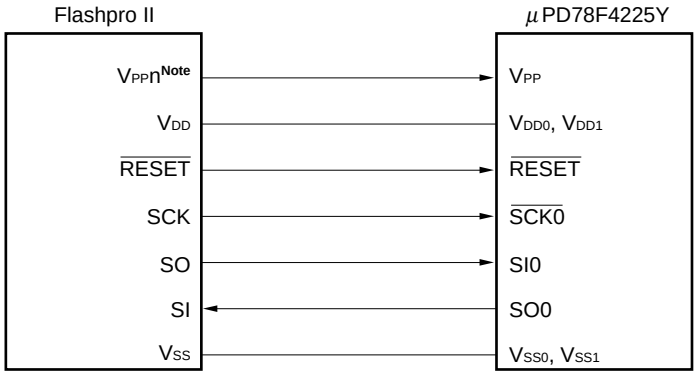
Table 6-2. Major Functions of Flash Memory Programming

Function	Description
Batch erasure	Erases all contents of memory.
Block erasure	Erases contents of specified memory block.
Batch blank check	Checks erased status of entire memory.
Block blank check	Checks erased status of specified block
Data write	Writes flash memory based on write start address and number of data to be written (in bytes).
Batch verify	Compares all contents of memory with input data.
Block verify	Compares contents of specified memory block with input data.

6.3 Connecting Flashpro II

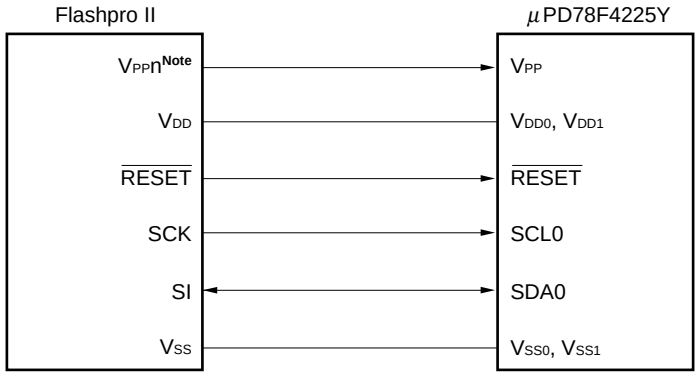
The Flashpro II and μPD78F4225Y are connected differently depending on the selected communication mode. Figures 6-2 through 6-5 show the connections in the respective communication modes.

Figure 6-2. Connection of Flashpro II in 3-Wire Serial I/O Mode (When Using 3-Wire Serial I/O 0)



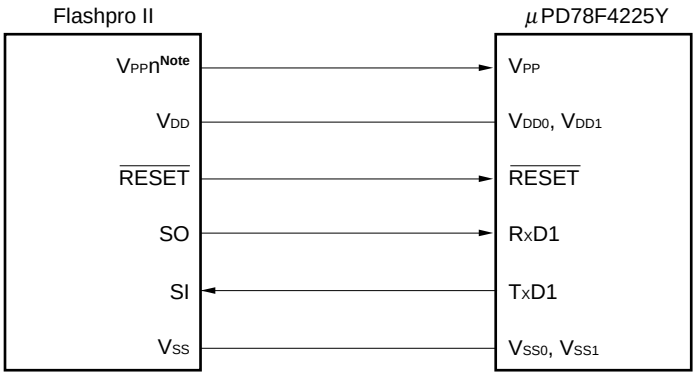
Note n = 1, 2

Figure 6-3. Connection of Flashpro II in I²C Bus Mode



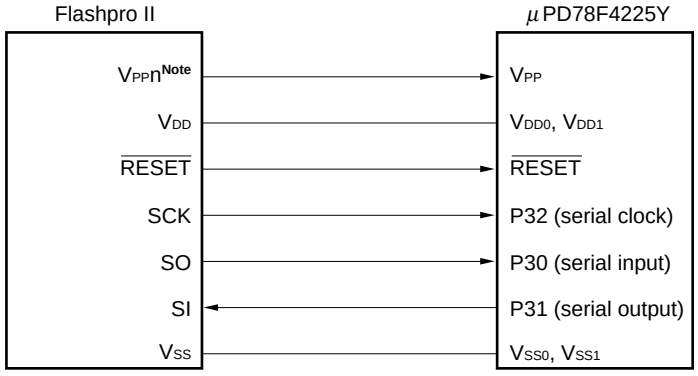
Note n = 1, 2

Figure 6-4. Connection of Flashpro II in UART Mode (When Using UART1)



Note n = 1, 2

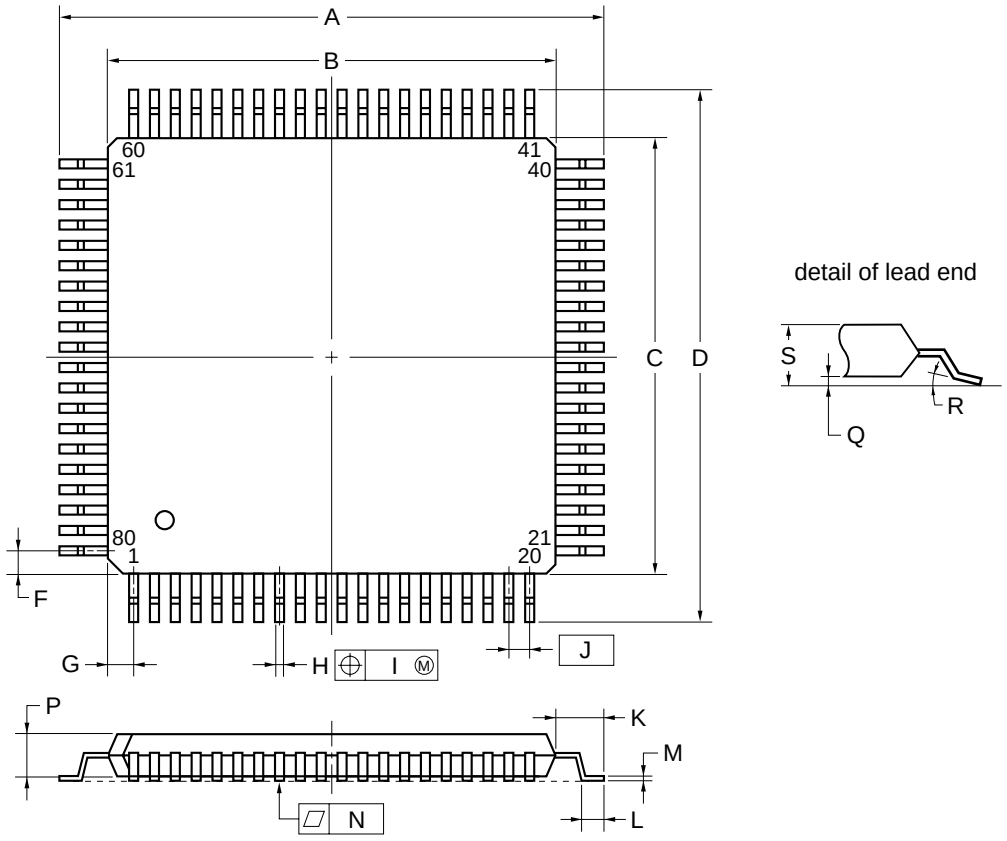
Figure 6-5. Connection of Flashpro II in Pseudo-3-Wire Serial I/O Mode



Note n = 1, 2

7. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



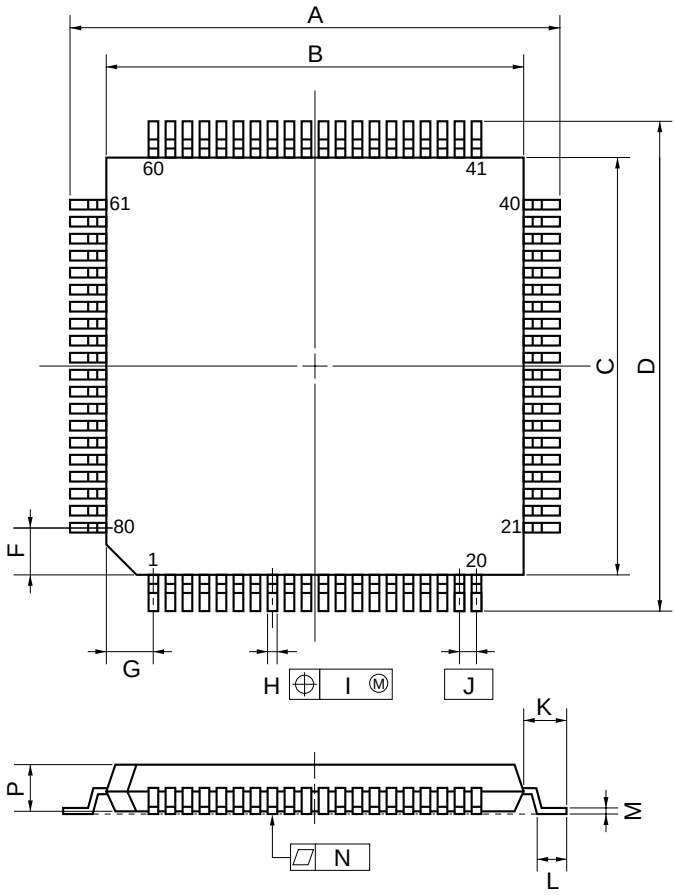
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

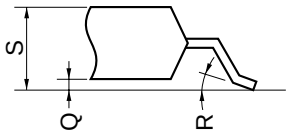
ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



detail of lead end



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for supporting development of a system using the μPD78F4225Y.

Language processor software

RA78K4[Note 1]	Assembler package common to 78K/IV series
CC78K4[Note 1]	C compiler package common to 78K/IV series
CC78K4-L[Note 1]	C compiler library source file common to 78K/IV series

Flash memory writing tool

Flashpro II	Dedicated flash writer. Flashpro is the product of Naito Densei Machida Mfg. Co., Ltd.
Product name pending	Adapter for flash memory writing.

Debugging tool

IE-784000-R	In-circuit emulator common to 78K/IV series
IE-784000-R-BK	Break board common to 78K/IV series
IE-784218-R-EM1 IE-784000-R-EM	Emulation board for evaluation of μPD784225Y subseries
IE-70000-98-IF-B	Interface adapter when PC-9800 series (except notebook type) is used as host machine
IE-70000-98N-IF	Interface adapter and cable when notebook type PC-9800 series is used as host machine
IE-70000-PC-IF-B	Interface adapter when IBM PC/AT™ is used as host machine
IE-78000-R-SV3	Interface adapter and cable when EWS is used as host machine
Product name pending	Emulation probe common to μPD784225Y subseries
SM78K4[Note 2]	System simulator common to 78K/IV series
ID78K4[Note 2]	Integrated debugger for IE-784000-R
DF784225 (Pending)[Note 3]	Device file for μPD784225Y subseries

Real-time OS

RX78K/IV[Note 3]	Real-time OS for 78K/IV series
MX78K4[Note 4]	OS for 78K/IV series

Remark RA78K4, CC78K4, SM78K4, and ID78K4 are used in combination with DF784225.

Notes 1.
- PC-9800 series (MS-DOS™) base
- IBM PC/AT and compatible machine (PC DOS™, Windows™, MS-DOS, IBM DOS™) base
- HP9000 series 700™ (HP-UX™) base
- SPARCstation™ (SunOS™) base
- NEWS™ (NEWS-OS™) base

2.
- PC-9800 series (MS-DOS+Windows) base
- IBM PC/AT and compatible machine (PC DOS, Windows, MS-DOS, IBM DOS) base
- HP9000 series 700 (HP-UX) base
- SPARCstation (SunOS) base

3.
- PC-9800 series (MS-DOS) base
- IBM PC/AT and compatible machine (PC DOS, Windows, MS-DOS, IBM DOS) base
- HP9000 series 700 (HP-UX) base
- SPARCstation (SunOS) base

4.
- PC-9800 series (MS-DOS) base
- IMB PC/AT and compatible machine (PC DOS, Windows, MS-DOS, IBM DOS) base

APPENDIX B. RELATED DOCUMENTS

Documents related to device

Document Name	Document No.	
	Japanese	English
μPD784224Y, 784225Y Preliminary Product Information	U12376J	Planned
μPD78F4225Y Preliminary Product Information	U11824J	This document
μPD784225, 784225Y Subseries User's Manual - Hardware	Planned	Planned
μPD784225Y Subseries Special Function Register Table	Planned	–
78K/IV Series User's Manual - Instruction	U10905J	U10905E
78K/IV Series Instruction Table	U10594J	–
78K/IV Series Instruction Set	U10595J	–
78K/IV Series Application Note - Software Basics	U10095J	–

Documents related to development tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K4 Assembler Package	Operation	U11334J	U11334E
	Language	U11162J	–
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K4 Series	Operation	EEU-960	–
	Language	EEU-961	–
CC78K Series Library Source File		U12322J	–
IE-784000-R		EEU-5004	EEU-1534
IE-784218-R-EM1		U12155J	U12155E
SM78K4 System Simulator - Windows Base	Reference	U10093J	U10093E
SM78K Series System Simulator	External component user open interface specification	U10092J	U10092E
ID78K4 Integrated Debugger - Windows based	Reference	U10440J	U10440E

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of a document for designing.

Documents related to embedded software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Basics	U10603J	–
	Installation	U10604J	–
	Debugger	U10364J	–
78K/IV Series OS MX78K4	Basics	U11779J	–

Other documents

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	–
Guide to Quality Assurance for Semiconductor Devices	C11893J	MEI-1202
Guide to Microcomputer-Related Products by Third Parties	U11416J	–

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 0211-65 03 490

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