M5M4C1000P, J, L-10, -12, -15

FAST PAGE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 1-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{RAS}$-only refresh mode, the hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

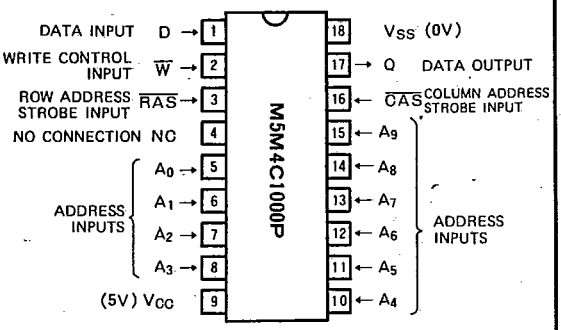
Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M4C1000P-10 M5M4C1000J-10 M5M4C1000L-10	100	25	50	190	300
M5M4C1000P-12 M5M4C1000J-12 M5M4C1000L-12	120	30	55	220	250
M5M4C1000P-15 M5M4C1000J-15 M5M4C1000L-15	150	40	70	260	200

- High performance CMOS technology
- Standard 18 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low standby power dissipation
  5.5mW (Max) . . . . . CMOS Input level
- Low operating power dissipation
  M5M4C1000P, J, L-10 . . . . . 413mW (Max)
  M5M4C1000P, J, L-12 . . . . . 358mW (Max)
  M5M4C1000P, J, L-15 . . . . . 303mW (Max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-Modify-write, $\overline{RAS}$-only-Refresh, Fast-Page-Mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All inputs, output TTL compatible and low capacitance.
- 512 refresh cycles every 8ms
- $\overline{CAS}$ controlled output allows hidden refresh
- Wide $\overline{RAS}$ low pulse width for
  Fast-Page-Mode . . . . . 100μs Max

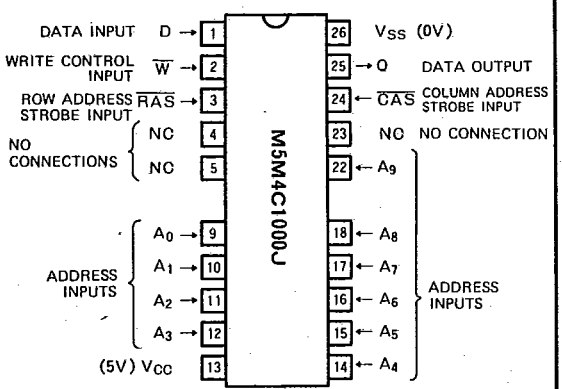
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

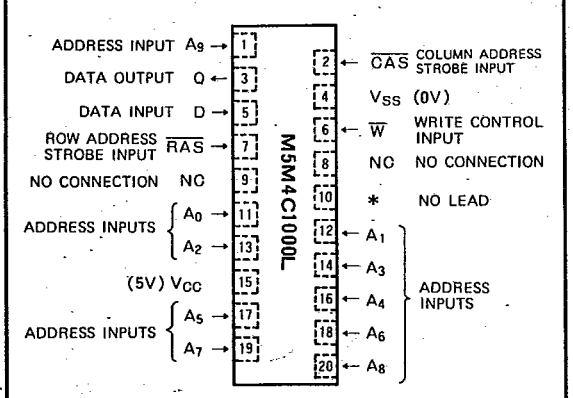
PIN CONFIGURATION (TOP VIEW)



Outline 18P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L (ZIP)

MITSUBISHI ELECTRIC

FAST PAGE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

T-46-23-15

FUNCTION

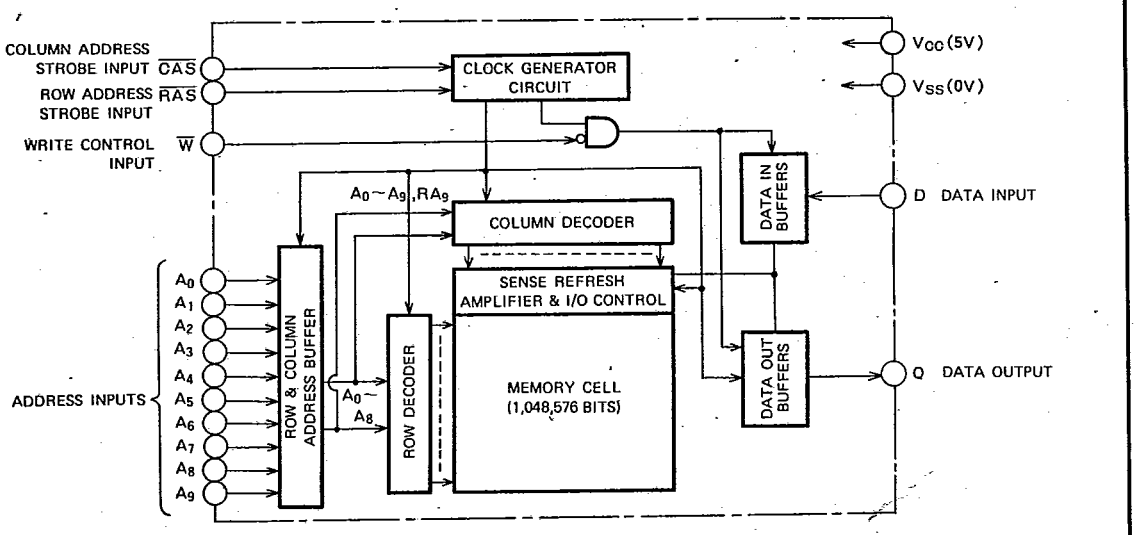
The M5M4C1000P, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast-page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

BLOCK DIAGRAM



T-46-23-15

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature	—	−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5, Other input pins=0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M4C1000-10	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}=t_{WC}$=min, output open			75	mA
		M5M4C1000-12				65	
		M5M4C1000-15				55	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}=\overline{CAS}=V_{IH}$, output open			2	mA
			$\overline{RAS}=\overline{CAS}\geqq V_{CC}-0.5$, output open			1	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M4C1000-10	$\overline{RAS}$ cycling, $\overline{CAS}=V_{IH}$ t_{RC}=min, output open			75	mA
		M5M4C1000-12				65	
		M5M4C1000-15				55	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast page mode (Note 3, 4)	M5M4C1000-10	$\overline{RAS}=V_{IL}$, $\overline{CAS}$=cycling t_{PC}=min, output open			65	mA
		M5M4C1000-12				55	
		M5M4C1000-15				45	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4C1000-10	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min, output open			75	mA
		M5M4C1000-12				65	
		M5M4C1000-15				55	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	$V_I=V_{SS}$ f=1MHz V_i=25mVrms			6	pF
$C_{I(D)}$	Input capacitance, data input				5	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
C_O	Output capacitance	$V_O=V_{SS}$, f=1MHz, V_i=25mVrms			7	pF

SWITCHING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		25		30		40	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		100		120		150	ns
t_{CAA}	Column address access time	(Note 6, 9)		50		55		70	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		55		60		75	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	20	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper devise operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCD(max)} \leqq t_{RCD}$ and $t_{RAD(max)} \geqq t_{RAD}$.
8: Assume that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$.
9: Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.
10: Assume that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
11: $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted, see notes 12, 13)

Symbol	Parameter		Limits						Unit
			M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		80		90		100		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	20	75	25	90	30	110	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 15)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 16)	25		30		35		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 17)	15	50	20	65	25	80	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	20	0	20	0	25	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		20		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low or $\overline{W}$ low		20		20		25		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low		95		110		135		ns
t_T	Transition time	(Note 19)	3	50	3	50	3	50	ns

Note 12: The timing requirements are assumed t_T = 5ns.
13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} as shown in note 7, 9.
15: t_{CRP} requirement is applicable for all $\overline{RAS}$/$\overline{CAS}$ cycles.
16: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)} - t_T$ except for t_{CP} of fast page mode cycle.
17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle.
18: $t_{ASC(max)}$ is specified as a reference point only of address access time.
19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

FAST PAGE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

T-46-23-15

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width		100	10000	120	10000	150	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		25		30		40		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time		50		55		70		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time		0		0		0		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle

Symbol	Parameter		Limits						Unit
			M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width		100	10000	120	10000	150	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		25		30		40		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 23)	−5		−5		−5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		20		25		30		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low		95		115		140		ns
t_{WP}	Write pulse width		20		25		30		ns
t_{DS}	Data setup time		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low		20		25		30		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low		95		115		140		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
			Min	Max	Min	Max	Min	Max	
t_{RWC}	Read-Write cycle time	(Note 21)	200		255		300		ns
t_{RMWC}	Read-Modify-Write cycle time	(Note 22)	220		255		300		ns
t_{RAS}	$\overline{RAS}$ low pulse width		130	10000	155	10000	190	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		55	10000	65	10000	80	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		130		155		190		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		55		65		80		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to write low	(Note 23)	25		30		40		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to write low	(Note 23)	100		120		150		ns
t_{CWL}	$\overline{CAS}$ hold time after write low		25		30		35		ns
t_{RWL}	$\overline{RAS}$ hold time after write low		25		30		35		ns
t_{WP}	Write pulse width		20		25		30		ns
t_{DS}	Data setup time		0		0		0		ns
t_{DH}	Data hold time after write low		20		25		30		ns
t_{AWD}	Delay time, address to write low	(Note 23)	50		55		70		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)} = t_{RCD(max)} + t_{CWD(min)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.
22: t_{RMWC} is specified as $t_{RMWC(min)} = t_{RAC(max)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.
23: t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} do not define the limits of operation, but are included as electrical characteristics only. When $t_{RWD} \geqq t_{RWD(min)}$, $t_{CWD} \geqq t_{CWD(min)}$ and $t_{AWD} \geqq t_{AWD(min)}$, a read-write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above condition is satisfied, the condition of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
When $t_{WCS} \geqq t_{WCS(min)}$, an early-write cycle is performed, and the data output keeps the high-impedance state.

Fast Page Mode Cycle (Read, Early Write, Read-Write Read-Modify-Write Cycles)

Symbol	Parameter		Limits						Unit
			M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
			Min	Max	Min	Max	Min	Max	
t_{PC}	Fast Page mode cycle time		60		65		80		ns
t_{RWPC}	Fast Page mode R/W, R/M/W cycle time		90		100		120		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read, write cycle		160	100000	185	100000	230	100000	ns
t_{CAS}	$\overline{CAS}$ low pulse width for read cycle		25	10000	30	10000	40	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 24)	15	25	15	25	20	30	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		25		30		40		ns

Note 24: $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leqq t_{CP}$, access time is assumed by t_{CAC}.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 25)

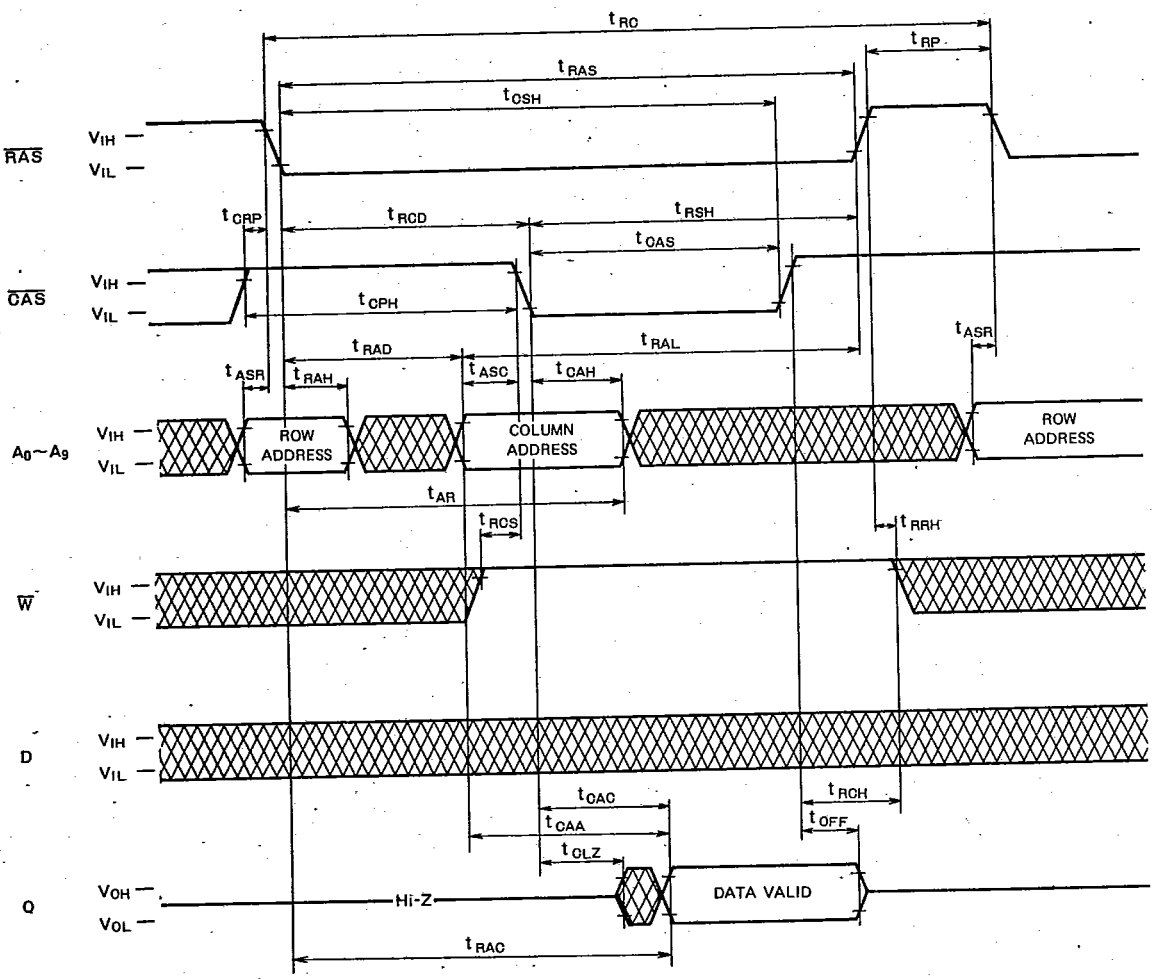
Symbol	Parameter	Limits						Unit
		M5M4C1000-10		M5M4C1000-12		M5M4C1000-15		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	20		25		30		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 25: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

T-46-23-15

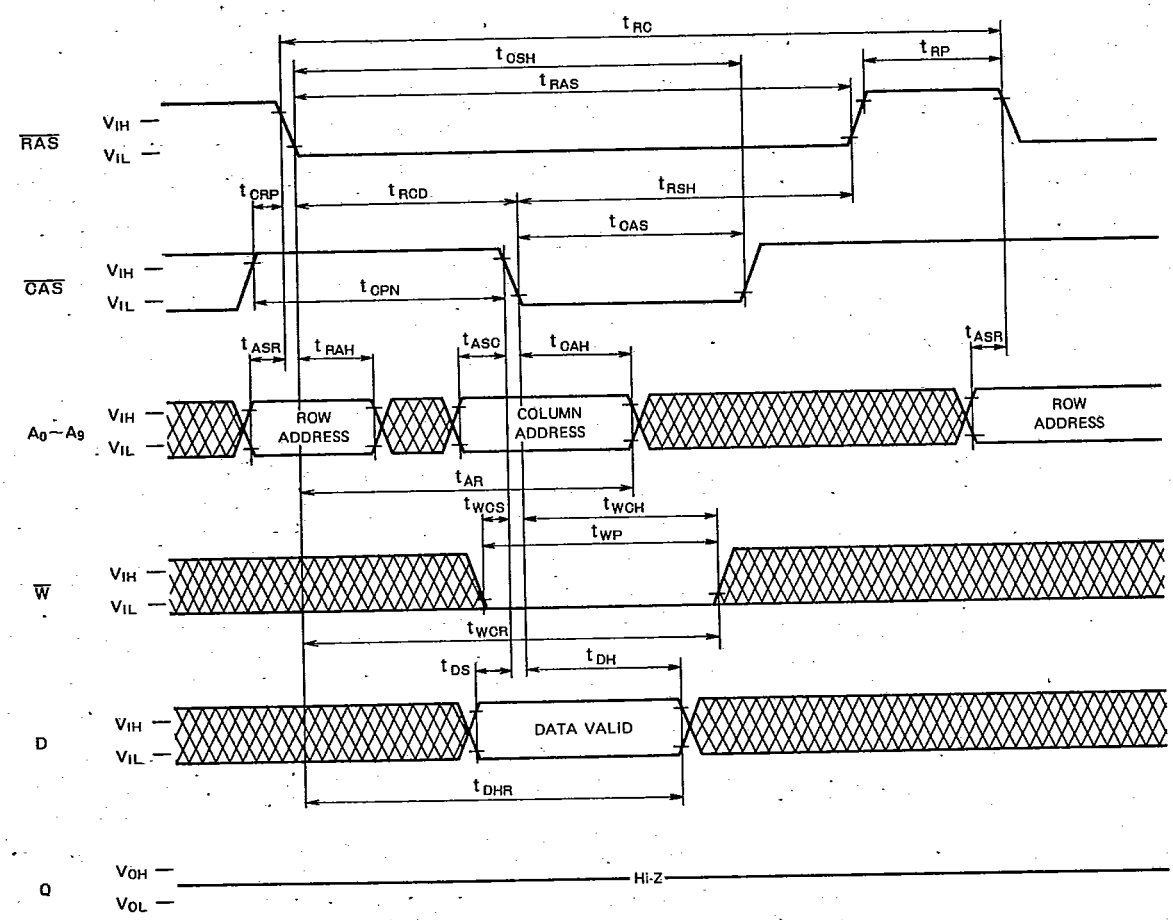
Timing Diagrams (Note 26)

Read Cycle



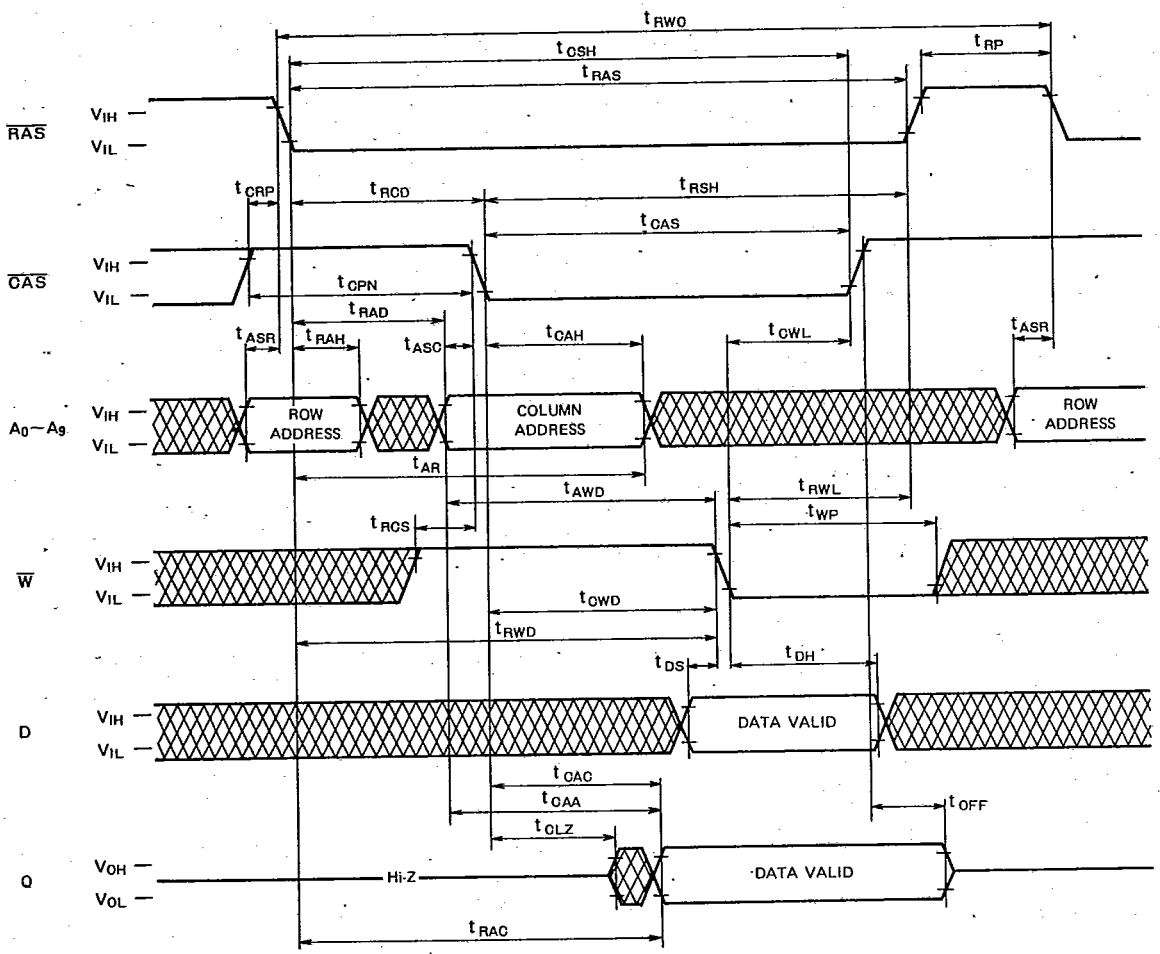
Note 26 Indicates the don't care input.

Write Cycle (Early write)



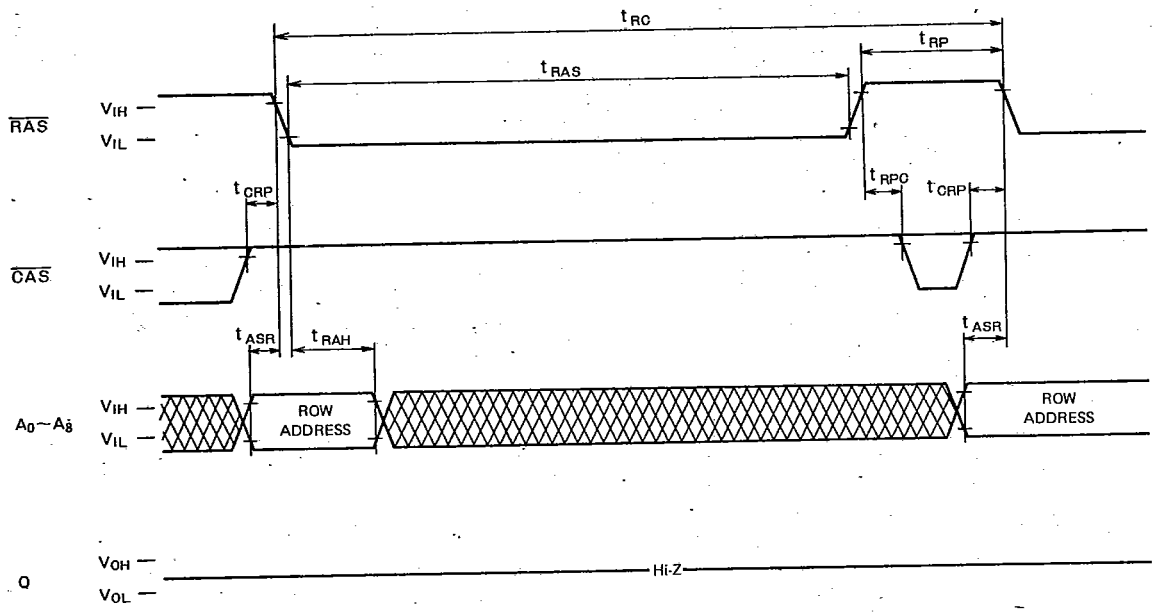
T-46-23-15

Read-Write, Read-Modify-Write Cycle



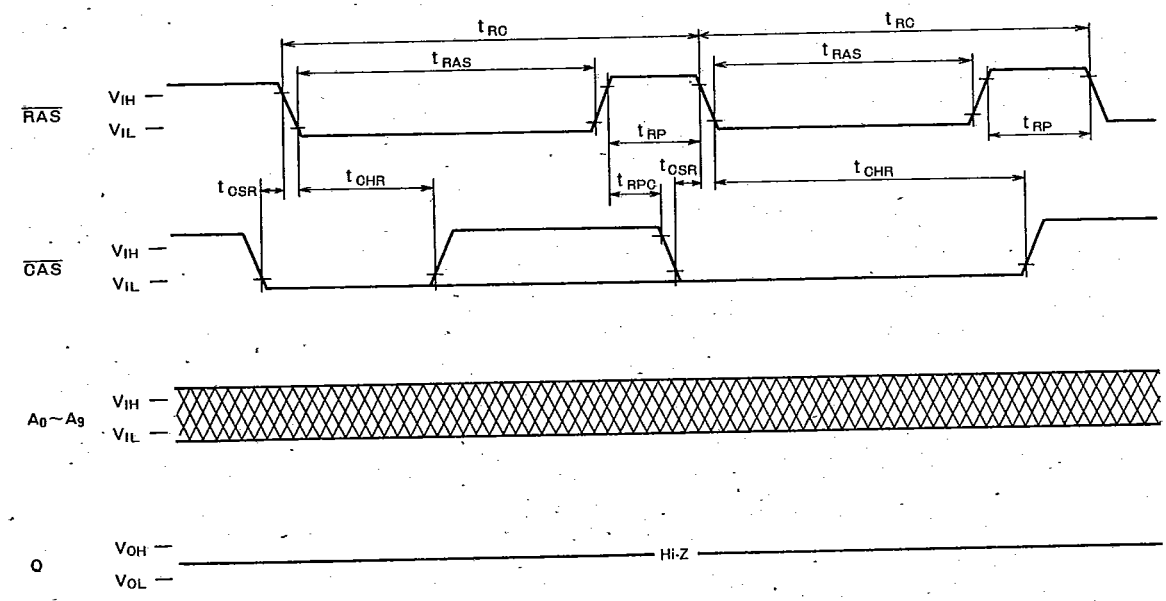
T-46-23-15

$\overline{RAS}$-only Refresh Cycle (Note 27)



Note 27: $\overline{W}$, D = don't care, A_9 may be V_{IH} or V_{IL}

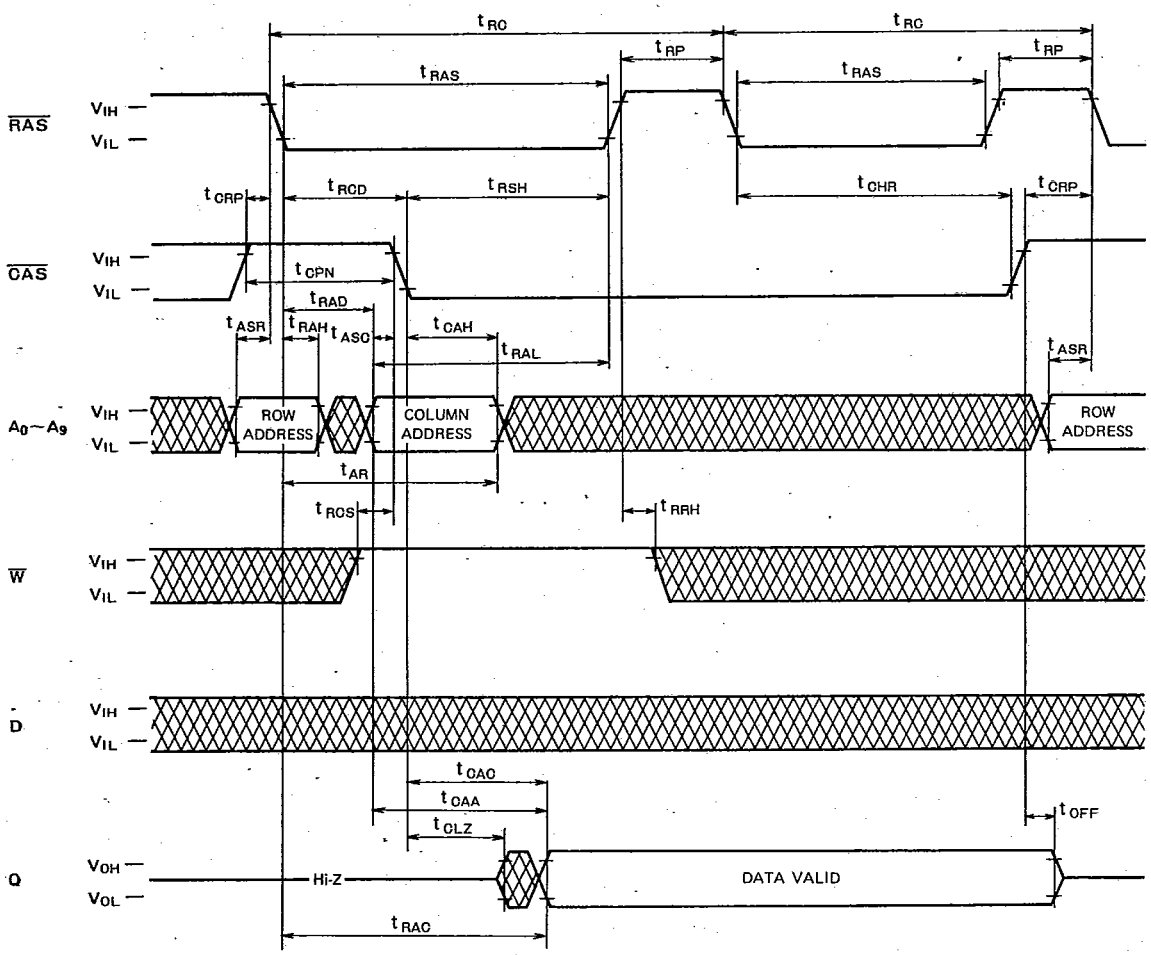
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)



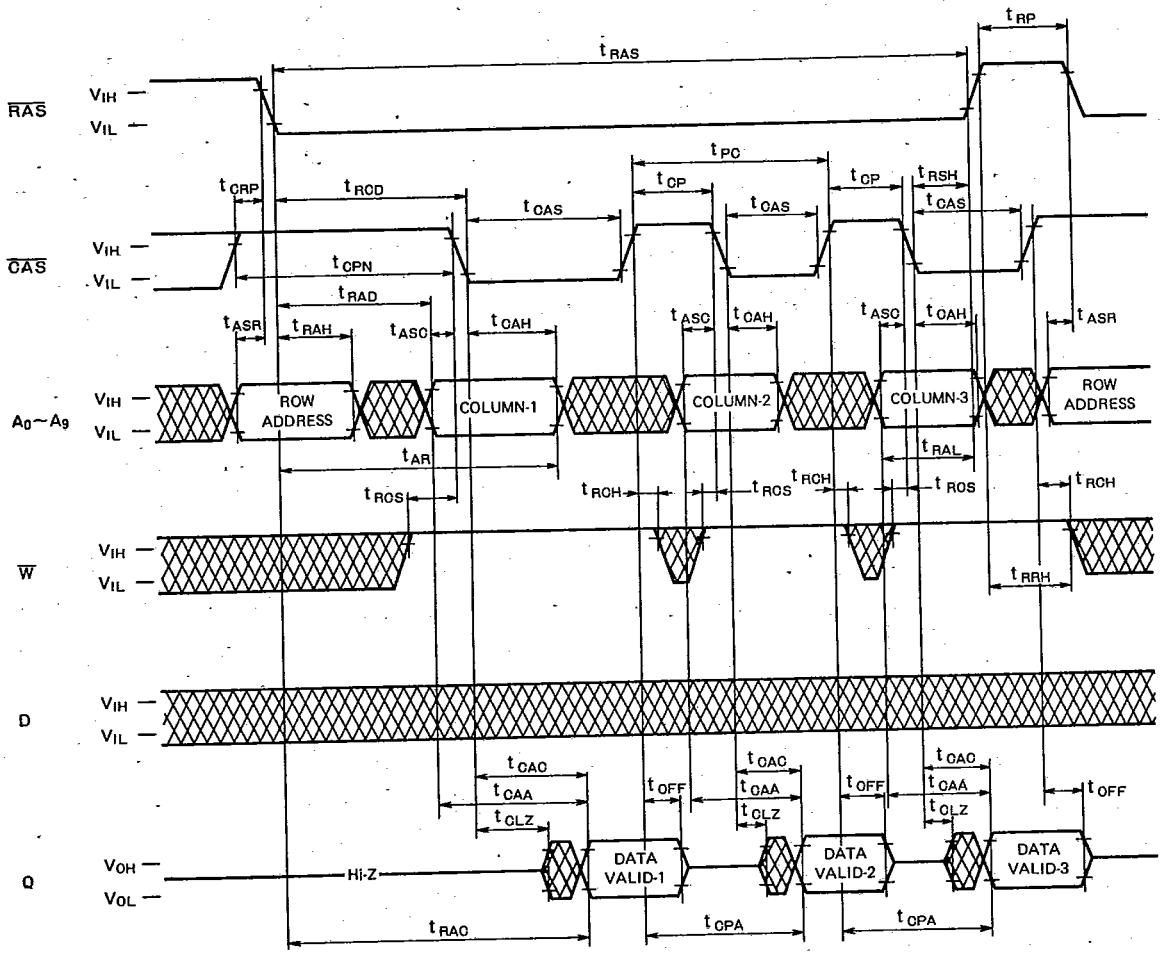
Note 28: $\overline{W}$, D = don't care

T-46-23-15

Hidden Refresh Cycle

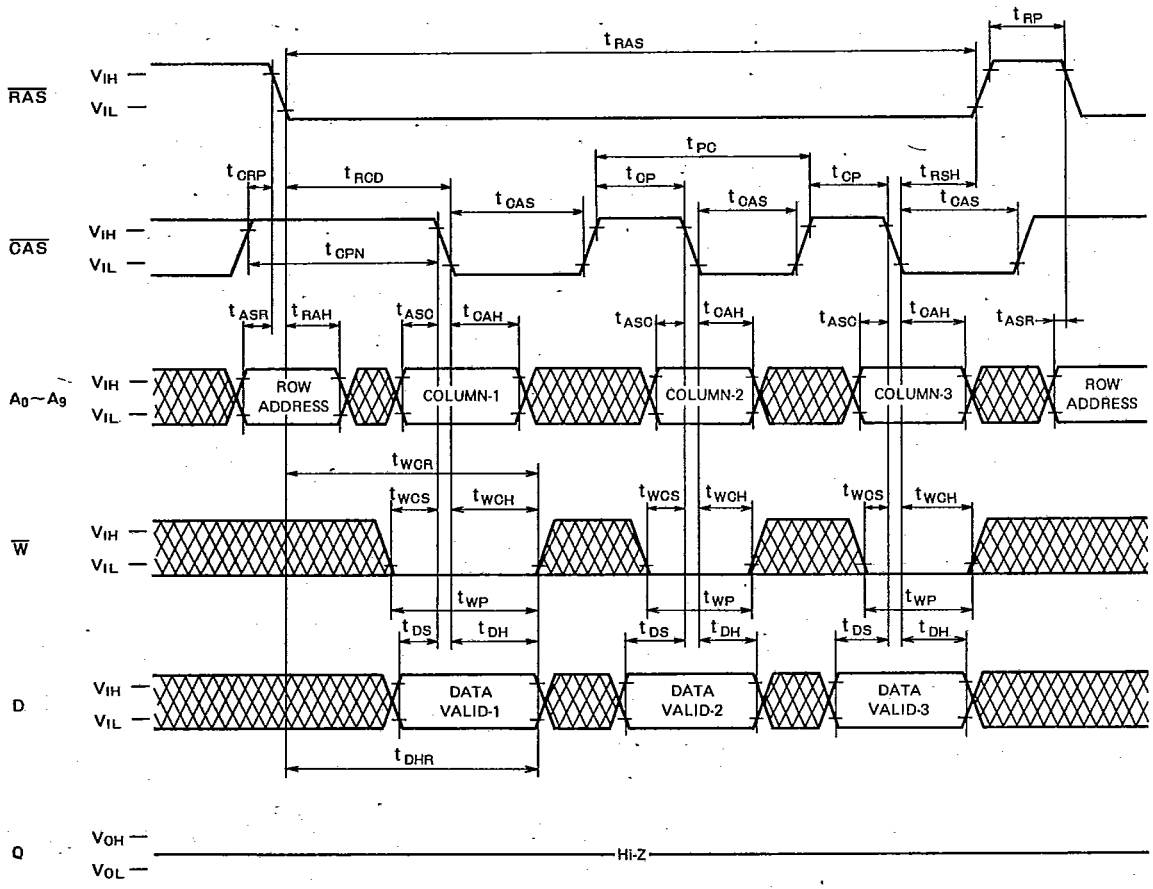


Fast-Page-Mode Read Cycle



T-46-23-15

Fast-Page-Mode Early Write Cycle



Fast-Page-Mode Read-Write, Read-Modify-Write Cycle