ADVANCE RELEASE

CIRRUS LOGIC®

CS5467

Four-channel Power/Energy IC

Features

- Energy Data Linearity: ±0.1% of Reading over 1000:1 Dynamic Range
- On-chip Functions:
  - Instantaneous Voltage, Current, and Power
  - I_{RMS} and V_{RMS}, Active, Reactive, and Apparent Power
  - Current Fault and Voltage Sag Detect
  - System Calibrations / Phase Compensation
  - Temperature Sensor
  - Energy-to-pulse Conversion
  - Positive-only Accumulation Mode
- Meets Accuracy Spec for IEC, ANSI, & JIS
- Low Power Consumption
- GND-referenced Signals with Single Supply
- On-chip, 2.5 V Reference
- Power Supply Monitor
- Simple Three-wire Digital Serial Interface
- "Auto-boot" Mode from Serial E^2PROM.
- Power Supply Configurations
  VA+ = +5 V; AGND = 0 V; VD+ = +3.3 V to +5 V

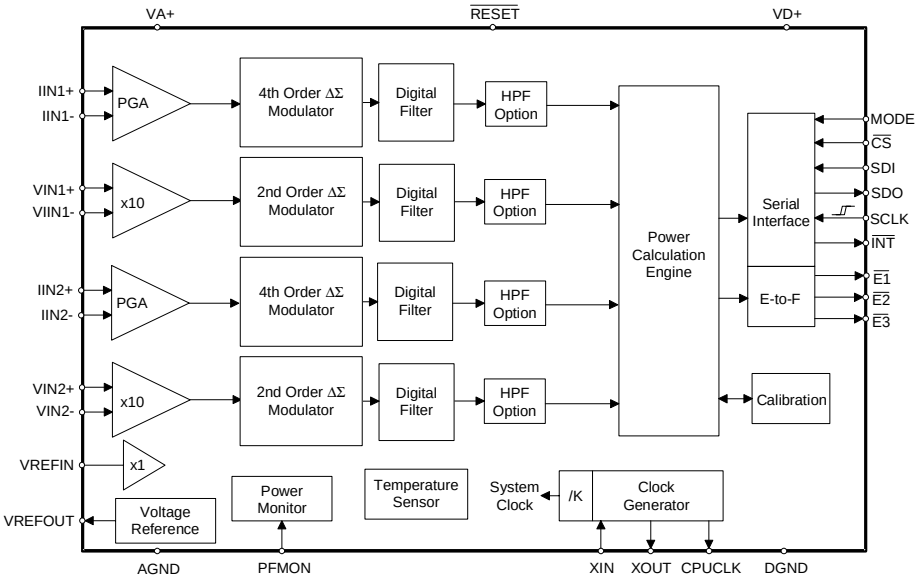
Description

The CS5467 is an integrated power measurement device which combines four ΔΣ analog-to-digital converters, power calculation engine, energy-to-frequency converter, and a serial interface on a single chip. It is designed to accurately measure instantaneous current and voltage and calculate V_{RMS}, I_{RMS}, instantaneous power, active power, apparent power, and reactive power for high-performance power measurement applications.

The CS5467 is optimized to interface to shunt resistors or current transformers for current measurement, and to resistive dividers or potential transformers for voltage measurement.

The CS5467 also features system-level calibration, a temperature sensor, voltage sag & current fault detection, and phase compensation.

ORDERING INFORMATION:
See Page 45.



Advance Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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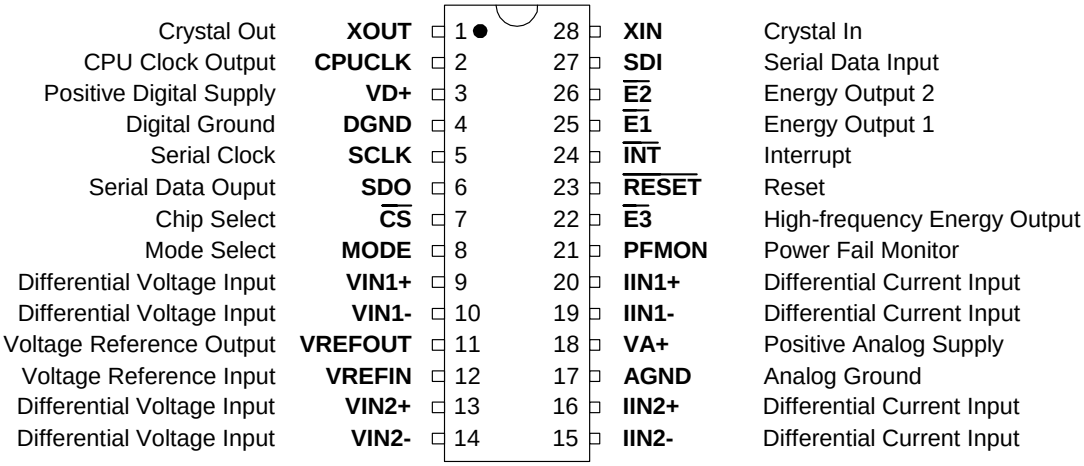
1. OVERVIEW

The CS5467 is a CMOS monolithic power measurement device with a computation engine and an energy-to-frequency pulse output. The CS5467 combines four ΔΣ analog-to-digital converters (ADCs), system calibration, and a computation engine on a single chip.

The CS5467 is designed for power measurement applications and is optimized to interface to a current-sense resistor or transformer for current measurement, and to a resistive divider or potential transformer for voltage measurement. The current channels provide programmable gains to accommodate various input levels from a multitude of sensing elements. With a single +5 V supply on VA+/AGND, the CS5467's four input channels can accommodate common mode plus signal levels between (AGND - 0.25 V) and VA+.

The CS5467 also is equipped with a computation engine that calculates instantaneous power, I_{RMS}, V_{RMS}, apparent power, active (real) power, reactive power, and power factor. Additional features of the CS5467 include line frequency monitoring, current and voltage sag detection, zero-cross detection, positive-only accumulation mode, and three programmable pulse output pins. To facilitate communication to a microprocessor, the CS5467 includes a simple three-wire serial interface which is SPI™ and Microwire™ compatible. The CS5467 provides three outputs for energy registration. Pins $\overline{E1}$, $\overline{E2}$, and $\overline{E3}$ are designed to interface to a microprocessor.

2. PIN DESCRIPTION



Clock Generator		
Crystal Out **Crystal In**	1,28	**XOUT, XIN** - The output and input of an inverting amplifier. Oscillation occurs when connected to a crystal, providing an on-chip system clock. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins and Serial Data I/O		
Serial Clock Input	5	**SCLK** - A Schmitt Trigger input pin. Clocks data from the SDI pin into the receive buffer and out of the transmit buffer onto the SDO pin when $\overline{CS}$ is low.
Serial Data Output	6	**SDO** -Serial port data output pin.SDO is forced into a high impedance state when $\overline{CS}$ is high.
Chip Select	7	**$\overline{CS}$** - Low, activates the serial port interface.
Mode Select	8	**MODE** - High, enables the “auto-boot” mode. The mode pin is pull-down by an internal resistor.
Energy Output	22, 25, 26	**$\overline{E3}$, $\overline{E1}$, $\overline{E2}$** - Active low pulses with an output frequency proportional to energy.
Reset	23	**$\overline{RESET}$** - A Schmitt Trigger input pin. Low activates Reset, all internal registers (some of which drive output pins) are set to their default states.
Interrupt	24	**$\overline{INT}$** - Low, indicates that an enabled event has occurred.
Serial Data Input	27	**SDI** - Serial port data input pin. Data will be input at a rate determined by SCLK.
Analog Inputs/Outputs		
Differential Voltage Inputs	9,10 13, 14	**VIN1+, VIN1-, VIN2+, VIN2-** - Differential analog input pins for the voltage channel.
Differential Current Inputs	19,20, 15,16	**IIN+, IIN-, IIN2+, IIN2-** - Differential analog input pins for the current channel.
Voltage Reference Output	11	**VREFOUT** - The on-chip voltage reference output. The voltage reference has a nominal magnitude of 2.5 V and is referenced to the AGND pin on the converter.
Voltage Reference Input	12	**VREFIN** - The input to this pin establishes the voltage reference for the on-chip modulator.
Power Supply Connections		
Positive Digital Supply	3	**VD**+ - The positive digital supply.
Digital Ground	4	**DGND** - Digital Ground.
Positive Analog Supply	18	**VA+** - The positive analog supply.
Analog Ground	17	**AGND** - Analog ground.
Power Fail Monitor	21	**PFMON** - The power fail monitor pin monitors the analog supply. If PFMON’s voltage threshold is tripped, a Low-Supply Detect (LSD) event is set in the status register.

3. CHARACTERISTICS & SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Digital Power Supply	VD+	3.135	5.0	5.25	V
Positive Analog Power Supply	VA+	4.75	5.0	5.25	V
Voltage Reference	VREFIN	-	2.5	-	V
Specified Temperature Range	T_A	-40	-	+85	°C

ANALOG CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 5 V ±5%; AGND = DGND = 0 V; VREFIN = +2.5 V. All voltages with respect to 0 V.
- MCLK = 4.096 MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy						
Active Power (Note 1)	All Gain Ranges Input Range 0.1% - 100%	P_{Active}	-	±0.1	-	%
Average Reactive Power (Note 1 and 2)	All Gain Ranges Input Range 0.1% - 100%	Q_{Avg}	-	±0.2	-	%
Power Factor (Note 1 and 2)	All Gain Ranges Input Range 1.0% - 100% Input Range 0.1% - 1.0%	PF	- -	±0.2 ±0.27	- -	% %
Current RMS (Note 1)	All Gain Ranges Input Range 1.0% - 100% Input Range 0.1% - 1.0%	I_{RMS}	- -	±0.1 ±0.17	- -	% % %
Voltage RMS (Note 1)	All Gain Ranges Input Range 5% - 100%	V_{RMS}	-	±0.1	-	%
Analog Inputs (All Channels)						
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Common Mode + Signal			-0.25	-	VA+	V
Analog Inputs (Current Channels)						
Differential Input Range [(IIN+) - (IIN-)]	(Gain = 10) (Gain = 50)	IIN	- -	500 100	- -	mV_{P-P} mV_{P-P}
Total Harmonic Distortion	(Gain = 50)	THD	80	94	-	dB
Crosstalk with Voltage Channel at Full Scale	(50, 60 Hz)		-	-115	-	dB
Input Capacitance		IC	-	27	-	pF
Effective Input Impedance		EII	30	-	-	kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_I	- -	- -	22.5 4.5	μV_{rms} μV_{rms}
Offset Drift (Without the High Pass Filter)		OD	-	4.0	-	µV/°C
Gain Error	(Note 3)	GE	-	±0.4		%

Notes: 1. Applies when the HPF option is enabled.

2. Applies when the line frequency is equal to the product of the Output Word Rate (OWR) and the value of epsilon (Ɛ).

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Analog Inputs (Voltage Channel)					
Differential Input Range [(VIN+) - (VIN-)]	VIN	-	500	-	mV_{P-P}
Total Harmonic Distortion	THD	65	75	-	dB
Crosstalk with Current Channel at Full Scale (50, 60 Hz)		-	-70	-	dB
Input Capacitance All Gain Ranges	IC	-	2.0	-	pF
Effective Input Impedance	EII	2	-	-	MΩ
Noise (Referred to Input)	N_V	-	-	140	μV_{rms}
Offset Drift (Without the High Pass Filter)	OD	-	16.0	-	µV/°C
Gain Error (Note 3)	GE	-	±3.0		%
Temperature Channel					
Temperature Accuracy	T	-	±5	-	°C
Power Supplies					
Power Supply Currents (Active State) I_{A+}	PSCA	-	1.3	-	mA
I_{D+} (VA+ = VD+ = 5 V)	PSCD	-	2.9	-	mA
I_{D+} (VA+ = 5 V, VD+ = 3.3 V)	PSCD	-	1.7	-	mA
Power Consumption Active State (VA+ = VD+ = 5 V)	PC	-	33	36	mW
(Note 4) Active State (VA+ = 5 V, VD+ = 3.3 V)		-	20	23	mW
Stand-by State		-	7	-	mW
Sleep State		-	10	-	uW
Power Supply Rejection Ratio (50, 60 Hz)					
(Note 5) Voltage Channel	PSRR	48	55	-	dB
Current Channel (Gain = 50x)		68	75	-	dB
Current Channel (Gain = 10x)		60	65	-	dB
PFMON Low-voltage Trigger Threshold (Note 6)	PMLO	2.3	2.45	-	V
PFMON High-voltage Power-on Trip Point (Note 7)	PMHI	-	2.55	2.7	V

Notes:

3. Applies before system calibration.
4. All outputs unloaded. All inputs CMOS level.
5. Measurement method for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV (zero-to-peak) (60 Hz) sinewave is imposed onto the +5 V DC supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to AGND. The CS5464 is then commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is (in dB):

$$PSRR = 20 \cdot \log\left[\frac{150}{V_{eq}}\right]$$

6. When voltage level on PFMON is sagging, and LSD bit = 0, the voltage at which LSD is set to 1.
7. If the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), this is the voltage level on PFMON at which the LSD bit can be permanently reset back to 0.

VOLTAGE REFERENCE

Parameter	Symbol	Min	Typ	Max	Unit
Reference Output					
Output Voltage	VREFOUT	+2.4	+2.5	+2.6	V
Temperature Coefficient (Note 8)	TC_{VREF}	-	25	60	ppm/°C
Load Regulation (Note 9)	ΔV_R	-	6	10	mV
Reference Input					
Input Voltage Range	VREFIN	+2.4	+2.5	+2.6	V
Input Capacitance		-	4	-	pF
Input CVF Current		-	100	-	nA

Notes: 8. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$TC_{VREF} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\left(\frac{1}{T_{AMAX} - T_{AMIN}}\right)\left(1.0 \times 10^{6}\right)$$

9. Specified at maximum recommended output of 1 µA, source or sink.

DIGITAL CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 5V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- MCLK = 4.096 MHz.

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Characteristics					
Master Clock Frequency Internal Gate Oscillator (Note 11)	MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle		40	-	60	%
CPUCLK Duty Cycle (Note 12 and 13)		40	-	60	%
Filter Characteristics					
Phase Compensation Range (Voltage Channel, 60 Hz)		-2.8	-	+2.8	°
Input Sampling Rate DCLK = MCLK/K		-	DCLK/8	-	Hz
Digital Filter Output Word Rate (Both Channels)	OWR	-	DCLK/1024	-	Hz
High-pass Filter Corner Frequency -3 dB		-	0.5	-	Hz
Full-scale DC Calibration Range (Referred to Input) (Note 14)	FSCR	25	-	100	%F.S.
Channel-to-channel Time-shift Error (Note 15)			1.0		µs
Input/Output Characteristics					
High-level Input Voltage All Pins Except XIN and SCLK and $\overline{RESET}$ XIN SCLK and $\overline{RESET}$	V_{IH}	 0.6 VD+ (VD+) - 0.5 0.8 VD+	 - - -	 - - -	 V V V
Low-level Input Voltage (VD = 5 V) All Pins Except XIN and SCLK and $\overline{RESET}$ XIN SCLK and $\overline{RESET}$	V_{IL}	 - - -	 - - -	 0.8 1.5 0.2 VD+	 V V V

Parameter	Symbol	Min	Typ	Max	Unit
Low-level Input Voltage (VD = 3.3 V) All Pins Except XIN and SCLK and $\overline{\text{RESET}}$ XIN SCLK and $\overline{\text{RESET}}$	V_{IL}	 - - -	 - - -	 0.48 0.3 0.2 VD+	 V V V
High-level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-level Output Voltage I_{out} = -5 mA (VD = +5V) I_{out} = -2.5 mA (VD = +3.3V)	V_{OL}	 - -	 - -	 0.4 0.4	 V V
Input Leakage Current (Note 16)	I_{in}	-	±1	±10	µA
3-state Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

Notes: 10. All measurements performed under static conditions.

11. If a crystal is used, XIN frequency must remain between 2.5 MHz - 5.0 MHz. If an external oscillator is used, XIN frequency range is 2.5 MHz - 20 MHz, but K must be set so that MCLK is between 2.5 MHz - 5.0 MHz.
12. If external MCLK is used, the duty cycle must be between 45% and 55% to maintain this specification.
13. The frequency of CPUCLK is equal to MCLK.
14. The minimum FSCR is limited by the maximum allowed gain register value. The maximum FSCR is limited by the full-scale signal applied to the channel input.
15. Configuration Register bits PC[6:0] are set to “0000000”.
16. The MODE pin is pulled low by an internal resistor.

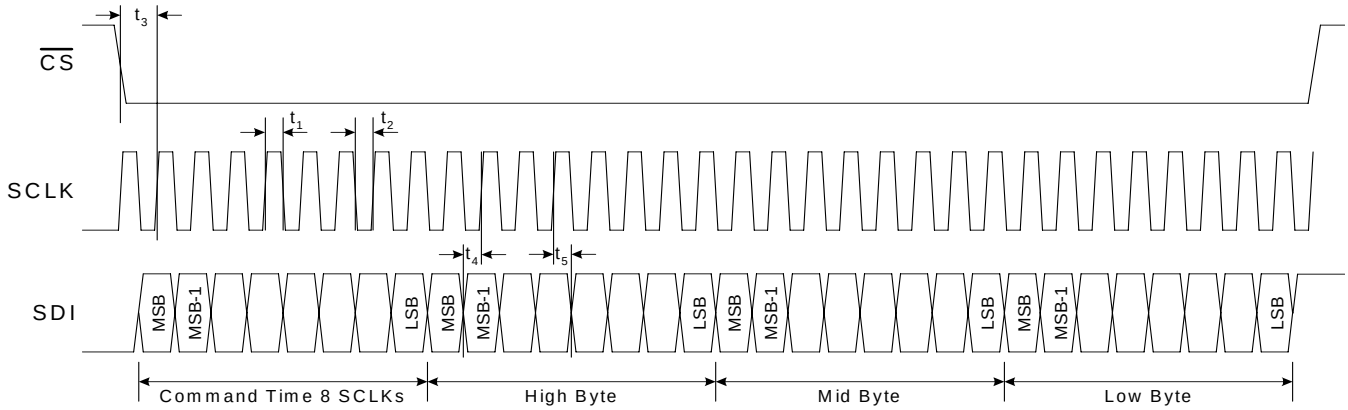
SWITCHING CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = 5 V ±5% VD+ = 3.3 V ±5% or 5 V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- Logic Levels: Logic 0 = 0 V, Logic 1 = VD+.

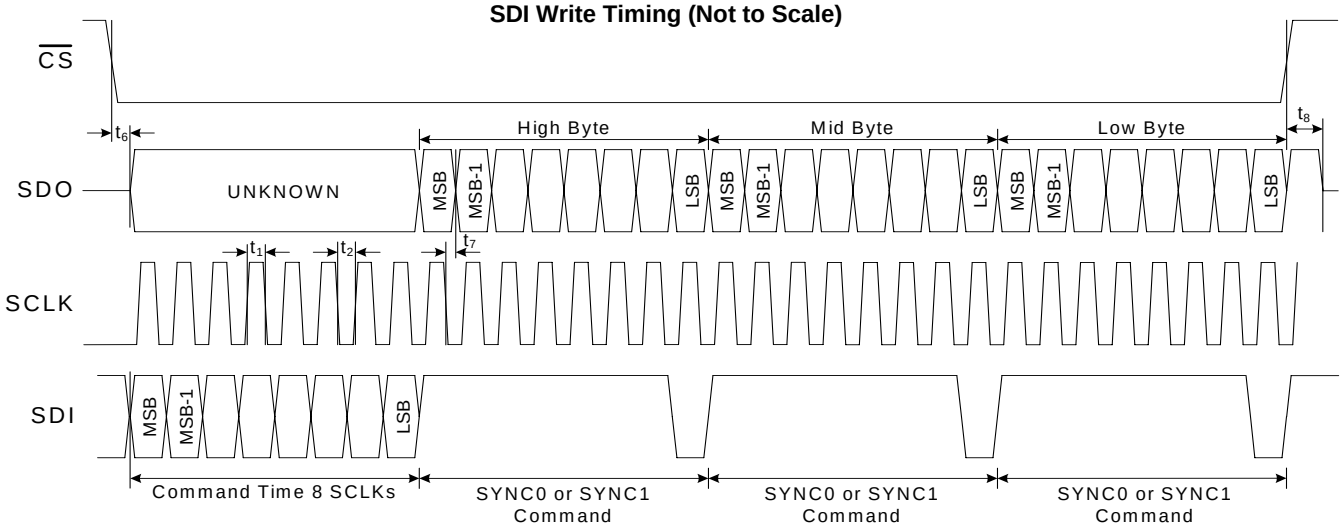
Parameter	Symbol	Min	Typ	Max	Unit
Rise Times (Note 17) Any Digital Output	t_{rise}	- -	- 50	1.0 -	µs ns
Fall Times (Note 17) Any Digital Output	t_{fall}	- -	- 50	1.0 -	µs ns
Start-up					
Oscillator Start-up Time XTAL = 4.096 MHz (Note 18)	t_{ost}	-	60	-	ms
Serial Port Timing					
Serial Clock Frequency	SCLK	-	-	2	MHz
Serial Clock Pulse Width High Pulse Width Low	t_1 t_2	200 200	- -	- -	ns ns
SDI Timing					
$\overline{CS}$ Falling to SCLK Rising	t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising	t_4	50	-	-	ns
Data Hold Time After SCLK Rising	t_5	100	-	-	ns
SDO Timing					
$\overline{CS}$ Falling to SDO Driving	t_6	-	20	50	ns
SCLK Falling to New Data Bit (hold time)	t_7	-	20	50	ns
$\overline{CS}$ Rising to SDO Hi-Z	t_8	-	20	50	ns
Auto-Boot Timing					
Serial Clock Pulse Width Low Pulse Width High	t_9 t_{10}		8 8		MCLK MCLK
MODE setup time to $\overline{RESET}$ Rising	t_{11}	50			ns
$\overline{RESET}$ rising to $\overline{CS}$ falling	t_{12}	48			MCLK
$\overline{CS}$ falling to SCLK rising	t_{13}	100	8		MCLK
SCLK falling to $\overline{CS}$ rising	t_{14}		16		MCLK
$\overline{CS}$ rising to driving MODE low (to end auto-boot sequence)	t_{15}	50			ns
SDO guaranteed setup time to SCLK rising	t_{16}	100			ns

Notes: 17. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

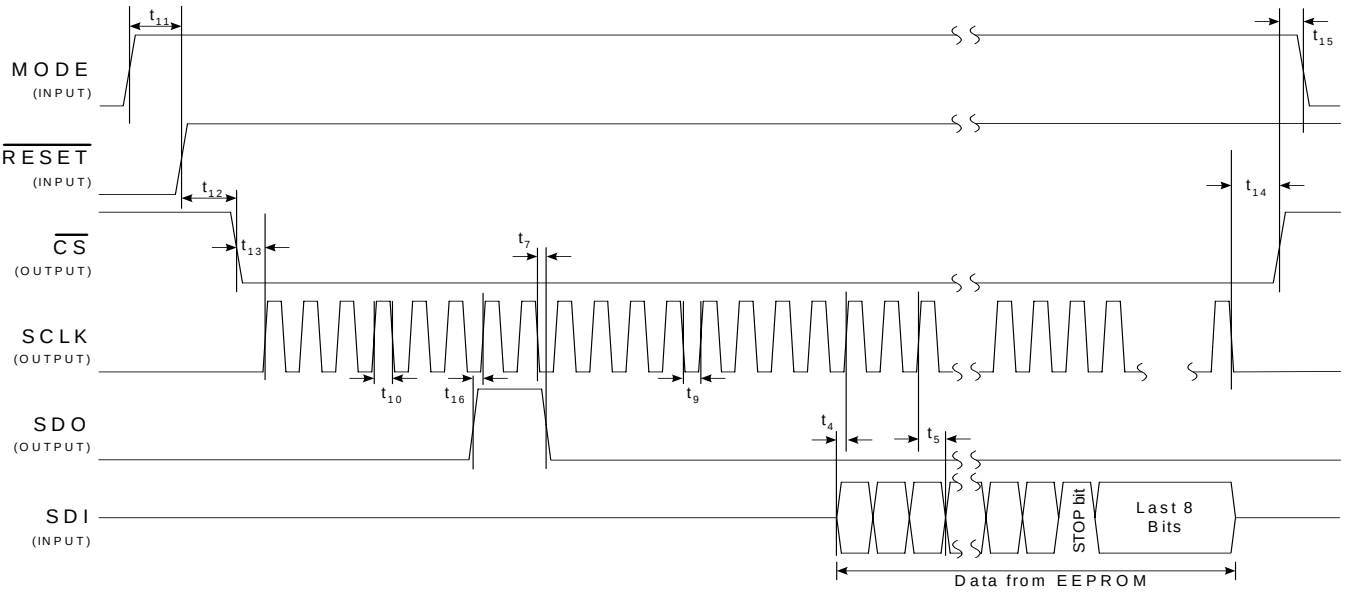
18. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.



SDI Write Timing (Not to Scale)



SDO Read Timing (Not to Scale)



Auto-boot Sequence Timing (Not to Scale)

Figure 1. CS5464 Read and Write Timing Diagrams

SWITCHING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{E1}$, $\overline{E2}$, and $\overline{E3}$ Timing (Note 19 and 20)					
Period	t_{period}	250	-	-	µs
Pulse Width	t_{pw}	244	-	-	µs
Rising Edge to Falling Edge	t_3	6	-	-	µs
$\overline{E2}$ Setup to $\overline{E1}$ and/or $\overline{E3}$ Falling Edge	t_4	1.5	-	-	µs
$\overline{E1}$ Falling Edge to $\overline{E3}$ Falling Edge	t_5	248	-	-	µs

Notes: 19. Pulse output timing is specified at MCLK = 4.096 MHz, E2MODE = 0, and E3MODE[1:0] = 0. Refer to 5.5 *Energy Pulse Output* on page 18 for more information on pulse output pins.

20. Timing is proportional to the frequency of MCLK.

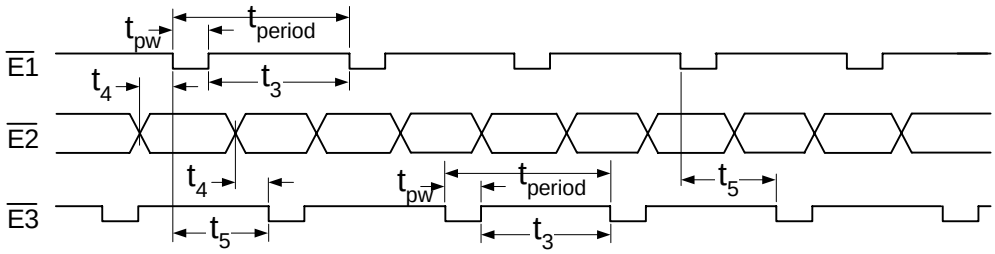


Figure 2. Timing Diagram for $\overline{E1}$, $\overline{E2}$, and $\overline{E3}$

ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 21 and 22)					
	Positive Digital	VD+	-0.3	-	+6.0	V
	Positive Analog	VA+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies	(Notes 23, 24, 25)	I_{IN}	-	-	±10	mA
Output Current, Any Pin Except VREFOUT		I_{OUT}	-	-	100	mA
Power Dissipation	(Note 26)	P_D	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	- 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 21. VA+ and AGND must satisfy [(VA+) - (AGND)] ≤ + 6.0 V.

22. VD+ and AGND must satisfy [(VD+) - (AGND)] ≤ + 6.0 V.

23. Applies to all pins including continuous over-voltage conditions at the analog input pins.

24. Transient current of up to 100 mA will not cause SCR latch-up.

25. Maximum DC input current for a power supply pin is ±50 mA.

26. Total power dissipation, including all input currents and output currents.

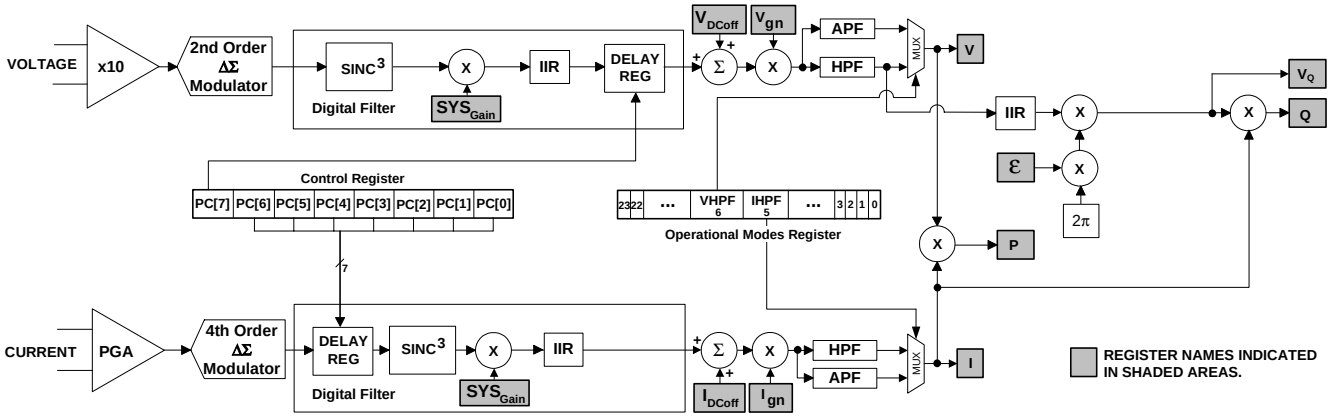


Figure 3. Data Measurement Flow Diagram

4. THEORY OF OPERATION

The CS5467 is a four-channel analog-to-digital converter (ADC) followed by a computation engine that performs power calculations and energy-to-pulse conversion. The data flow for the voltage and current channel measurement and the power calculation algorithms are depicted in Figures 3, 4, and 5.

The CS5467 analog inputs are structured with two *Current* channels and two *Voltage* channels, and are optimized to simplify interfacing to various sensing elements. As shown in Figures 3 and 4, the current and voltage channels are fully independent.

The voltage-sensing elements introduces a voltage waveform on the two voltage channel inputs VIN± and VIN2±, which is subject to a gain of 10x. A second-order delta-sigma modulator samples the amplified signal for digitization.

Simultaneously, the current-sensing elements introduce a voltage waveform on the two current channel inputs IIN± and IIN2±, which is subject to the two selectable gains of the programmable gain amplifier (PGA). The amplified signals are sampled by a fourth-order delta-sigma modulator for digitization. The converters sample at a rate of MCLK/8. The over-sampling provides a wide dynamic range and simplified anti-alias filter design.

4.1 Digital Filters

The decimating digital filters on the four channels are Sinc^3 filters followed by 3rd-order IIR filters. The single-bit data is passed to the low-pass decimation filter and output at a fixed word rate. The output word is passed to an IIR filter to compensate for the magnitude roll off of the low-pass filtering operation.

An optional digital high-pass filter (*HPF* in Figures 3 and 4) removes any DC component from the selected signal path. By removing the DC component from the voltage and/or the current channel, any DC content will also be removed from the calculated active power as well. With both HPFs enabled the DC component will be removed

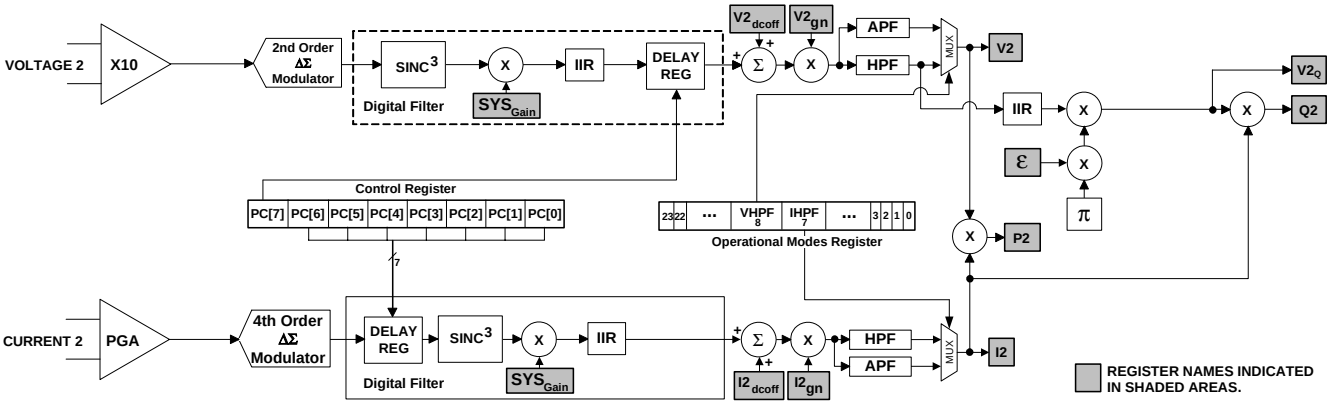


Figure 4. Data Measurement Flow Diagram

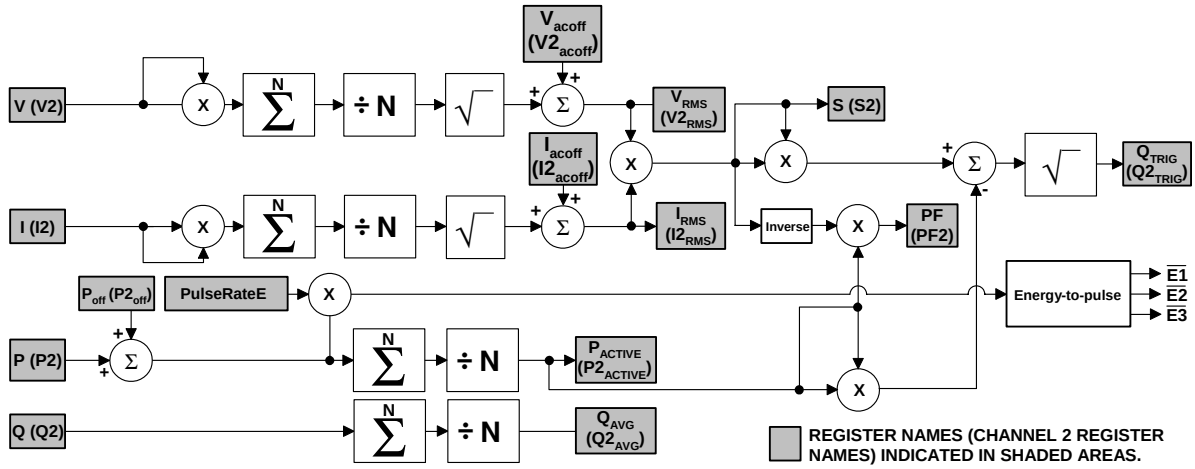


Figure 5. Power Calculation Flow

from the calculated V_{RMS} and I_{RMS}, as well as the apparent power.

When the optional HPF in either channel is disabled, an all-pass filter (APF) in the complementary channel is implemented. The APF has an amplitude response that is flat within the channel bandwidth and is used for matching phase in systems where only one channel's HPF is engaged.

4.2 Voltage and Current Measurements

The digital filter output word is subject to a DC-offset adjustment and a gain calibration (See Section 7. *System Calibration* on page 39). The calibrated measurement is available by reading the instantaneous voltage and current registers.

The Root Mean Square (*RMS* in Figure 5) calculations are performed on N instantaneous voltage and current samples, V_n and I_n, respectively (where N is the cycle count), using the formula:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} I_n}{N}}$$

and likewise for V_{RMS}, using V_n. I_{RMS} and V_{RMS} are accessible by register reads, which are updated once every cycle count (referred to as a computational cycle).

4.3 Power Measurements

The instantaneous voltage and current samples are multiplied to obtain the instantaneous power (see Figure 3 and 4). The product is then averaged over N conversions to compute active power. The average active power measured on channels 1 and 2 is used to drive energy pulse output $\overline{E1}$. Energy output $\overline{E2}$ is configurable and can provide an energy sign or a pulse output that is proportional to the average apparent power measured on channels 1 and 2. Energy output $\overline{E3}$ provides a pulse output that is proportional to the average reactive power or the average apparent power measured on channels 1 and 2. Output $\overline{E3}$ can also be set to indicate the PFMON comparator output or to indicate the sign of the voltage applied to the voltage channel.

The apparent power (S, S2) is the combination of the active power and reactive power, without reference to an impedance phase angle, and is calculated by the CS5467 using the following formula:

$$S = V_{RMS} \times I_{RMS}$$

Power Factor (PF, PF2) is the active power (P_{Active}, $P2_{Active}$) divided by the apparent power (S, S2)

$$PF = \frac{P_{Active}}{S}$$

The sign of the power factor is determined by the active power.

The CS5467 calculates the reactive power (Q_{Trig}, $Q2_{Trig}$) utilizing trigonometric identities, using the formula

$$Q_{Trig} = \sqrt{S^2 - P^2_{Active}}$$

The average reactive power calculation (Q_{Avg}, $Q2_{Avg}$) is generated by averaging the voltage and multiplying that value by the current measurement with a 90° phase difference between the two. The 90° phase shift is realized by applying an IIR digital filter in the voltage channel to obtain quadrature voltage (see Figure 3 and 4). This filter will give exactly -90° phase shift across all frequencies, and utilizes epsilon (Ɛ) to achieve unity gain at the line frequency.

The instantaneous quadrature voltage (V_Q, $V2_Q$) and current (I, I2) samples are multiplied to obtain the instantaneous quadrature power (Q, Q2). The product is then averaged over N conversions, utilizing the formula

$$Q_{Avg} = \frac{\sum_{n=1}^{N} Q_n}{N}$$

The peak current (I_{peak}, $I2_{peak}$) and peak voltage (V_{peak}, $V2_{peak}$) are the instantaneous current and voltage, respectively, with the greatest magnitude detected during the previous computation cycle. Active, apparent, reactive, and fundamental power are updated every computation cycle.

4.4 Linearity Performance

The linearity of the V_{RMS}, I_{RMS}, active, reactive, and power-factor power measurements (before calibration) will be within ±0.1% of reading over the ranges specified, with respect to the input voltage levels required to cause full-scale readings in the I_{RMS} and V_{RMS} registers. Refer to *Accuracy Specifications* on page 7.

Until the CS5467 is calibrated, the *accuracy* of the CS5467 (with respect to a reference line-voltage and line-current level on the power mains) is not guaranteed

5. FUNCTIONAL DESCRIPTION

5.1 Analog Inputs

The CS5467 is equipped with four fully differential input channels. The inputs VIN±, VIN2±, IIN±, and IIN2± are designated as the voltage, voltage 2, current, and current 2 channel inputs, respectively. The full-scale differential input voltage for the current and voltage channel is ±250 mV_P.

5.1.1 Voltage Channel Input

The output of the line voltage resistive divider or transformer is connected to the VIN+ (VIN2+) and VIN- (VIN2-) input pins of the CS5467. The voltage channels are equipped with a 10x fixed-gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±250 mV. If the input signal is a sine wave, the maximum RMS voltage at a gain 10x is:

$$\frac{250mV_P}{\sqrt{2}} \cong 176.78mV_{RMS}$$

which is approximately 70.7% of maximum peak voltage. The voltage channel is also equipped with a *Voltage Gain Register*, allowing for an additional programmable gain of up to 4x.

5.1.2 Current Channel Inputs

The output of the current-sense resistor or transformer is connected to the IIN+ (IIN2+) and IIN- (IIN2-) input pins of the CS5467. To accommodate different current-sensing elements, the current channel incorporates a programmable gain amplifier (PGA) with two programmable input gains. *Configuration Register* bit Igain (I2gain) defines the two gain selections and corresponding maximum input signal level.

Igain, I2gain	Maximum Input	Gain
0	±250 mV	10x
1	±50 mV	50x

Table 1. Current Channel PGA Setting

For example, if Igain=0 (I2gain=0), current channel 1(2) PGA gain is set to 10x. If the input signals are pure sinusoids with zero phase shift, the maximum peak differential signal on the current or voltage channel is ±250 mV_P. The input signal levels are approximately 70.7% of maximum peak voltage and produce a full-scale energy pulse registration equal to 50% of absolute maximum energy registration. This will be discussed further in See Section 5.5 *Energy Pulse Output* on page 18.

The *Current Gain Register* also facilitates an additional programmable gain of up to 4x. If an additional gain is applied to the voltage and/or current channel, the maximum input range should be adjusted accordingly.

5.2 IIR Filters

The current and voltage channels are equipped with a 3rd-order IIR filter, that is used to compensate for the magnitude roll off of the low-pass decimation filter.

5.3 High-pass Filters

By removing the offset from either channel, no error component will be generated at DC when computing the active power. By removing the offset from both channels, no error component will be generated at DC when computing V_{RMS}, I_{RMS}, and apparent power. *Operational Mode Register* bits VHPF, VHPF2, IHPF and IHPF2 activate the HPF in the voltage and current channel, respectively. When a high-pass filter is active in only one channel, an all-pass filter (APF) is applied to the companion channel. The APF has an amplitude response that is flat within the channel bandwidth and is used for matching phase in systems where only one HPF is engaged.

5.4 Performing Measurements

The CS5467 performs measurements of instantaneous voltage (V_n) and current (I_n), and calculates instantaneous power (P_n) at an output word rate (OWR) of

$$OWR = \frac{(MCLK/K)}{1024}$$

where K is the value of the clock divider selected in the *Configuration Register* by bits K[3:0]. Note that a value of K[3:0] = 0000 results in a clock divider setting of 16, rather than zero.

The RMS voltage (V_{RMS}, $V2_{RMS}$), RMS current (I_{RMS}, $I2_{RMS}$), and active power (P_{active}, $P2_{active}$) are computed using N instantaneous samples of V_n, I_n, and P_n respectively, where N is the value in the *Cycle Count Register* and is referred to as a "*computation cycle*". The apparent power (S, S2) is the product of V_{RMS} and I_{RMS}. A computation cycle is derived from the master clock (MCLK), with frequency: Under default conditions and

$$\text{Computation Cycle} = \frac{OWR}{N}$$

with K = 1, N = 4000, and MCLK = 4.096 MHz – the OWR = 4000 and the Computation Cycle = 1 Hz.

All measurements are available as a percentage of full scale. The format for *signed* registers is a two's complement, normalized value between -1 and +1. The format for *unsigned* registers is a normalized value between 0 and 1. A register value of

$$\frac{(2^{23}-1)}{2^{23}} = 0.99999988$$

represents the maximum possible value.

At each instantaneous measurement, the CRDY bit will be set in the *Status Register*, and the $\overline{INT}$ pin will become active if the CRDY bit is unmasked in the *Mask Register*. At the end of each computation cycle, the DRDY bit will be set in the *Status Register*, and the $\overline{INT}$ pin will become active if the DRDY bit is unmasked in the *Mask Register*. When these bits are asserted, they must be cleared before they can be asserted again.

If the *Cycle Count Register* (N) is set to 1, all output calculations are instantaneous, and DRDY, like CRDY, will indicate when instantaneous measurements are finished. Some calculations are inhibited when the cycle count is less than 2.

Epsilon (ε) is the ratio of the input line frequency (f_i) to the sample frequency (f_s) of the ADC.

$$\varepsilon = f_i / f_s$$

where f_s = MCLK / (K x 1024). With MCLK = 4.096 MHz and clock divider K = 1, f_s = 4000 Hz. For the two most-common line frequencies, 50 Hz and 60 Hz

$$\varepsilon = 50\ Hz / 4000\ Hz = 0.0125$$

and

$$\varepsilon = 60\ Hz / 4000\ Hz = 0.015$$

respectively. Epsilon is used to set the gain of the 90° phase shift (IIR) filter for the average reactive power calculation.

5.5 Energy Pulse Output

The CS5467 provides three output pins for energy registration. By default, $\overline{E1}$ is used to register average active energy measured on channels 1 and 2, $\overline{E3}$ is used to register average reactive energy measured on channels 1 and 2, and $\overline{E2}$ indicates the sign of both active and reactive energy. (See Figure 2. *Timing Diagram for E1, E2, and E3* on page 13.)

The $\overline{E1}$ pulse output is designed to indicate the average active energy measured on channels 1 and 2. The $\overline{E2}$ pin can be used to register average apparent energy measured on channels 1 and 2 or to indicate the sign of energy. Table 2 defines the pulse output mode, which is controlled by bit E2MODE in the *Operational Mode Register.*

E2MODE	$\overline{E2}$ Output Mode
0	Sign of Energy
1	Apparent Energy

Table 2. $\overline{E2}$ Pin Configuration

The $\overline{E3}$ pin can be set to register average reactive energy measured on channels 1 and 2 (default), PFMON, voltage channel sign, or average apparent energy measured on channels 1 and 2. Table 3 defines the pulse output format, which is controlled by bits E3MODE[1:0] in the *Operational Mode Register.*

E3MODE1	E3MODE0	$\overline{E3}$ OutPut Mode
0	0	Reactive Energy
0	1	PFMON
1	0	Voltage Channel Sign
1	1	Apparent Energy

Table 3. $\overline{E3}$ Pin Configuration

The pulse output frequencies of $\overline{E1}$, $\overline{E2}$, and $\overline{E3}$ are directly proportional to the power calculated from the input signals. The value contained in the *PulseRateE Register* is the ratio of the frequency of energy-output pulses to the number of samples, at full scale, which defines the average frequency for the output pulses. The pulse width, t_{pw} in Figure 2, is an integer multiple of MCLK cycles approximately equal to:

$$t_{pw}(sec) \cong \frac{1}{(MCLK/K)/1024}$$

If MCLK = 4.096 MHz and K = 1 then $t_{pw} \cong 0.25$ ms.

5.5.1 Active Energy

The $\overline{E1}$ pin produces active-low pulses with an output frequency proportional to the average active power measured on channels 1 and 2. The $\overline{E2}$ pin is the energy direction indicator. Positive energy is represented by $\overline{E1}$ pin falling while the $\overline{E2}$ is high. Negative energy is represented by the $\overline{E1}$ pin falling while the $\overline{E2}$ is low. The $\overline{E1}$ and $\overline{E2}$ switching characteristics are specified in Figure 2. *Timing Diagram for E1, E2, and E3* on page 13.

Figure 6 illustrates the pulse output format with positive active energy and negative reactive energy.

Figure 6. Active and Reactive energy pulse outputs

The pulse output frequency of $\overline{E1}$ is directly proportional to the active power calculated from the input signals. To calculate the output frequency of $\overline{E1}$, the following transfer function can be utilized:

$$FREQ_P = [(P_{Active} + P2_{Active})/2] \times PulseRate$$

where

$$P(2)_{Active} = \frac{VIN(2) \times V(2)gain \times IIN(2) \times I(2)gain \times PF(2)}{VREFIN^2}$$

$FREQ_P$ = Average frequency of active energy $\overline{E1}$ pulses [Hz]
VIN(2) = rms voltage across VIN(2)+ and VIN(2)- [V]
V(2)gain = Voltage channel gain
IIN(2) = rms voltage across IIN(2)+ and IIN(2)- [V]
I(2)gain = Current channel gain
PF(2) = Power Factor
PulseRate = PulseRateE x (MCLK/K)/2048 [Hz]
VREFIN = Voltage at VREFIN pin [V]

With MCLK = 4.096 MHz, PF = 1, and default settings, the pulses will have an average frequency equal to the frequency specified by *PulseRateE* when the input signals applied to the voltage and current channels cause full-scale readings in the instantaneous voltage and current registers. The maximum pulse frequency from the $\overline{E1}$ pin is (MCLK/K)/2048.

5.5.2 Apparent Energy Mode

Pin $\overline{E2}$ outputs apparent energy pulses when the *Operational Mode Register* bit E2MODE = 1. Pin $\overline{E3}$ outputs apparent energy pulses when the *Operational Mode Register* bits E3MODE[1:0] = 3 (11b). Figure 7 illustrates the pulse output format with apparent energy on $\overline{E2}$ (E2MODE = 1 and E3MODE[1:0] = 0)

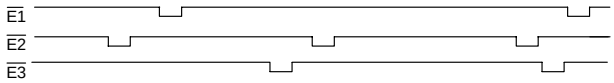


Figure 7. Apparent energy pulse outputs

The pulse output frequency of $\overline{E2}$ (and/or $\overline{E3}$) is directly proportional to the apparent power calculated from the input signals. Since apparent power is without reference to an impedance phase angle, the following transfer function can be utilized to calculate the output frequency on $\overline{E2}$ (and/or $\overline{E3}$).

$$FREQ_S = [(S + S2)/2] \times PulseRate$$

where

$$S(2) = \frac{VIN(2) \times V(2)gain \times IIN(2) \times I(2)gain}{VREFIN^2}$$

$FREQ_S$ = Average frequency of apparent energy $\overline{E2}$ and/or $\overline{E3}$ pulses [Hz]
VIN(2) = rms voltage across VIN(2)+ and VIN(2)- [V]
V(2)gain = Voltage channel gain
IIN(2) = rms voltage across IIN(2)+ and IIN(2)- [V]
I(2)gain = Current channel gain
PulseRate = PulseRateE x (MCLK/K)/2048 [Hz]
VREFIN = Voltage at VREFIN pin [V]

With MCLK = 4.096 MHz and default settings, the pulses will have an average frequency equal to the frequency specified by *PulseRateE* when the input signals applied to the voltage and current channels cause full-scale readings in the instantaneous voltage and current registers. The maximum pulse frequency from the $\overline{E2}$ (and/or $\overline{E3}$) pin is (MCLK/K)/2048. The $\overline{E2}$ (and/or $\overline{E3}$) pin outputs apparent energy, but has no energy direction indicator.

5.5.3 Reactive Energy Mode

Reactive energy pulses are output on pin $\overline{E3}$ by setting bit E3MODE[1:0] = 0 (default) in the *Operational Mode Register*. Positive reactive energy is registered by $\overline{E3}$ falling when $\overline{E2}$ is high. Negative reactive energy is registered by $\overline{E3}$ falling when $\overline{E2}$ is low. Figure 6 on page 19 illustrates the pulse output format with negative reactive energy output on pin $\overline{E3}$ and the sign of the energy on $\overline{E2}$. The $\overline{E3}$ and $\overline{E2}$ pulse output switching characteristics are specified in Figure 2 on page 13.

The pulse output frequency of $\overline{E3}$ is directly proportional to the reactive power calculated from the input signals. To calculate the output frequency on $\overline{E3}$, the following transfer function can be utilized:

$$FREQ_Q = [(Q_{Avg} + Q2_{Avg})/2] \times PulseRate$$

where

$$Q(2)_{Avg} = \frac{VIN(2) \times V(2)gain \times IIN(2) \times I(2)gain \times PQ(2)}{VREFIN^2}$$

$FREQ_Q$ = Average frequency of reactive energy $\overline{E3}$ pulses [Hz]
VIN(2) = rms voltage across VIN(2)+ and VIN(2)- [V]
V(2)gain = Voltage channel gain
IIN(2) = rms voltage across IIN(2)+ and IIN(2)- [V]
I(2)gain = Current channel gain
$PQ = \sqrt{1 - PF^2}$
PulseRate = PulseRateE x (MCLK/K)/2048 [Hz]
VREFIN = Voltage at VREFIN pin [V]

With MCLK = 4.096 MHz, PF = 0 and default settings, the pulses will have an average frequency equal to the frequency specified by *PulseRateE* when the input signals applied to the voltage and current channels cause full-scale readings in the instantaneous voltage and cur-

rent registers. The maximum pulse frequency from the $\overline{E1}$ pin is (MCLK/K)/2048.

5.5.4 Voltage Channel Sign Mode

Setting bits E3MODE[1:0] = 2 (10b) in the *Operational Mode Register* outputs the sign of the voltage channel on pin $\overline{E3}$. Figure 8 illustrates the output format with voltage channel sign on $\overline{E3}$

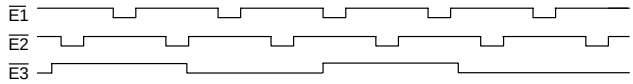


Figure 8. Voltage Channel Sign Pulse outputs

Output pin $\overline{E3}$ is high when the line voltage is positive and pin $\overline{E3}$ is low when the line voltage is negative.

5.5.5 PFMON Output Mode

Setting bit E3MODE[1:0] = 1 (01b) in the *Operational Mode Register* outputs the state of the PFMON comparator on pin $\overline{E3}$. Figure 9 illustrates the output format with PFMON on $\overline{E3}$

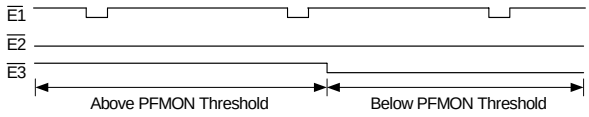


Figure 9. PFMON output to pin $\overline{E3}$

When PFMON is greater than the threshold, pin $\overline{E3}$ is high and when PFMON is less than the threshold pin $\overline{E3}$ is low.

5.6 Sag and Fault Detect Feature

Status bit VSAG (V2SAG) and IFAULT (I2FAULT) in the *Status Register,* indicates a sag occurred in the power line voltage (voltage 2) and current (current 2), respectively. For a sag condition to be identified, the absolute value of the instantaneous voltage or current must be less than the sag level for more than half of the sag duration (see Figure 10).

To activate voltage sag detection, a voltage sag level must be specified in the *Voltage Sag Level Register* ($VSAG_{level}$, $V2SAG_{level}$), and a voltage sag duration must be specified in the *Voltage Sag Duration Register* ($VSAG_{duration}$, $V2SAG_{duration}$). To activate current fault detection, a current sag level must be specified in the *Current Fault Level Register* ($ISAG_{level}$, $I2SAG_{level}$), and a current sag duration must be specified in the *Current Fault Duration Register* ($ISAG_{duration}$, $I2SAG_{duration}$). The voltage and current sag levels are specified as the average of the absolute instantaneous voltage and current, respectively. Voltage and current sag duration is specified in terms of ADC cycles.

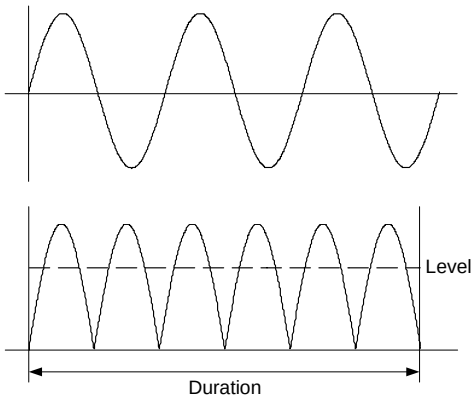


Figure 10. Sag and Fault Detect

5.7 On-chip Temperature Sensor

The on-chip temperature sensor is designed to assist in characterizing the measurement element over a desired temperature range. Once a temperature characterization is performed, the temperature sensor can be utilized to assist in compensating for temperature drift.

Temperature measurements are performed when a one is written to the *Temperature Measurement* (T_{meas}) register and stored in the *Temperature Register*. The *Temperature Register* (T) default is Celsius scale (°C). The *Temperature Gain Register* (T_{gain}) and *Temperature Offset Register* (T_{off}) are constant values allowing for temperature scale conversions.

The temperature update rate is a function of the number of ADC samples. With MCLK = 4.096 MHz and K = 1 the update rate is:

$$\frac{2240 \text{ samples}}{(MCLK/K)/1024} = 0.56 \text{ sec}$$

The *Cycle Count Register* (N) must be set to a value greater than one. Status bit TUP in the *Status Register,* indicates when the *Temperature Register* is updated.

The *Temperature Offset Register* sets the zero-degree measurement. To improve temperature measurement accuracy, the zero-degree offset may need to be adjusted after the CS5467 is initialized. Temperature-offset calibration is achieved by adjusting the *Temperature Offset Register* (T_{off}) by the differential temperature (ΔT) measured from a calibrated digital thermometer and the CS5467 temperature sensor. A one-degree adjustment to the *Temperature Register* (T) is achieved by

adding 2.737649x10^{-4} to the *Temperature Offset Register* (T_{off}). Therefore,

$$T_{off} = T_{off} + (\Delta T \times 2.737649 \cdot 10^{-4})$$

if T_{off} = -0.094488 and ΔT = -2.0 (°C), then

$$T_{off} = (-0.094488 + (-2.0 \times 2.737649 \cdot 10^{-4})) = -0.09504$$

or 0xF3D5BB (2's compliment notation) is stored in the *Temperature Offset Register* (T_{off}).

To convert the *Temperature Register* (T) from a Celsius scale (°C) to a Fahrenheit scale (°F) utilize the formula

$$^{o}F = \frac{9}{5}(^{o}C + 17.7778)$$

Applying the above relationship to the CS5461A temperature measurement algorithm

$$T\langle^{o}F\rangle = \left(\frac{9}{5} \times T_{gain}\right)\left[T\langle^{o}C\rangle + \left(T_{off} + (17.7778 \times 2.737649 \cdot 10^{-4})\right)\right]$$

If T_{off} = -0.09504 and T_{gain} = 26.443 for a Celsius scale, the modified values are T_{off} = -0.09017 (0xF47550) and T_{gain} = 47.6 (0x5F3333) for a Fahrenheit scale.

5.8 Voltage Reference

The CS5467 is specified for operation with a +2.5 V reference between the VREFIN and AGND pins. To utilize the on-chip 2.5 V reference, connect the VREFOUT pin to the VREFIN pin of the device. The VREFIN can be used to connect external filtering and/or references.

5.9 System Initialization

Upon powering up, the digital circuitry is held in reset until the analog voltage reaches 4.0 V. At that time, an eight-XIN-clock-period delay is enabled to allow the oscillator to stabilize. The CS5467 will then initialize.

A hardware reset is initiated when the $\overline{\text{RESET}}$ pin is asserted with a minimum pulse width of 50 ns. The $\overline{\text{RESET}}$ signal is asynchronous, with a Schmitt-trigger input. Once the $\overline{\text{RESET}}$ pin is de-asserted, an eight-XIN-clock-period delay is enabled.

A software reset is initiated by writing the command 0x80. After a hardware or software reset, the internal registers (some of which drive output pins) will be reset to their default values. Status bit DRDY in the *Status Register,* indicates the CS5467 is in its *active* state and ready to receive commands.

5.10 Power-down States

The CS5467 has two power-down states, *Stand-by* and *Sleep*. In the stand-by state all circuitry except the voltage reference and crystal oscillator is turned off. To return the device to the active state, a power-up command is sent to the device.

In Sleep state, all circuitry except the instruction decoder is turned off. When the power-up command is sent to the device, a system initialization is performed (See Section 5.9 *System Initialization* on page 21).

5.11 Oscillator Characteristics

XIN and XOUT are the input and output of an inverting amplifier configured as an on-chip oscillator, as shown in Figure 11. The oscillator circuit is designed to work with a quartz crystal. To reduce circuit cost, two load capacitors C1 and C2 are integrated in the device, from XIN to DGND, and XOUT to DGND. PCB trace lengths should be minimized to reduce stray capacitance. To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS level signals. This amplifier works with sinusoidal inputs so there are no problems with slow edge times.

The CS5467 can be driven by an external oscillator ranging from 2.5 to 20 MHz, but the K divider value must be set such that the internal MCLK will run somewhere between 2.5 MHz and 5 MHz. The K divider value is set with the K[3:0] bits in the *Configuration Register*. As an example, if XIN = MCLK = 15 MHz, and K is set to 5, DCLK will equal 3 MHz, which is a valid value for DCLK.

5.12 Event Handler

The $\overline{\text{INT}}$ pin is used to indicate that an internal error or event has taken place in the CS5467. Writing a logic 1

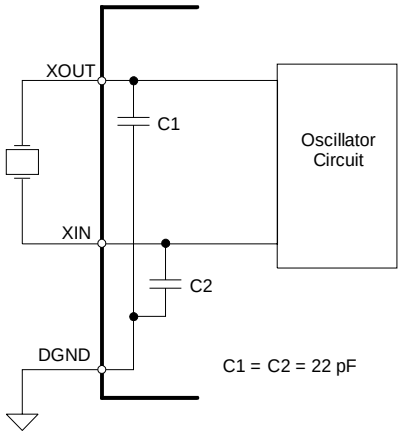


Figure 11. Oscillator Connection

to any bit in the *Mask Register* allows the corresponding bit in the *Status Register* to activate the INT pin. The interrupt condition is cleared by writing a logic 1 to the bit that has been set in the *Status Register*.

The behavior of the INT pin is controlled by the IMODE and IINV bits of the *Configuration Register*.

IMODE	IINV	INT Pin	
0	0	Active-low Level	
0	1	Active-high Level	
1	0	Low Pulse	
1	1	High Pulse	

Table 4. Interrupt Configuration

If the interrupt output signal format is set for either falling or rising edge, the duration of the INT pulse will be at least one DCLK cycle (DCLK = MCLK/K).

5.12.1 Typical Interrupt Handler

The steps below show how interrupts can be handled.

INITIALIZATION:

1) All Status bits are cleared by writing 0xFFFFFF to the Status Register.
2) The condition bits which will be used to generate interrupts are set to logic 1 in the Mask Register.
3) Enable interrupts.

INTERRUPT HANDLER ROUTINE:

4) Read the Status Register.
5) Disable all interrupts.
6) Branch to the proper interrupt service routine.
7) Clear the Status Register by writing back the read value in step 4.
8) Re-enable interrupt
9) Return from interrupt service routine.

This handshaking procedure ensures that any new interrupts activated between steps 4 and 7 are not lost (cleared) by step 7.

5.13 Serial Port Overview

The CS5467 incorporates a serial port transmit and receive buffer with a command decoder that interprets one-byte (8-bit) commands as they are received. There are four types of commands: instructions, synchronizing, register writes, and register reads (See Section 5.15 *Commands* on page 24).

Instructions are one byte in length and will interrupt any instruction currently executing. Instructions do not affect register reads currently being transmitted.

Synchronizing commands are one byte in length and only affect the serial interface. Synchronizing commands do not affect operations currently in progress.

Register writes must be followed by three bytes of data. Register reads can return up to four bytes of data.

Commands and data are transferred most-significant bit (MSB) first. Figure 1 on page 12, defines the serial port timing and required sequence necessary for writing to and reading from the serial port receive and transmit buffer, respectively. While reading data from the serial port, commands and data can be written simultaneously. Starting a new register read command while data is being read will terminate the current read in progress. This is acceptable if the remainder of the current read data is not needed. During data reads, the serial port requires input data. If a new command and data is not sent, SYNC0 or SYNC1 must be sent.

5.13.1 Serial Port Interface

The serial port interface is a “4-wire” synchronous serial communications interface. The interface is enabled to start excepting SCLKs when CS (Chip Select) is asserted (logic 0). SCLK (Serial bit-clock) is a Schmitt-trigger input that is used to strobe the data on SDI (Serial Data In) into the receive buffer and out of the transmit buffer onto SDO (Serial Data Out).

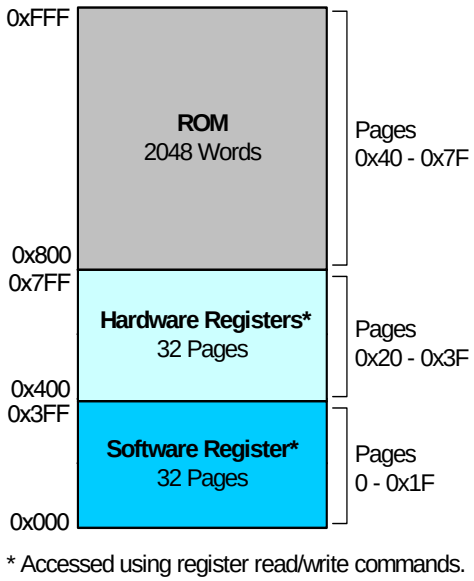
If the serial port interface becomes unsynchronized with respect to the SCLK input, any attempt to clock valid commands into the serial interface may result in unexpected operation. Therefor, the serial port interface must be re-initialized by one of the following actions:

- Drive the $\overline{CS}$ pin high, then low.
- Hardware Reset (drive $\overline{RESET}$ pin low for at least 10 µs).
- Issue the *Serial Port Initialization Sequence*, which is 3 (or more) SYNC1 command bytes (0xFF) followed by one SYNC0 command byte (0xFE).

If a re-synchronization is necessary, it is best to re-initialize the part either by hardware or software reset (command 0x80), as the state of the part may be unknown.

5.14 Register Paging

Read/write commands access one of the 32 registers within a specified page. By default, Page = 0. To access registers in another page, the *Page Register* (address 0x1F) must be written with the desired page number.



* Accessed using register read/write commands.

Figure 12. CS5467 Memory Map

Example:

Reading register 6 in page 3.

1. Write 3 to page register with command and data:

   0x7E 0x00 0x00 0x03

2. Read register 6 with command:

   0x0C 0xFF 0xFF 0xFF

5.15 Commands

All commands are 8 bits in length. Any command byte value that is not listed in this section is invalid. Commands that write to registers must be followed by 3 bytes of data. Commands that read data can be chained with other commands (e.g., while reading data, a new command can be sent which can execute during the original read). All commands except register reads, register writes, and SYNC0 & SYNC1 will abort any currently executing commands.

5.15.1 Start Conversions

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	C3	0	0	0

Initiates acquiring measurements and calculating results. The device has two modes of acquisition.

C3 — Modes of acquisition/measurement
0 = Perform a single computation cycle
1 = Perform continuous computation cycles

5.15.2 SYNC0 and SYNC1

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	SYNC

The serial port is resynchronized to byte boundaries by sending three or more consecutive SYNC1 commands followed by a SYNC0 command. The SYNC0 or SYNC1 commands can also be used as a NOP command.

SYNC — Designates calibration
0 = This command is the end of the serial port re-initialization sequence.
1 = This command is part of the serial port re-initialization sequence.

5.15.3 Power-down, Power-up, Halt and Software Reset

B7	B6	B5	B4	B3	B2	B1	B0
1	0	S1	S0	0	0	0	0

To conserve power the CS5467 has two power-down states. In stand-by state all circuitry, except the analog/digital clock generators, is turned off. In the sleep state all circuitry, except the digital clock generator and the command decoder, is turned off. Bringing the CS5467 out of sleep state requires more time than bringing it out of stand-by state, because of the extra time needed to re-start and re-stabilize the analog clock signal. If the device is powered-down, Power-Up/Halt will initiate a power on reset. If the part is already powered-on, all computations will be halted.

S[1:0] — Power-down state
00 = Software Reset
01 = Halt and enter sleep power saving state. This state requires a slow power-on time
10 = Power-up and Halt
11 = Halt and enter stand-by power saving state. This state allows quick power-on time

5.15.4 Register Read/Write

B7	B6	B5	B4	B3	B2	B1	B0
0	W/$\overline{R}$	RA4	RA3	RA2	RA1	RA0	0

The Read/Write informs the command decoder that a register access is required. During a *read* operation, the addressed register is loaded into the device's output buffer and clocked out by SCLK. During a *write* operation, the data is clocked into the input buffer and transferred to the addressed register upon completion of the 24th SCLK.

W/$\overline{R}$ Write/Read control
0 = Read register
1 = Write register

RA[4:0] Register address bits (bits 5 through 1) of the read/write command.

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Address	RA[4:0]	Name	Description
0	00000	Config	Configuration
1	00001	I	Instantaneous Current
2	00010	V	Instantaneous Voltage
3	00011	P	Instantaneous Power
4	00100	P_{Active}	Average Active (Real) Power
5	00101	I_{RMS}	RMS Current
6	00110	V_{RMS}	RMS Voltage
7	00111	I2	Instantaneous Current 2
8	01000	V2	Instantaneous Voltage 2
9	01001	P2	Instantaneous Power 2
10	01010	$P2_{Active}$	Average Active (Real) Power 2
11	01011	$I2_{RMS}$	RMS Current 2
12	01100	$V2_{RMS}$	RMS Voltage 2
13	01101	Q_{Avg}	Average Reactive Power
14	01110	Q	Instantaneous Reactive Power
15	01111	Status	Status (Write of '1' to status bit will clear the bit)
16	10000	$Q2_{Avg}$	Average Reactive Power 2
17	10001	Q2	Instantaneous Reactive Power 2
18	10010	I_{peak}	Peak Current
19	10011	V_{peak}	Peak Voltage
20	10100	S	Apparent Power
21	10101	PF	Power Factor
22	10110	$I2_{peak}$	Peak Current 2
23	10111	$V2_{peak}$	Peak Voltage 2
24	11000	S2	Apparent Power 2
25	11001	PF2	Power Factor 2
26	11010	Mask	Mask
27	11011	T	Temperature
28	11100	Ctrl	Control
29	11101	P_{pulse}	Active Energy Pulse Output Accumulator
30	11110	S_{pulse}	Apparent Energy Pulse Output Accumulator
31	11111	Q_{pulse} / Page	Reactive Energy Pulse Output Accumulator (read only) and Page (write only)

Note: For proper operation, *do not* attempt to write to unspecified registers.

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Address	RA[4:0]	Name	Description
0	00000	I_{dcoff}	Current DC offset
1	00001	I_{gn}	Current Gain Calibration
2	00010	V_{dcoff}	Voltage DC offset
3	00011	V_{gn}	Voltage Gain Calibration
4	00100	P_{off}	Power Offset
5	00101	I_{acoff}	Current AC (RMS) offset
6	00110	V_{acoff}	Voltage AC (RMS) offset
7	00111	$I2_{dcoff}$	Current DC offset 2
8	01000	$I2_{gn}$	Current Gain Calibration 2
9	01001	$V2_{dcoff}$	Voltage DC offset 2
10	01010	$V2_{gn}$	Voltage Gain Calibration 2
11	01011	$P2_{off}$	Power Offset 2
12	01100	$I2_{acoff}$	Current AC (RMS) offset 2
13	01101	$V2_{acoff}$	Voltage AC (RMS) offset 2
15	01111	PulseRateE	Sets the energy-to-frequency output pulse rate
16	10000	Mode	Operational Modes
17	10001	Epsilon	Epsilon
19	10011	Cycle Count	Number of conversions in one computation cycle (N)
20	10100	Q_{Trig}	Reactive Power calculated from Power Triangle
21	10101	$Q2_{Trig}$	Reactive Power calculated from Power Triangle 2
22	10110	T_{Gain}	Temperature Sensor Gain
23	10111	T_{off}	Temperature Sensor Offset
26	11010	T_{meas}	Temperature Measurement
28	11100	SYS_{gain}	System Gain

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Address	RA[4:0]	Name	Description
0	00000	$VSAG_{duration}$	VSAG Duration
1	00001	$VSAG_{level}$	VSAG Level
4	00100	$ISAG_{duration}$	ISAG Duration
5	00101	$ISAG_{level}$	ISAG Level
8	01000	$V2SAG_{duration}$	VSAG Duration 2
9	01001	$V2SAG_{level}$	VSAG Level 2
12	01100	$I2SAG_{duration}$	ISAG Duration 2
13	01101	$I2SAG_{level}$	ISAG Level 2

Note: For proper operation, *do not* attempt to write to unspecified registers.

5.15.5 Calibration

B7	B6	B5	B4	B3	B2	B1	B0
1	0	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0

The CS5467 can perform system calibrations. Proper input signals must be applied to the current and voltage channel before performing a designated calibration.

CAL[5:4]* Designates calibration to be performed
00 = Channel DC offset
01 = Channel DC gain
10 = Channel AC offset
11 = Channel AC gain

CAL[3:0]* Designates channel to calibrate
0001 = Current channel
0010 = Voltage channel
0100 = Current channel 2
1000 = Voltage channel 2

*By utilizing different combinations for CAL[3:0], multiple channels can be calibrated simultaneously, e.g. CAL[5:0] = 001111 commands the CS5467 to perform a DC offset calibration on all four channels. Values for CAL[5:0] not specified should not be used.

6. REGISTER DESCRIPTION

1. "Default" = bit status after power-on or reset
2. Any bit not labeled is Reserved. A zero should always be used when writing to one of these bits.

6.1 Page 0 Registers

6.1.1 Configuration (Config) Register

Address: 0

23	22	21	20	19	18	17	16
PC[7]	PC[6]	PC[5]	PC[4]	PC[3]	PC[2]	PC[1]	PC[0]
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EWA	-	-	IMODE	IINV	-	-	-
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	iCPU	K[3]	K[2]	K[1]	K[0]

Default = 0x000001

PC[7:0] Phase compensation. Sets a delay in the voltage channel relative to the current channel 1. Default setting is 00000000 = 0.0215 degree phase delay at 60 Hz (when MCLK = 4.096 MHz).

EWA Allows the $\overline{E1}$ and $\overline{E2}$ pins to be configured as open-collector output pins.
0 = Normal outputs (default)
1 = Only the pull-down device of the $\overline{E1}$ and $\overline{E2}$ pins are active

IMODE, IINV Soft interrupt configuration bits. Select the desired pin behavior for indication of an interrupt.
00 = Active-low level (default)
01 = Active-high level
10 = Low pulse
11 = High pulse

iCPU Inverts the CPUCLK clock. In order to reduce the level of noise present when analog signals are sampled, the logic driven by CPUCLK should not be active during the sample edge.
0 = Normal operation (default)
1 = Minimize noise when CPUCLK is driving rising edge logic

K[3:0] Clock divider. A 4-bit binary number used to divide the value of MCLK to generate the internal clock DCLK. The internal clock frequency is DCLK = MCLK/K. The value of K can range between 1 and 16. Note that a value of "0000" will set K to 16 (not zero). K = 1 at reset.

6.1.2 Instantaneous Current (I, I2), Voltage (V, V2), and Power (P, P2) Registers

Address: 1 (I), 2 (V), 3 (P), 7 (I2), 8 (V2), 9 (P2)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

I (I2) and V (V2)contain the instantaneous measured values for current and voltage, respectively. The instantaneous voltage (voltage 2) and current (current 2) samples are multiplied to obtain Instantaneous Power, P (P2). The value is represented in two's complement notation and in the range of $-1.0 \le I, V, P < 1.0$ ($-1.0 \le I2, V2, P2 < 1.0$), with the binary point to the right of the MSB.

6.1.3 Active (Real) Power (P_{Active}, $P2_{Active}$) Registers

Address: 4 (P_{Active}), 10 ($P2_{Active}$)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

The instantaneous power is averaged over each computation cycle (N conversions) to compute Active Power, P_{Active} ($P2_{Active}$). The value will be within in the range of $-1.0 \le P_{Active} < 1.0$ ($-1.0 \le P2_{Active} < 1.0$). The value is represented in two's complement notation, with the binary point to the right of the MSB.

6.1.4 RMS Current (I_{RMS}, $I2_{RMS}$) & Voltage (V_{RMS}, $V2_{RMS}$) Registers

Address: 5 (I_{RMS}), 6 (V_{RMS}), 11 ($I2_{RMS}$), 12 ($V2_{RMS}$)

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

I_{RMS} ($I2_{RMS}$) and V_{RMS} ($V2_{RMS}$) contain the Root Mean Square (RMS) values of I (I2) and V (V2), calculated each computation cycle. The value is represented in unsigned binary notation and in the range of $0.0 \le I_{RMS}, V_{RMS} < 1.0$ ($0.0 \le I2_{RMS}, V2_{RMS} < 1.0$), with the binary point to the left of the MSB.

6.1.5 Instantaneous Reactive Power (Q, Q2) Registers

Address: 14 (Q), 17 (Q2)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

The Instantaneous Reactive Power (Q, Q2) is the product of the voltage (voltage 2) signal, shifted 90 degrees, and the current (current 2) signal. The value is represented in two's complement notation and in the range of $-1.0 < Q < 1.0$ ($1.0 < Q2 < 1.0$), with the binary point to the right of the MSB.

6.1.6 Average Reactive Power (Q_{Avg}, $Q2_{Avg}$) Registers

Address: 13 (Q_{Avg}), 16 ($Q2_{Avg}$)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

The Average Reactive Power (Q_{AVG}, $Q2_{AVG}$) is Q (Q2) averaged over N samples. The value is represented in two's complement notation and in the range of $-1.0 < Q_{AVG} < 1.0$ ($-1.0 < Q2_{AVG} < 1.0$), with the binary point to the right of the MSB.

6.1.7 Status (Status) and Mask (Mask) Register

Address: *15* (*Status*)*; 26 (Mask)*

23	22	21	20	19	18	17	16
DRDY	I2OR	V2OR	CRDY	I2ROR	V2ROR	IOR	VOR
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
E2OR	IROR	VROR	EOR	IFAULT	VSAG	I2FAULT	V2SAG
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TUP	V2OD	I2OD	VOD	IOD	LSD	FUP	$\overline{IC}$

Default = 0x800001 (Status Register), 0x000000 (Mask Register)

The Status Register indicates status within the chip. In normal operation, writing a '1' to a bit will cause the bit to reset. Writing a '0' to a bit will not change it's current state.

The Mask Register is used to control the activation of the $\overline{INT}$ pin. Placing a logic '1' in a Mask bit will allow the corresponding bit in the Status Register to activate the $\overline{INT}$ pin when the status bit is asserted.

DRDY — Data Ready. During conversions, this bit will indicate the end of computation cycles. For calibrations, this bit indicates the end of a calibration sequence.

IOR (I2OR) — Current Out of Range. Set when the magnitude of the measured current value causes the I (I2) register to overflow.

VOR (V2OR) — Voltage Out of Range. Set when the magnitude of the measured voltage value causes the V (V2) register to overflow.

CRDY — Conversion Ready. Indicates a new conversion is ready. This will occur at the output word rate.

IROR (I2ROR) — RMS Current Out of Range. Set when the calculated RMS current value causes the I_{RMS} ($I2_{RMS}$) register to overflow.

VROR (V2ROR) — RMS Voltage Out of Range. Set when the calculated RMS voltage value causes the V_{RMS} ($V2_{RMS}$) register to overflow.

EOR (E2OR) — Energy Out of Range. Set when P_{Active} ($P2_{Active}$) overflows.

IFAULT (I2FAULT) — Indicates a current fault occurred in the power line current. If the absolute value of the instantaneous current is less than $ISAG_{level}$ ($I2SAG_{level}$) for more than half of the $ISAG_{duration}$ ($I2SAG_{duration}$), the IFAULT (I2FAULT) bit will be set.

VSAG (V2SAG) — Indicates a voltage sag occurred in the power line voltage. If the absolute value of the instantaneous voltage is less than $VSAG_{level}$ ($V2SAG_{level}$) for more than half of the $VSAG_{duration}$ ($V2SAG_{duration}$), the VSAG (V2SAG) bit will be set.

TUP — Temperature Updated. Indicates a temperature conversion is ready.

VOD (V2OD) — Modulator Oscillation Detected on the voltage (voltage 2) channel. Set when the modulator oscillates due to an input above full scale. The level at which the modulator oscillates is significantly higher than the voltage (voltage 2) channel's differential input voltage range.

IOD (I2OD) — Modulator Oscillation Detected on the current (current 2) channel. Set when the modulator oscillates due to an input above full scale. The level at which the modulator oscillates is significantly higher than the current (current 2) channel's differential input voltage range.

Note: The IOD (I2OD) and VOD (V2OD) bits may be 'falsely' triggered by very brief voltage

spikes from the power line. This event should not be confused with a DC overload situation at the inputs, when the IOD (I2OD) and VOD (V2OD) bits will re-assert themselves even after being cleared, multiple times.

LSD — Low Supply Detect. Set when the voltage at the PFMON pin falls below the low-voltage threshold (PMLO), with respect to AGND pin. For a given part, PMLO can be as low as 2.3 V. LSD bit cannot be permanently reset until the voltage at PFMON pin rises back above the high-voltage threshold (PMHI), which is typically 100 mV above the device's low-voltage threshold. PMHI will never be greater than 2.7 V.

FUP — Epsilon Updated. Indicates an update to the epsilon value has been placed in the register.

$\overline{IC}$ — Invalid Command. Normally logic 1. Set to logic 0 if the host interface is strobed with an 8-bit word that is not recognized as one of the valid commands (see See Section 5.15 *Commands* on page 24).

6.1.8 Peak Current (I_{peak}, $I2_{peak}$) and Peak Voltage (V_{peak}, $V2_{peak}$) Register

Address: 18 (I_{peak}), 19 (V_{peak}), 22 ($I2_{peak}$), 23 ($V2_{peak}$)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

The Peak Current (I_{peak}, $I2_{peak}$) and Peak Voltage (V_{peak}, $V2_{peak}$) registers contain the instantaneous current and voltage with the greatest magnitude detected during the last computation cycle. The value is represented in two's complement notation and in the range of $-1.0 \le I_{peak}, V_{peak} < 1.0$ ($-1.0 \le I2_{peak}, V2_{peak} < 1.0$), with the binary point to the right of the MSB.

6.1.9 Apparent Power (S, S2) Register

Address: 20 (S), 24 (S2)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Apparent power S (S2) is the product of the V_{RMS} and I_{RMS} ($V2_{RMS}$ and $I2_{RMS}$), The value is represented in unsigned notation and in the range of $0 \le S < 1.0$ ($0 \le S2 < 1.0$), with the binary point to the right of the MSB.

6.1.10 Power Factor (PF, PF2) Register

Address: 21 (PF), 25 (PF2)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Power Factor is calculated by dividing the Active (Real) Power by Apparent Power. The value is represented in two's complement notation and in the range of $-1.0 \le PF < 1.0$ ($-1.0 \le PF2 < 1.0$), with the binary point to the right of the MSB.

6.1.11 Temperature (T) Register

Address: 27

MSB															LSB
$-(2^7)$	2^6	2^5	2^4	2^3	2^2	2^1	2^0	.....	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

T contains measurements from the on-chip temperature sensor. Measurements are performed during continuous conversions, with the default the Celsius scale (ºC). The value is represented in two's complement notation and in the range of $-128.0 \leq T < 128.0$, with the binary point to the right of the eighth MSB.

6.1.12 Control (Crtl) Register

Register Address: 28

23	22	21	20	19	18	17	16
PC2[7]	PC2[6]	PC2[5]	PC2[4]	PC2[3]	PC2[2]	PC2[1]	PC2[0]
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
-	-	-	I2gain	-	-	-	STOP
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	Igain	INTOD	-	NOCPU	NOOSC	-

Default = 0x000000

PC2[7:0] Phase compensation. Sets a delay in the voltage channel relative to current channel 2. Default setting is 00000000 = 0.0215 degree phase delay at 60 Hz (when MCLK = 4.096 MHz).

Igain (I2gain) Sets the gain of the current (current 2) PGA.
0 = Gain is 10 (default)
1 = Gain is 50

STOP Terminates the auto-boot sequence.
0 = Normal (default)
1 = Stop sequence

INTOD Converts $\overline{\text{INT}}$ output pin to an open drain output.
0 = Normal (default)
1 = Open drain

NOCPU Saves power by disabling the CPUCLK pin.
0 = Normal (default)
1 = Disables CPUCLK

NOOSC Saves power by disabling the crystal oscillator.
0 = Normal (default)
1 = Disabling oscillator circuit

6.1.13 Active Energy Pulse Output Accumulator (P_{pulse}) Register

Address: 29

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

The Active Energy Pulse Output Accumulator (P_{pulse}) contains the average active energy measured on channels 1 & 2 and is used to drive the pulse output. The value is represented in two's complement notation and in the range of $-1.0 \le P_{pulse} < 1.0$, with the binary point to the right of the MSB.

6.1.14 Apparent Energy Pulse Output Accumulator (S_{pulse}) Register

Address: 30

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

The Apparent Energy Pulse Output Accumulator (S_{pulse}) contains the average apparent power measured on channels 1 & 2 and is used to drive the pulse output. This result is updated after each computation cycle. The value is represented in two's complement notation and in the range of $-1.0 \le S_{pulse} < 1.0$, with the binary point to the right of the MSB.

6.1.15 Reactive Energy Pulse Output Accumulator (Q_{pulse}) Register

Address: 31 (read only)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

The Reactive Energy Pulse Output Accumulator (Q_{pulse}) contains the average reactive power measured channels 1 & 2 and is used to drive the pulse output. The value is represented in two's complement notation and in the range of $-1.0 \le Q_{pulse} < 1.0$, with the binary point to the right of the MSB.

6.1.16 Page Register

Address: 31 (write only)

MSB						LSB
2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x00

Determines which register page the serial port will access.

6.2 Page 1 Registers

6.2.1 Current DC Offset (I_{dcoff}, $I2_{dcoff}$) and Voltage DC Offset (V_{dcoff}, $V2_{dcoff}$) Registers

Address: 0 (I_{dcoff}), 2 (V_{dcoff}), 7 ($I2_{dcoff}$), 9 ($V2_{dcoff}$)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x000000

The DC Offset registers (I_{dcoff},V_{dcoff}, $I2_{dcoff}$,$V2_{dcoff}$) are initialized to 0.0 on reset. When DC Offset calibration is performed, the register is updated with the DC offset measured over a computation cycle. DRDY will be set at the end of the calibration. This register may be read and stored for future system offset compensation. The value is represented in two's complement notation and in the range of $-1.0 \le I_{dcoff}, V_{dcoff} < 1.0$ ($-1.0 \le I2_{dcoff}, V2_{dcoff} < 1.0$), with the binary point to the right of the MSB. See Section 7.1.2.1 *DC Offset Calibration Sequence* on page 39 for more information.

6.2.2 Current Gain (I_{gn}, $I2_{gn}$) and Voltage Gain (V_{gn}, $V2_{gn}$) Registers

Address: 1 (I_{gn}), 3 (V_{gn}), 8 ($I2_{gn}$), 10 ($V2_{gn}$)

MSB															LSB
2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default = 0x400000 = 1.000

The gain registers (I_{gn},V_{gn}, $I2_{gn}$,$V2_{gn}$) are initialized to 1.0 on reset. When either a AC or DC Gain calibration is performed, the register is updated with the gain measured over a computation cycle. DRDY will be set at the end of the calibration. This register may be read and stored for future system gain compensation. The value is in the range $0.0 \le I_{gn},V_{gn} < 3.9999$ ($0.0 \le I2_{gn},V2_{gn} < 3.9999$), with the binary point to the right of the second MSB.

6.2.3 Power Offset (P_{off}, $P2_{off}$) Registers

Address: 4 (P_{off}), 11 ($P2_{off}$)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x000000

Power Offset (P_{off}, $P2_{off}$) is added to the instantaneous power being accumulated in the P_{active} ($P2_{active}$) register, and can be used to offset contributions to the energy result that are caused by undesirable sources of energy that are inherent in the system. The value is represented in two's complement notation and in the range of $-1.0 \le P_{off} < 1.0$ ($-1.0 \le P2_{off} < 1.0$), with the binary point to the right of the MSB.

6.2.4 Current AC Offset (I_{acoff}, $I2_{acoff}$) and Voltage AC Offset (V_{acoff}, $V2_{acoff}$) Registers

Address: 5 (I_{acoff}), 6 (V_{acoff}), 12 ($I2_{acoff}$), 13 ($V2_{acoff}$)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x000000

The AC Offset Registers (V_{acoff}, I_{acoff}, $V2_{acoff}$, $I2_{acoff}$) are initialized to zero on reset, allowing for uncalibrated normal operation. AC Offset Calibration updates these registers. This sequence lasts approximately (6N + 30) ADC cycles (where N is the value of the *Cycle Count Register*). DRDY will be asserted at the end of the calibration.

These values may be read and stored for future system AC offset compensation. The value is represented in two's complement notation in the range of $-1.0 \le V_{acoff}, I_{acoff} < 1.0$ ($-1.0 \le V2_{acoff}, I2_{acoff} < 1.0$), with the binary point to the right of the MSB.

6.2.5 PulseRateE Register

Address: 15

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x800000 = 1.00 (2 kHz @ 4.096 MHz MCLK)

PulseRateE sets the frequency of $\overline{E1}$, $\overline{E2}$, & $\overline{E3}$ pulses. $\overline{E1}$, $\overline{E2}$, $\overline{E3}$ frequency = (MCLK x PulseRateE) / 2048 at full scale. For a 4 khz sample rate, the maximum pulse rate is 2 khz. The value is represented in two's complement notation and in the range is $-1.0 \le$ PulseRateE < 1.0, with the binary point to the right of the MSB. Negative values have the same effect as positive. See Section 5.5 *Energy Pulse Output* on page 18 for more information.

6.2.6 Operational Mode (Mode) Register

Address: 16

23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
-	-	-		-	-	E2MODE	VHPF2
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IHPF2	VHPF	IHPF	-	E3MODE[1]	E3MODE[0]	POS	AFC

Default = 0x000000

E2MODE — E2 Output Mode
0 = Sign of Active Power (default)
1 = Apparent Power

VHPF(VHPF2) — Enables the High Pass Filter on the voltage channel.
0 = High-pass filter disabled (default)
1 = High-pass filter enabled

IHPF(IHPF2) — Enables the High Pass Filter on the current channel.
0 = High-pass filter disabled (default)
1 = High-pass filter enabled

E3MODE1:0 — E3 Output Mode
00 = Reactive Power (default)
01 = PFMON
10 = Voltage sign
11 = Apparent Power

POS — Positive Energy Only. Negative energy pulses on E1 are suppressed. However, negative P register results will NOT be suppressed.

AFC — Enables automatic line frequency measurement and sets the frequency of the local sine/cosine generator used in fundamental/harmonic measurements. When AFC is enabled, the Epsilon register will be updated periodically.

6.2.7 *Epsilon (ε) Register*

Address: 17

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x01999A = 0.0125 sec

Epsilon (ε) is the ratio of the input line frequency to the sample frequency of the ADC (See Section 5.4 *Performing Measurements* on page 17). Epsilon is either written to the register, or measured during conversions. The value is represented in two's complement notation and in the range of $-1.0 \le \varepsilon < 1.0$, with the binary point to the right of the MSB. Negative values have no significance.

6.2.8 *Cycle Count Register*

Address: 19

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x000FA0 = 4000

Cycle Count, denoted as N, determines the length of one *computation cycle*. During continuous conversions, the computation cycle frequency is (MCLK/K)/(1024∗N). A one second computational cycle period occurs when MCLK = 4.096 MHz, K = 1, and N = 4000.

6.2.9 *Reactive Power (Q_{Trig}, $Q2_{Trig}$) Registers*

Address: 20 (Q_{Trig}), 21 ($Q2_{Trig}$)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

The Reactive Power (Q_{Trig}, $Q2_{Trig}$) is calculated using trigonometric identities. (See Section 4.3 *Power Measurements* on page 15). The value is represented in unsigned notation and in the range of $0 \le Q_{Trig} < 1.0$ ($0 \le Q2_{Trig} < 1.0$), with the binary point to the right of the MSB.

6.2.10 *Temperature Gain (T_{Gain}) Register*

Address: 22

MSB															LSB
2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	.....	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}

Default = 0x34E2E7 = 26.443169117

Temperature gain (T_{Gain}) is utilized to convert from one temperature scale to another. The Celsius scale (ºC) is the default. Values will be within in the range of $0 \le T_{Gain} < 128$. The value is represented in unsigned notation, with the binary point to the right of bit 7th MSB.

6.2.11 Temperature Offset (T_{off}) Register

Address: 23

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0xF38701 = -0.0974425

Temperature offset (T_{off}) is used to remove the temperature channel's offset at the zero-degree reading. Values are represented in two's complement notation and in the range of $-1.0 \le T_{off} < 1.0$, with the binary point to the right of the MSB.

6.2.12 Temperature Measurement (T_{meas}) Register

Address: 26

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x000000

The Temperature Measurement register is used to cycle-steal voltage channel 2 for temperature measurement. Writing a one to the LSB causes the temperature to be measured and the Temperature register (T) to be updated.

6.2.13 System Gain Register (SYS_{Gain})

Address: 28

MSB															LSB
$-(2^1)$	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default = 0x500000 = 1.25

System Gain (SYS_{Gain}) determines the one's density of the channel measurements. Small changes in the modulator due to temperature can be fine adjusted by changing the system gain. The value is represented in two's complement notation and in the range of $-2.0 < SYS_{Gain} < 2.0$, with the binary point to the right of the second MSB.

6.3 Page 2 Registers

6.3.1 Voltage Sag Duration ($VSAG_{duration}$, $V2SAG_{duration}$) Registers

Address: 0 ($VSAG_{duration}$), 8 ($V2SAG_{duration}$)

MSB															LSB
0	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Default = 0x000000

Voltage Sag Duration ($VSAG_{duration}$, $V2SAG_{duration}$) defines the number of instantaneous measurements utilized to determine a sag event. Setting these register to zero will disable this feature. The value is represented in unsigned notation. See Section 5.6 *Sag and Fault Detect Feature* on page 20

6.3.2 Current Fault Duration ($ISAG_{duration}$, $I2SAG_{duration}$) Registers

Address: 4 ($ISAG_{duration}$), 12 ($I2SAG_{duration}$)

MSB															LSB
0	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Default = 0x000000

Current Fault Duration ($ISAG_{duration}$, $I2SAG_{duration}$) defines the number of instantaneous measurements utilized to determine a sag event. Setting these register to zero will disable this feature. The value is represented in unsigned notation. See Section 5.6 *Sag and Fault Detect Feature* on page 20.

6.3.3 Voltage Sag Level ($VSAG_{level}$, $V2SAG_{Level}$) Registers

Address: 1 ($VSAG_{level}$), 9 ($V2SAG_{level}$)

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Default = 0x000000

Voltage Sag Level ($VSAG_{level}$), $V2SAG_{level}$) defines the voltage level that the magnitude of input samples, averaged over the sag duration, must fall below in order to register a sag condition. These value are represented in unsigned notation and in the range of $0 \le VSAG_{level} < 1.0$ ($0 \le V2SAG_{level} < 1.0$), with the binary point to the left of the MSB. See Section 5.6 *Sag and Fault Detect Feature* on page 20.

6.3.4 Current Fault Level ($ISAG_{level}$, $I2SAG_{level}$) Registers

Address: 5 ($ISAG_{level}$), 13 ($I2SAG_{level}$)

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Default = 0x000000

Current Fault Level ($ISAG_{level}$, $I2SAG_{level}$) defines the voltage level that the magnitude of input samples, averaged over the fault duration, must fall below in order to register a fault condition. These value are represented in unsigned notation and in the range of $0 \le ISAG_{level} < 1.0$ ($0 \le I2SAG_{level} < 1.0$), with the binary point to the left of the MSB. See Section 5.6 *Sag and Fault Detect Feature* on page 20.

7. SYSTEM CALIBRATION

7.1 Channel Offset and Gain Calibration

The CS5467 provides digital DC offset and gain compensation that can be applied to the instantaneous voltage and current measurements, and AC offset compensation to the voltage and current RMS calculations.

Since the voltage and current channels have independent offset and gain registers, system offset and/or gain can be performed on either channel without the calibration results from one channel affecting the other.

The computational flow of the calibration sequences are illustrated in Figure 13. The flow applies to both the voltage channel and current channel.

7.1.1 Calibration Sequence

The CS5467 must be operating in its active state and ready to accept valid commands. Refer to 5.15 *Commands* on page 24. The calibration algorithms are dependent on the value N in the *Cycle Count Register* (see Figure 13). Upon completion, the results of the calibration are available in their corresponding register. The DRDY bit in the *Status Register* will be set. If the DRDY bit is to be output on the INT pin, the DRDY bit in the Mask Register must be set. The initial values in the AC gain and offset registers do affect the results of the calibration results.

7.1.1.1 Duration of Calibration Sequence

The value of the *Cycle Count Register* (N) determines the number of conversions performed by the CS5467 during a given calibration sequence. For DC offset and gain calibrations, the calibration sequence takes at least N + 30 conversion cycles to complete. For AC offset calibrations, the sequence takes at least 6N + 30 ADC cycles to complete, (about 6 computation cycles). As N is increased, the accuracy of calibration results will increase.

7.1.2 Offset Calibration Sequence

For DC and AC offset calibrations, the VIN± (V2IN±) pins of the voltage and IIN± (I2IN±) pins of the current channels should be connected to their ground reference level. (see Figure 14.)

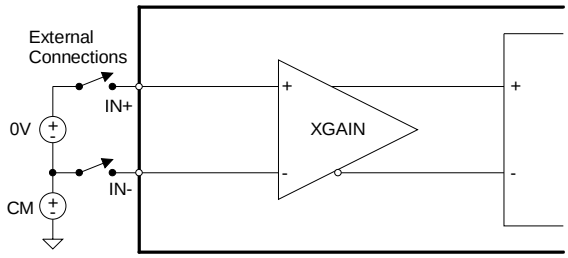


Figure 14. System Calibration of Offset

The AC offset registers must be set to the default (0x000000).

7.1.2.1 DC Offset Calibration Sequence

Channel gain should be set to 1.0 when performing DC offset calibration. Initiate a DC offset calibration. The DC offset registers are updated with the negative of the average of the instantaneous samples collected over a computational cycle. Upon completion of the DC offset calibration the DC offset is stored in the corresponding DC offset register. The DC offset value will be added to

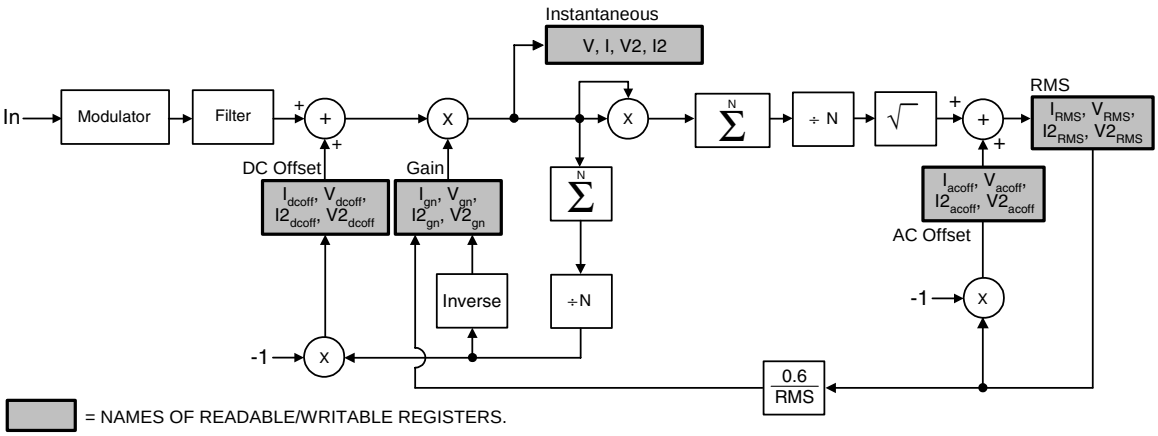


Figure 13. Calibration Data Flow

each instantaneous measurement to nullify the DC component present in the system during conversion commands.

7.1.2.2 AC Offset Calibration Sequence

Corresponding offset registers I_{acoff} ($I2_{acoff}$) and/or V_{acoff} ($V2_{acoff}$) should be cleared prior to initiating AC offset calibrations. Initiate an AC offset calibration.The AC offset registers are updated with an offset value that reflects the RMS output level. Upon completion of the AC offset calibration the AC offset is stored in the corresponding AC offset register. The AC offset register value is subtracted from each successive V_{RMS} and I_{RMS} calculation.

7.1.3 Gain Calibration Sequence

When performing gain calibrations, a reference signal should be applied to the VIN± (V2IN±) pins of the voltage and IIN± (I2IN±) pins of the current channels that represents the desired maximum signal level. Figure 15 shows the basic setup for gain calibration.

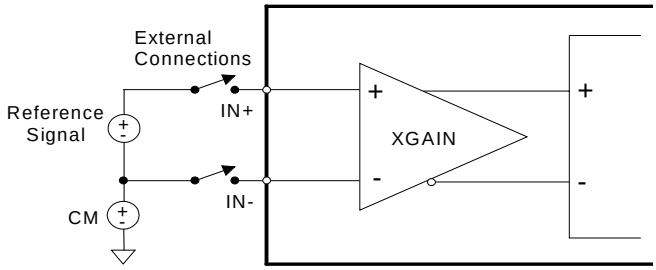


Figure 15. System Calibration of Gain.

For gain calibrations, there is an absolute limit on the RMS voltage levels that are selected for the gain calibration input signals. The maximum value that the gain registers can attain is 4. Therefore, if the signal level of the applied input is low enough that it causes the CS5467 to attempt to set either gain register higher than 4, the gain calibration result will be invalid and all CS5467 results obtained while performing measurements will be invalid.

If the channel gain registers are initially set to a gain other than 1.0, AC gain calibration should be used.

7.1.3.1 AC Gain Calibration Sequence

The corresponding gain register should be set to 1.0, unless a different initial gain value is desired. Initiate an AC gain calibration. The AC gain calibration algorithm computes the RMS value of the reference signal applied to the channel inputs. The RMS register value is then divided into 0.6 and the quotient is stored in the corresponding gain register. Each instantaneous measurement will be multiplied by its corresponding AC gain value.

A typical rms calibration value which allows for reasonable over-range margin would be 0.6 or 60% of the voltage and current channel's maximum input voltage level.

Two examples of AC gain calibration and the updated digital output codes of the channel's instantaneous data registers are shown in Figure 16 and 17. Figure 17

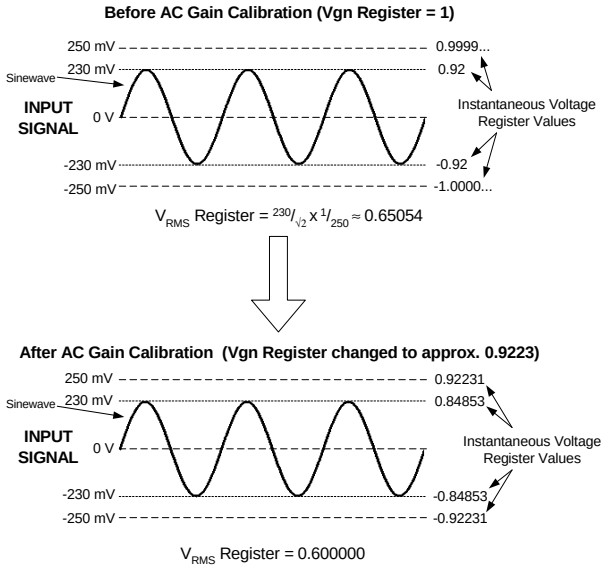


Figure 16. Example of AC Gain Calibration

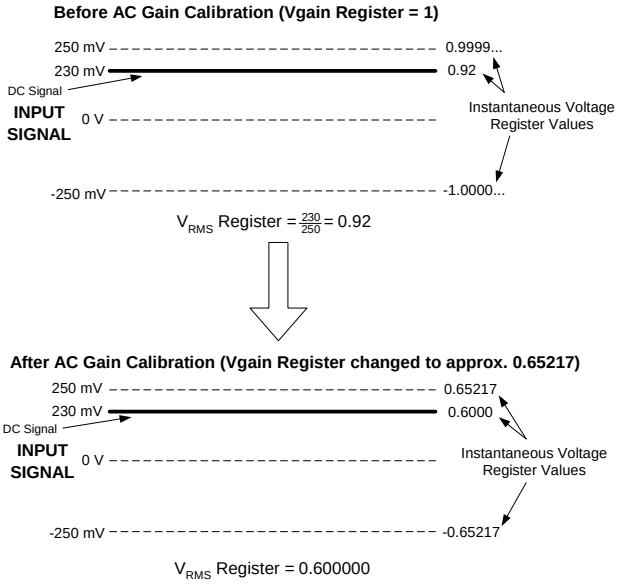


Figure 17. Example of AC Gain Calibration

shows that a positive (or negative) DC-level signal can be used even though an AC gain calibration is being executed.

However, an AC signal cannot be used for DC gain calibration.

7.1.3.2 DC Gain Calibration Sequence

Initiate a DC gain calibration. The corresponding gain register is restored to default (1.0). The DC gain calibration averages the channel's instantaneous measurements over one computation cycle (N samples). The average is then divided into 1.0 and the quotient is stored in the corresponding gain register

After the DC gain calibration, the instantaneous register will read at full-scale whenever the DC level of the input signal is equal to the level of the DC calibration signal applied to the inputs during the DC gain calibration.The HPF option should not be enabled if DC gain calibration is utilized.

7.1.4 Order of Calibration Sequences

1. If the HPF option is enabled, any DC component that may be present in the selected signal path will be removed and a DC offset calibration is not required. However, if the HPF option is disabled the DC offset calibration sequence should be performed.

   When using high-pass filters, it is recommended that the DC Offset register for the corresponding channel be set to zero. When performing DC offset calibration, the corresponding gain channel should be set to one.

2. If there is an AC offset in the V_{RMS} or I_{RMS} calculation, the AC offset calibration sequence should be performed.

3. Perform the gain calibration sequence.

4. Finally, if an AC offset calibration was performed (step 2), the AC offset may need to be adjusted to compensate for the change in gain (step 3). This can be accomplished by restoring zero to the AC offset register and performing an AC offset calibration sequence. The adjustment could also be done by multiplying the AC offset register value that was calculated in step 2 by the gain calculated in step 3 and updating the AC offset register with the product.

7.2 Phase Compensation

The CS5467 is equipped with phase compensation to cancel out phase shifts introduced by the measurement element. Phase Compensation is set by bits PC[7:0] (for channel 1) in the *Configuration Register* and bits PC2[7:0] (for channel 2) in the *Control Register*

The default value of PC[7:0] (PC2[7:0]) is zero. With MCLK = 4.096 MHz and K = 1, the phase compensation has a range of ±5.4 degrees when the input signals are 60 Hz. Under these conditions, each step of the phase compensation register (value of one LSB) is approximately 0.04 degrees. For values of MCLK other than 4.096 MHz, the range and step size should be scaled by 4.096 MHz/(MCLK/K). For power line frequencies other than 60Hz, the values of the range and step size of the PC[7:0] (PC2[7:0]) bits can be determined by converting the above values from angular measurement into the time domain (seconds), and then computing the new range and step size (in degrees) with respect to the new line frequency. To calculate the phase shift induced between the voltage and the current channel use the equation:

$$\text{Phase} = \frac{\text{Freq} \times 360^{\circ} \times \text{PC}[7:0]}{(\text{MCLK}/\text{K})/8}$$

Freq = Line Frequency [Hz]
PC[7:0] = 2's Compliment number in the range of -128 ≤ PC[7:0} < 127

7.3 Active Power Offset

The *Power Offset Register* can be used to offset system power sources that may be resident in the system, but do not originate from the power line signal. These sources of extra energy in the system contribute undesirable and false offsets to the power and energy measurement results. After determining the amount of stray power, the Power Offset Register can be set to cancel the effects of this unwanted energy.

8. AUTO-BOOT MODE USING E²PROM

When the CS5467 MODE pin is asserted (logic 1), the CS5467 *auto-boot mode* is enabled. In auto-boot mode, the CS5467 downloads the required commands and register data from an external serial E²PROM, allowing the CS5467 to begin performing energy measurements.

8.1 Auto-boot Configuration

A typical auto-boot serial connection between the CS5467 and a E²PROM is illustrated in Figure 18. In auto-boot mode, the CS5467's $\overline{CS}$ and SCLK are configured as outputs. The CS5467 asserts $\overline{CS}$ (logic 0), provides a clock on SCLK, and sends a read command to the E²PROM on SDO. The CS5467 reads the user-specified commands and register data presented on the SDI pin. The E²PROM's programmed data is utilized by the CS5467 to change the designated registers' default values and begin registering energy.

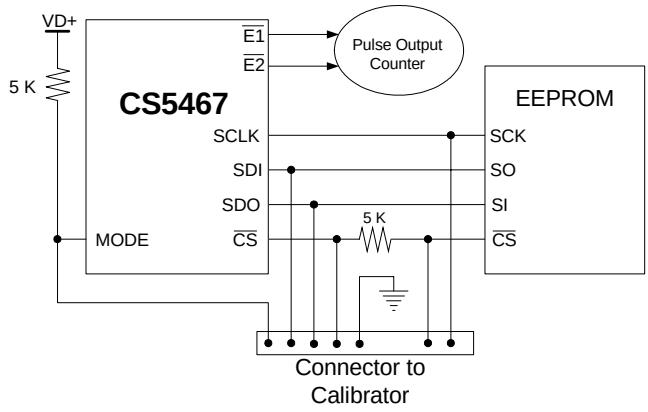


Figure 18. Typical Interface of E²PROM to CS5467

Figure 18 also shows the external connections that would be made to a calibrator device, such as a PC or custom calibration board. When the metering system is installed, the calibrator would be used to control calibration and/or to program user-specified commands and calibration values into the E²PROM. The user-specified commands/data will determine the CS5467's exact operation, when the auto-boot initialization sequence is running. Any of the valid commands can be used.

8.2 Auto-boot Data for E²PROM

Below is an example code set for an auto-boot sequence. This code is written into the E²PROM by the user. The serial data for such a sequence is shown below in single-byte hexidecimal notation:

-7E 00 00 01
Change to page 1.
-60 00 01 E0
Write Operation Mode Register, turn high-pass filters on.
-42 7F C4 A9
Write value of 0x7FC4A9 to Current Gain Register.
-46 FF B2 53
Write value of 0xFFB253 to Voltage Gain Register.
-50 7F C4 A9
Write value of 0x7FC4A9 to Current 2 Gain Register.
-54 FF B2 53
Write value of 0xFFB253 to Voltage 2 Gain Register.
-7E 00 00 00
Change to page 0.
-74 00 00 04
Unmask bit #2 (LSD) in the Mask Register.
-E8
Start continuous conversions
-78 00 01 00
Write STOP bit to Control Register, to terminate auto-boot initialization sequence.

8.3 Which E²PROMs Can Be Used?

Several industry-standard serial E²PROMs that will successfully run auto-boot with the CS5467 are listed below:

- Atmel AT25010, AT25020 or AT25040
- National Semiconductor NM25C040M8 or NM25020M8
- Xicor X25040SI

These types of serial E²PROMs expect a specific 8-bit command (00000011) in order to perform a memory read. The CS5467 has been hardware programmed to transmit this 8-bit command to the E²PROM at the beginning of the auto-boot sequence.

9. BASIC APPLICATION CIRCUITS

Figure 19 shows the CS5467 configured to measure power in a single-phase, 3-wire system while operating in a single-supply configuration. In this diagram, a current transformer (CT) is used to sense the line current and a voltage divider is used to sense the line voltage.

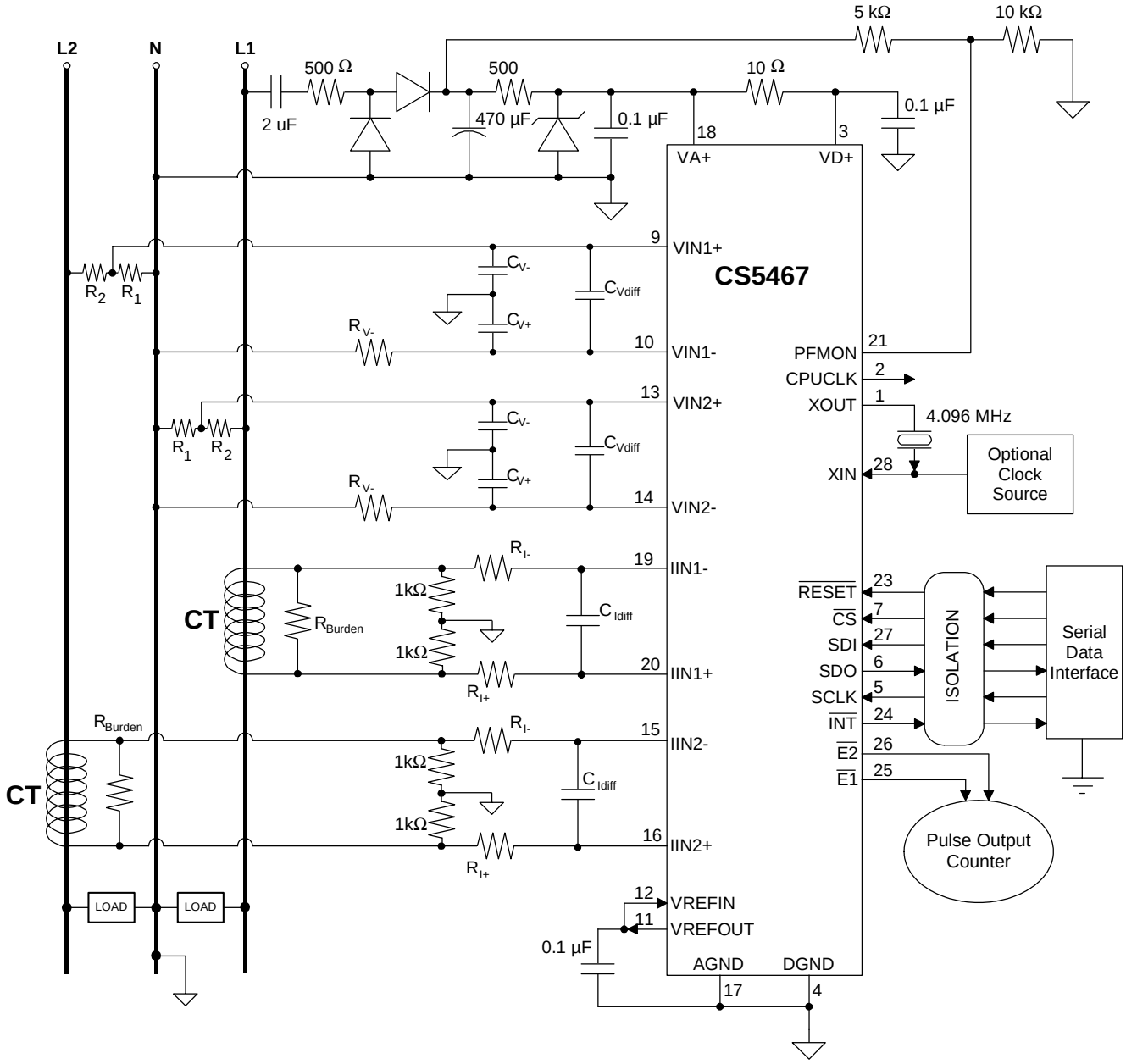
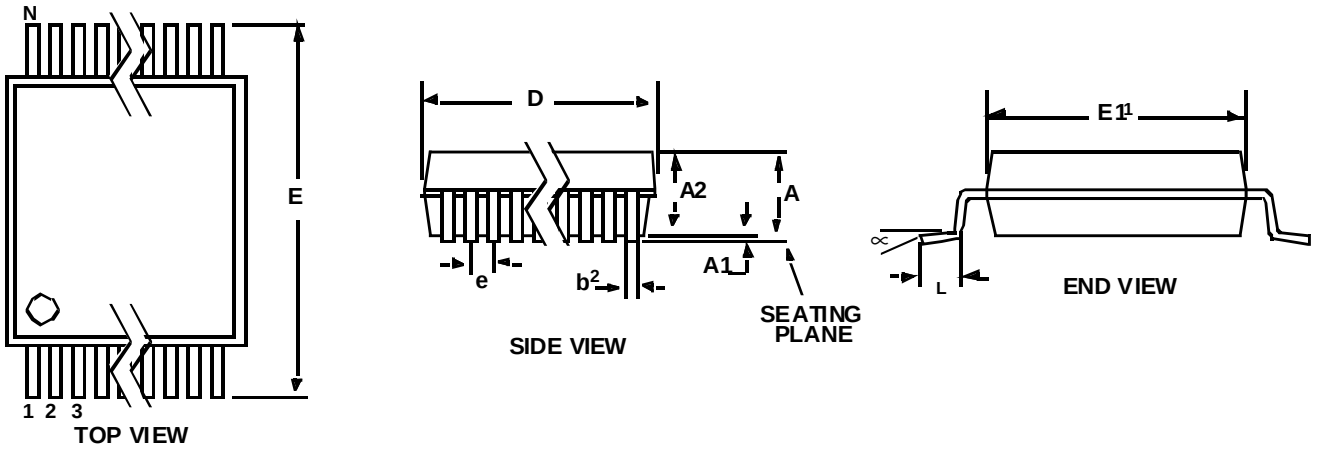


Figure 19. Typical Connection Diagram *(Single-phase, 3-wire – Direct Connect to Power Line)*

10.PACKAGE DIMENSIONS

28L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	?	?	?	?	?	?	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters.

Notes:
3. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
4. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
5. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

11. ORDERING INFORMATION

Model	Temperature	Package
CS5467-IS	-40 to +85 °C	28-pin SSOP
CS5467-ISZ (lead free)		

12. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5467-IS	240 °C	2	365 Days
CS5467-ISZ (lead free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

13. REVISION HISTORY

Revision	Date	Changes
A1	MAR 2006	Advance Release

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com