Preliminary Data Sheet
January 1992

AT&T Microelectronics

ATT7C106 High-Speed CMOS SRAM, 1 Mbit (256K x 4) Common I/O, Output Enable

Features

- High speed —15 ns maximum access time
- Automatic powerdown during long cycles
- Advanced CMOS technology
- TTL-compatible inputs and outputs
- Data retention at 2 V for battery backup operation
- Low-power operation
  - — Active: 635 mW maximum at 25 ns
  - — Standby (typical): 110 mW (TTL inputs); 11 mW (CMOS inputs)
- Package styles available:
  - — 28-pin, plastic DIP
  - — 28-pin, plastic SOJ

Description

The ATT7C106 device is a high-performance, low-power CMOS static RAM organized as 262,144 words by 4 bits per word. The data-in and data-out signals share I/O pins. The ATT7C106 has an active-low chip enable and a separate output enable. This device is available in three speeds with maximum access times from 15 ns to 25 ns.

Inputs and output are TTL compatible. Operation is from a single 5 V power supply. Power consumption is 635 mW (maximum) at 25 ns cycle time. Dissipation drops to 110 mW (typical) when the memory is deselected (enable is high).

Two standby modes are available. Powerdown circuitry reduces power consumption automatically during read or write cycles which are longer than the access time, or when the memory is deselected. In addition, data can be retained in inactive storage with a supply voltage as low as 2 V. The ATT7C106 consumes only 1.5 mW (typical) at 3 V, allowing effective battery backup operation.

Pin Information

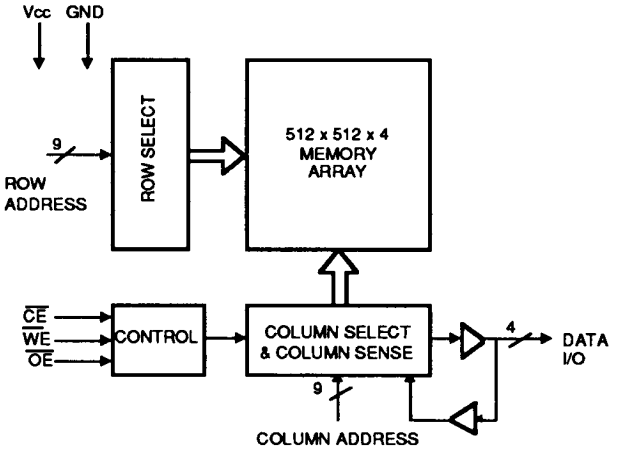


Figure 1. Block Diagram

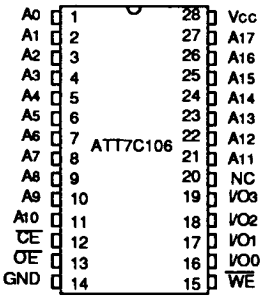


Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Function
A0—A17	Address Inputs
I/O0—I/O3	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
GND	Ground
Vcc	+5 V Supply
NC	No Connection

Functional Description

The ATT7C106 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low chip enable and an active-low output enable simplify control of the 3-state I/O bus, easing the connection of several chips for increased storage capacity.

Writing to the device occurs when both chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are taken low. Data on the four I/O pins (I/O0 through I/O3) is written into the memory location specified on the address pins (A0 through A17). During a write operation, the output enable ($\overline{OE}$) may be either low or high.

Reading the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) low while write enable ($\overline{WE}$) remains high. Under these conditions, the contents of the memory location specified on the address pins will appear on the four I/O pins (I/O0 through I/O3).

The data I/O pins (I/O0 through I/O3) on the ATT7C106 are placed in a high-impedance state when the device is deselected ($\overline{CE}$ is high), or when the I/O pins are disabled ($\overline{OE}$ high and $\overline{WE}$ high).

The ATT7C106 will go into powerdown mode (standby I_{SB}) when chip enable ($\overline{CE}$) is taken high without regard to the state of either output enable ($\overline{OE}$) or write enable ($\overline{WE}$). Table 3 summarizes this data.

Latch-up and static discharge protection are provided on-chip. The ATT7C106 can withstand an injection current of up to 200 mA on any pin without damage.

Truth Table

Table 2. Truth Table for the ATT7C106

($\overline{CE}$)	($\overline{WE}$)	($\overline{OE}$)	I/O0—I/O3	Mode	Power
H	X	X	High Z	Powerdown	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those indicated in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	150	°C
Operating Ambient Temperature	T_A	0	70	°C
Supply Voltage with Respect to Ground	V_{CC}	–0.5	7.0	V
Input Signal with Respect to Ground	—	–3.0	7.0	V
Signal Applied to High-impedance Output	—	–3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latch-up Current	—	>200	—	mA

Handling Precautions

The ATT7C106 device includes internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0 °C to 70 °C	4.5 V ≤ Vcc ≤ 5.5 V
Data Retention, Commercial	0 °C to 70 °C	2.0 V ≤ Vcc ≤ 5.5 V

Electrical Characteristics

Over all recommended operating conditions.

Table 3. General Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage:						
High	V_{OH}	I_{OH} = –4.0 mA, Vcc = 4.5 V	2.4	—	—	V
Low	V_{OL}	I_{OL} = 8.0 mA	—	—	0.4	V
Input Voltage:						
High	V_{IH}	—	2.2	—	Vcc + 0.3	V
Low[1]	V_{IL}	—	–3.0	—	0.8	V
Input Current	I_{IX}	GND ≤ V_{IN} ≤ Vcc	–10	—	10	µA
Output Leakage Current	I_{OZ}	GND ≤ V_{OUT} ≤ Vcc, $\overline{CE}$ = Vcc	–10	—	10	µA
Output Short Current	I_{OS}	V_{OUT} = GND, Vcc = Max[2]	—	—	–350	mA
Vcc Current:						
TTL Inactive[3]	I_{CC2}	—	—	20	30	mA
CMOS Standby[4]	I_{CC3}	—	—	2	25	mA
Data Retention Mode[5]	I_{CC4}	Vcc = 3.0 V	—	0.5	8	mA
Capacitance (SOJ Package)[7]:						
Inputs (A0—A17)	C_I	Ambient Temp = 25 °C, Vcc = 5.0 V	—	—	6	pF
Inputs ($\overline{CE}$, $\overline{WE}$, $\overline{OE}$)	C_I	Test Frequency = 1 MHz[6]	—	—	8	pF
Outputs (I/O0—I/O3)	C_O		—	—	8	pF

1. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.
2. Duration of the output short circuit test should not exceed 30 seconds.
3. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ VIH; max Vcc.
4. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = Vcc. Input levels are within 0.2 V of Vcc or ground; max Vcc.
5. Data retention operation requires that Vcc never drop below 2.0 V. $\overline{CE}$ must be ≥ Vcc – 0.2 V. For all other inputs, V_{IN} ≥ Vcc – 0.2 V or V_{IN} ≤ 0.2 V is required to ensure full powerdown.
6. These parameters are not 100% tested.
7. Consult AT&T regarding DIP package capacitiance.

Table 4. Electrical Characteristics By Speed

Parameter	Symbol	Test Conditions	Speed (ns)			Unit
			25	20	15	
Max Vcc Current, Active	I_{CC1}	*	115	140	180	mA

* Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}, Vcc = max, and I_{OUT} = 0 mA. Input pulse levels are within 0 V to 3.0 V. Max Icc shown applies over the active operating temperature range.

Timing Characteristics

Table 5. Read Cycle [1, 2, 3, 4, 5, 6] (See Figures 3, 4, and 5.)

Symbol	Parameter	Speed (ns)					
		25		20		15	
		Min	Max	Min	Max	Min	Max
tADVADX, tCELCEH	Read Cycle Time	25	—	20	—	15	
tADVDOV	Address Valid to Output Valid[7]	—	25	—	20	—	15
tADVDOX	Address Valid to Output Change[7]	3	—	3	—	3	—
tCELDOV	Chip Enable Low to Output Valid[8]	—	25	—	20	—	15
tCELDOZ	Chip Enable Low to Output Low Z[9, 10]	3	—	3	—	3	—
tCEHDOZ	Chip Enable High to Output High Z[9, 10]	—	10	—	8	—	8
tOELDOV	Output Enable Low to Output Valid	—	10	—	10	—	8
tOELDOZ	Output Enable Low to Output Low Z[9, 10]	0	—	0	—	0	—
tOEHDOZ	Output Enable High to Output High Z[9, 10]	—	10	—	8	—	8
tCELICH, tADVICH	Input Transition to Powerup[11, 12]	0	—	0	—	0	—
tICHICL	Powerup to Powerdown[11, 12]	—	30	—	25	—	20
tCEHVCL	Chip Enable High to Data Retention[11]	0	—	0	—	0	—
tVCHCEL	End of Data Retention to Beginning of Read Cycle[11]	—	25	—	20	—	15

1. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Figure 8), and input pulse levels of 0 V to 3.0 V (Figure 9).
2. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADVCEH (Table 6) is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
3. All address timings are referenced from the last valid address line to the first transitioning address line.
4. $\overline{CE}$ must be inactive or $\overline{WE}$ must be high during address transitions.
5. This product is a very high-speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.
6. $\overline{WE}$ is high for the read cycle.
7. The chip is continuously selected $\overline{OE}$ and $\overline{CE}$ = V_{IL}.
8. All address lines are valid prior to or coincident with the $\overline{CE}$ transition to low.
9. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
10. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 8. This parameter is sampled and not 100% tested.
11. These parameters are not 100% tested.
12. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) transition of $\overline{CE}$ to an active state, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active). The device automatically powers down from I_{CC2} to I_{CC1} after tICHICL has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, not on chip enable pulse width. The device automatically powers down from I_{CC2} to I_{CC1} after tICHICL has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, not on chip enable pulse width.

Timing Characteristics (continued)

Table 6. Write Cycle[1, 2, 3, 4, 5, 10, 11, 12] (See Figures 6 and 7.)

Symbol	Parameter	Speed (ns)					
		25		20		15	
		Min	Max	Min	Max	Min	Max
tADVADX	Write Cycle Time	20	—	20	—	15	—
tCELWEH, tCELCEH	Chip Enable Low to End of Write	15	—	15	—	12	—
tADVWEX, tADVCEL	Address Valid to Beginning of Write	0	—	0	—	0	—
tADVWEH, tADVCEH,	Address Valid to End of Write	15	—	15	—	12	—
tWEHADX, tCEHADX	End of Write to Address Change	0	—	0	—	0	—
tWELWEH, tWELCEH	Write Enable Pulse Width	15	—	15	—	12	—
tDIVWEH, tDIVCEH	Data Valid to End of Write	10	—	10	—	7	—
tWEHDIX, tCEHDIX	End of Write to Data Change	0	—	0	—	0	—
tWEHDOX	Write Enable High to Output Low Z[6, 7]	0	—	0	—	0	—
tWELDOZ	Write Enable Low to Output High Z[6, 7]	—	7	—	7	—	5
tCELICH	Input Transition to Powerup[8, 9]	0	—	0	—	0	—
tICHICL	Powerup to Powerdown[8, 9]	—	30	—	25	—	20

1. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Figure 8), and input pulse levels of 0 V to 3.0 V (Figure 9).
2. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADVCEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
3. All address timings are referenced from the last valid address line to the first transitioning address line.
4. $\overline{CE}$ must be inactive or $\overline{WE}$ must be high during address transitions.
5. This product is a very high-speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.
6. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
7. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 8. This parameter is sampled and not 100% tested.
8. These parameters are not 100% tested.
9. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active). The device automatically powers down from I_{CC2} to I_{CC1} after tICHICL has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, not on chip select pulse width.
10. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last and rises first.
11. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high-impedance state.
12. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Timing Characteristics (continued)

Timing Diagrams

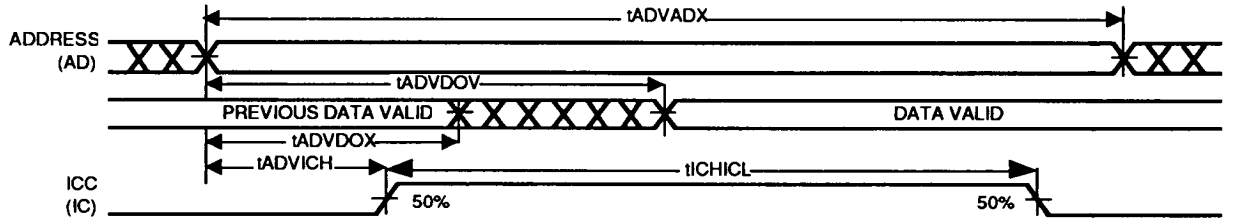


Figure 3. Read Cycle — Address Controlled (See Table 5, Notes 6 and 7.)

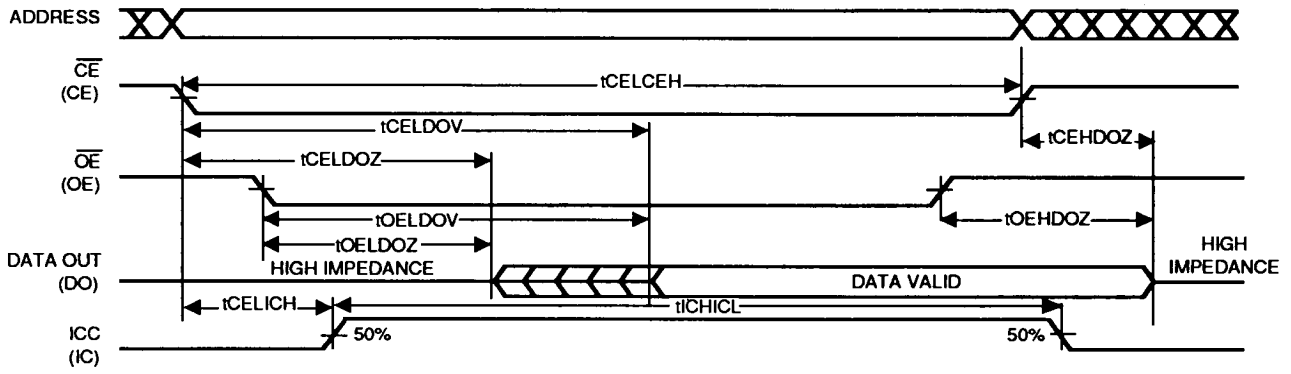


Figure 4. Read Cycle — $\overline{CE}$ / $\overline{OE}$ Controlled (See Table 5, Notes 6 and 7.)

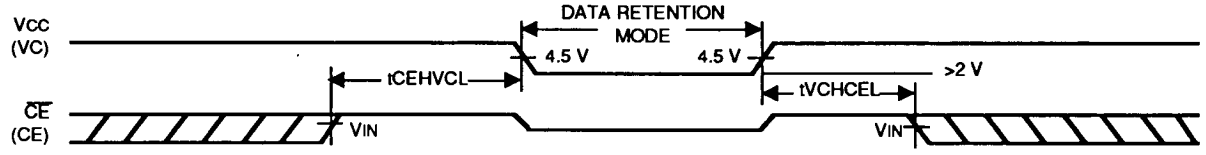


Figure 5. Data Retention

Timing Characteristics (continued)

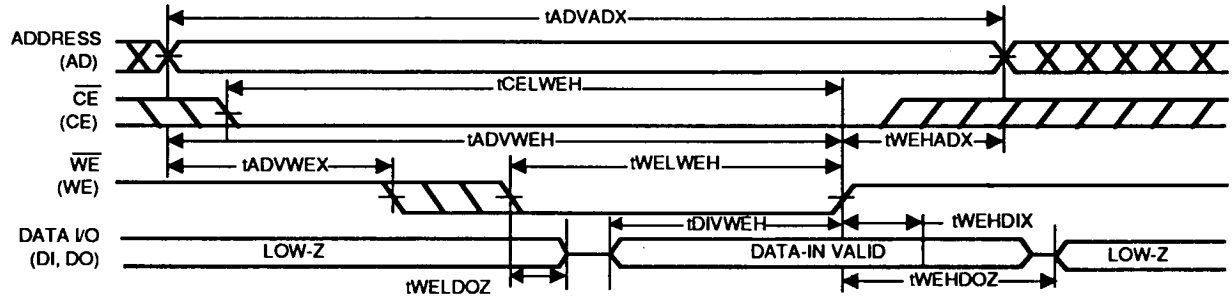


Figure 6. Write Cycle — $\overline{WE}$ Controlled ($\overline{OE}$ Low During Write)

(See Table 6, Notes 9, 10, 11, 12.)

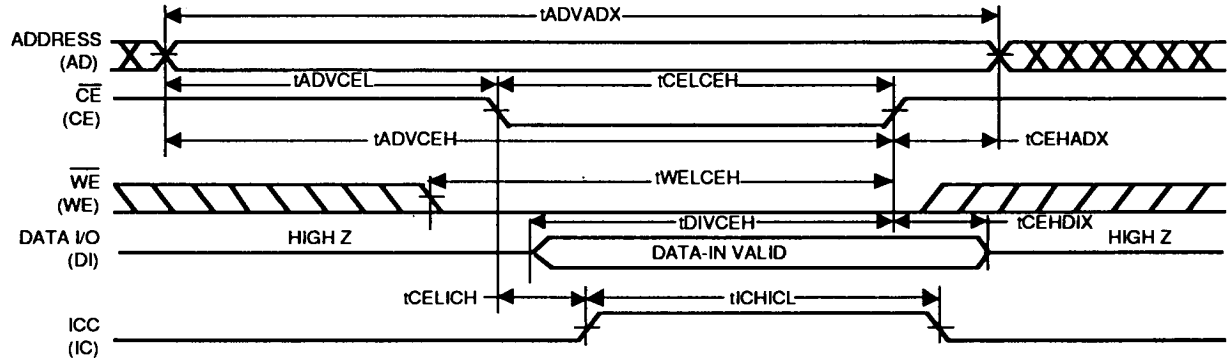


Figure 7. Write Cycle — $\overline{CE}$ Controlled

(See Table 6, Notes 9, 10, 11, 12.)

Timing Characteristics (continued)

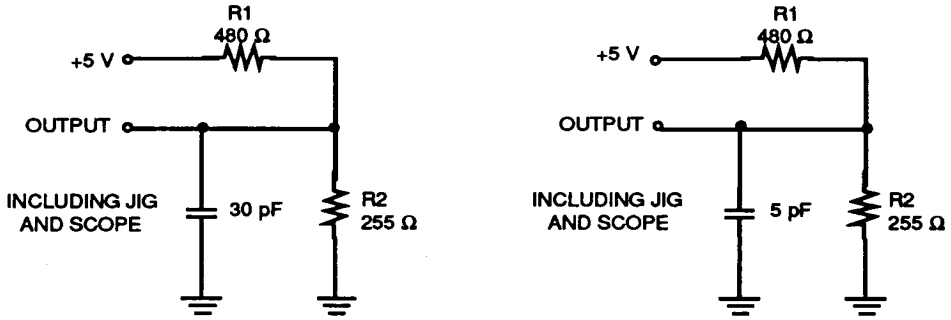


Figure 8. Test Loads

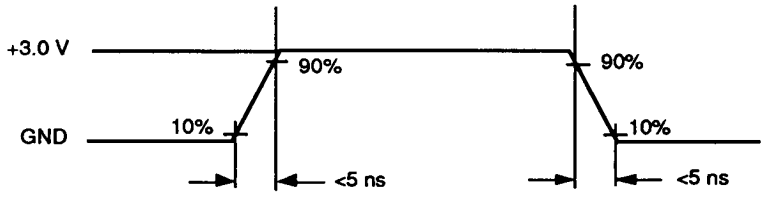
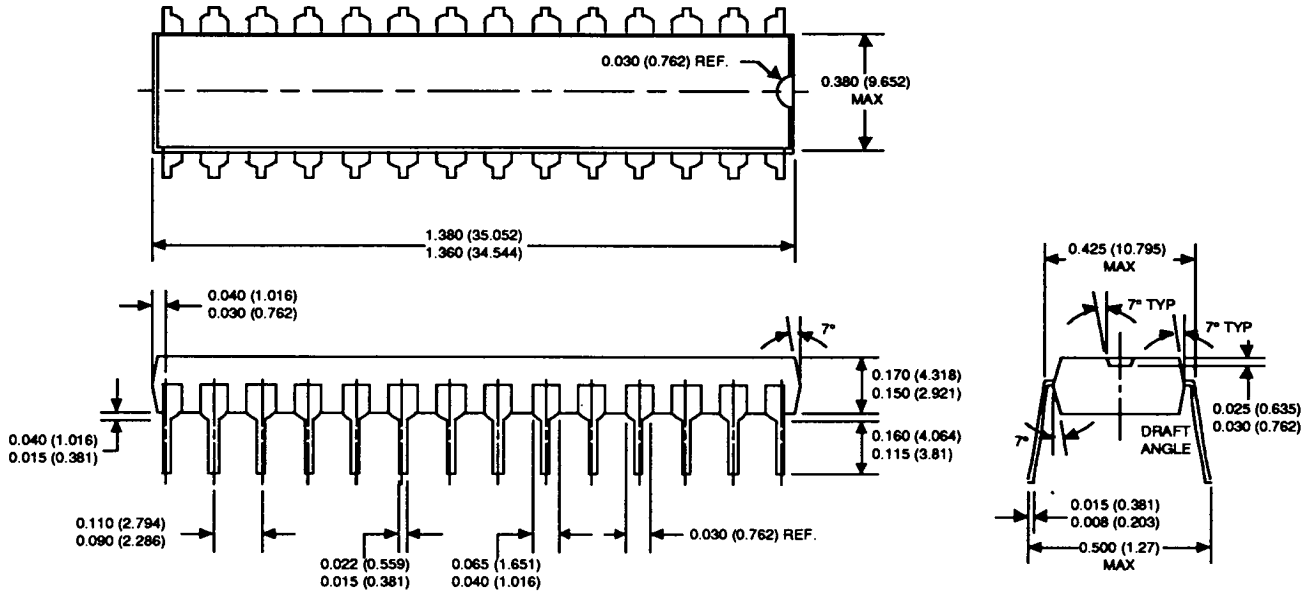


Figure 9. Transition Times

Outline Diagrams

28-Pin, Plastic DIP

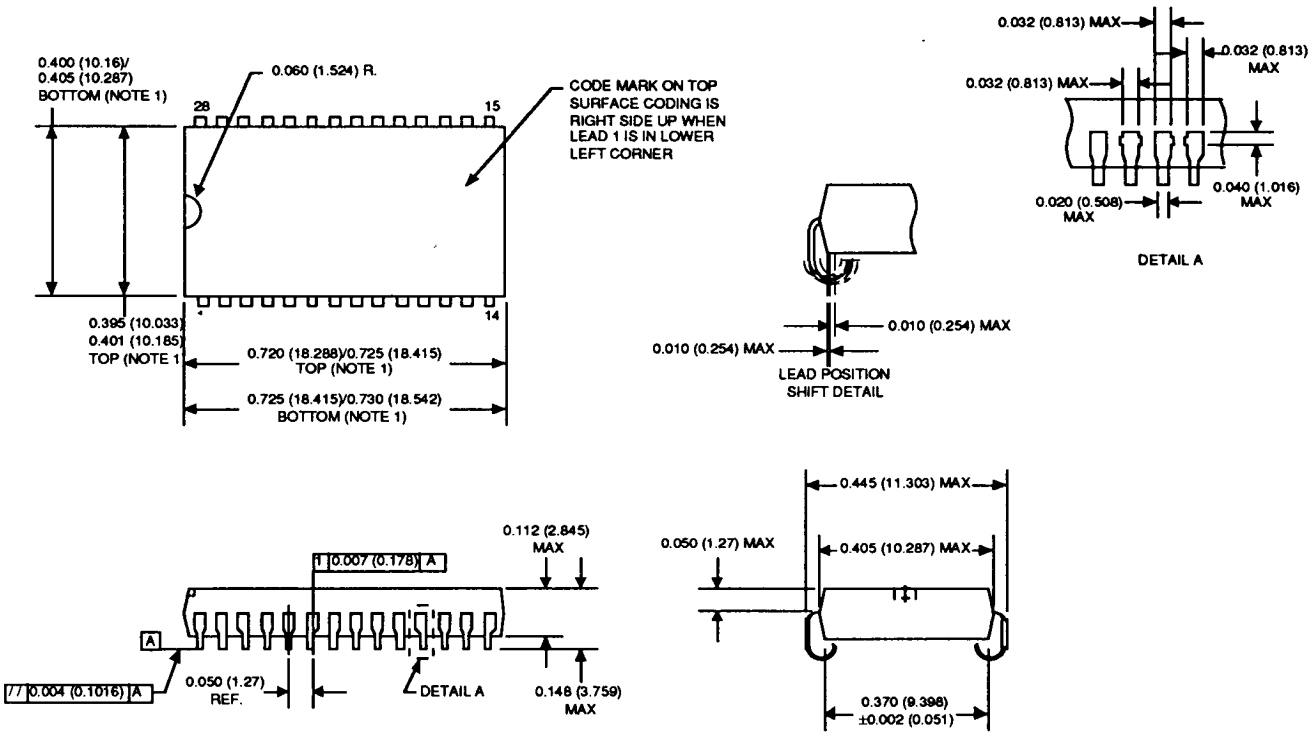
Dimensions are in inches and (millimeters).



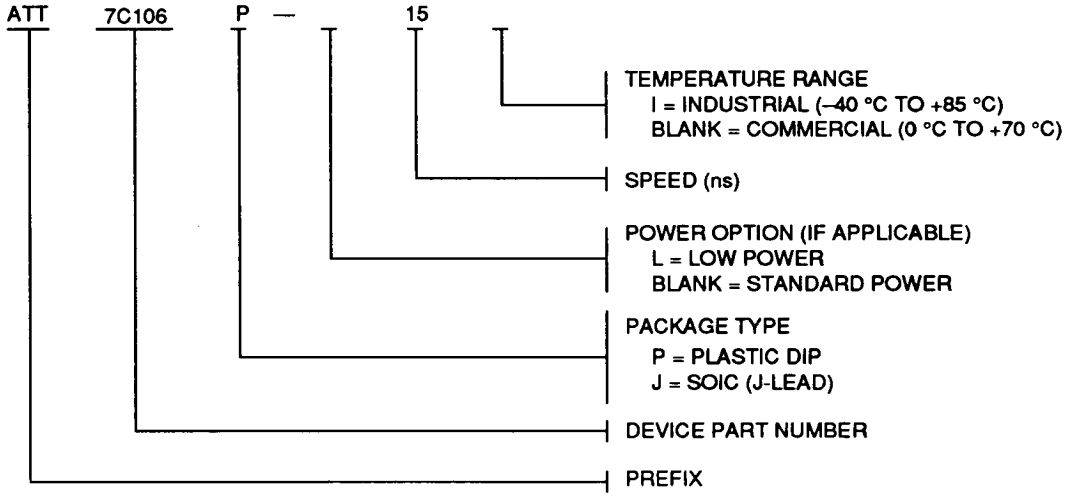
Outline Diagrams (continued)

28-Pin, Plastic SOJ

Dimensions are in inches and (millimeters).



Ordering Information



Operating Range 0 °C to 70 °C

Package Style	Performance Speed		
	25 ns	20 ns	15 ns
28-Pin, Plastic DIP	ATT7C106P–25	ATT7C106P–20	ATT7C106P–15
28-Pin, Plastic SOJ	ATT7C106J–25	ATT7C106J–20	ATT7C106J–15

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