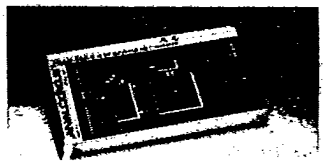

ANALOGIC

ADAM-826-2

16-Bit, 2.0 μs A/D Converter with Input Buffer Amplifier

Description T-51-10-16

In systems that simultaneously sample multiple channels prior to multiplexing the analog signal, a sample-and-hold (S/H) directly at the input to the A/D Converter is not required. In other multi-channel systems, the analog inputs will be essentially low frequency and stable during conversion. In either case, the high conversion rate of the ADAM-826-2 may be desirable in order to minimize the time required to input the data and clear the input channel to the computer. The unit includes a high input impedance (100 MΩ) buffer with settling time of less than 400 ns resulting in an overall conversion time of 2.0 μs. Input full scale ranges of ±10V bipolar or 0V to +10V unipolar can be accommodated. To make the ADAM-826-2 even more flexible, the output of the buffer amplifier and the input to the A/D Converter are brought out to separate pins. Normally, these two pins would be connected together as shown in the Block Diagram in Figure 9; however, this connection may be broken, or signals may be injected at this point. This should be done only when absolutely required by external system considerations as the output of the buffer amplifier is not short-circuit protected. Refer also to the sections on the ADAM-826-3 and PC BOARD LAYOUT.

In order to determine whether an error will occur due to the changing signal without using a S/H, the system designer need only consider the first 1.5 μs of the conversion process. Any change in input signal thereafter will not affect the result as this remaining time is used to complete the conversion and to transfer the resulting data word to the internal output data register. This timing relationship is depicted in the Typical Timing Diagram of Figure 10.

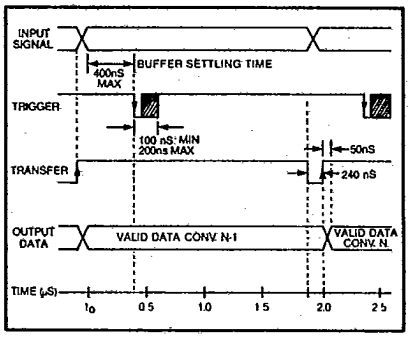

Figure 10. Typical Timing — ADAM-826-2.

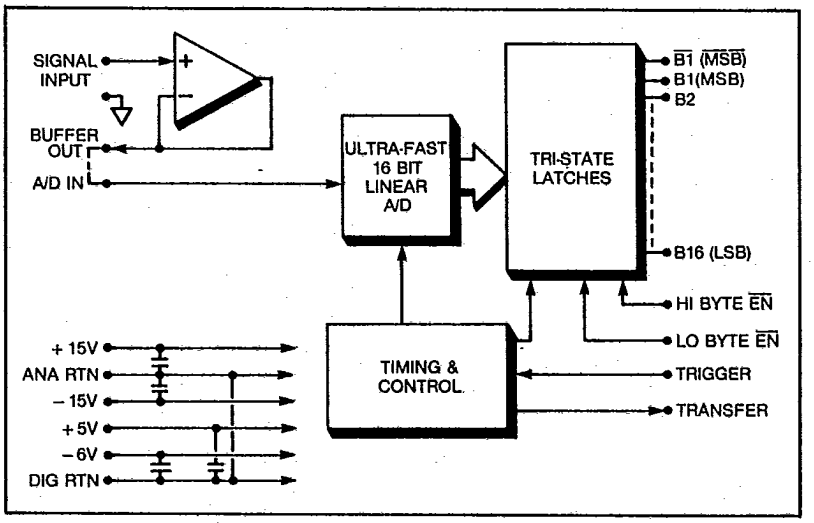

Figure 9. Block Diagram — ADAM-826-2.

SPECIFICATIONS T-51-10-16

(All specifications guaranteed at 25°C unless otherwise noted)

COMBINED BUFFER AMPLIFIER AND A/D PERFORMANCE

Note: These specifications represent the total error of all sources including both the Buffer Amplifier and A/D converter errors. As tabulated in subsequent sections, the specifications for the Buffer Amplifier and A/D by themselves are even better.

INPUT

Input Voltage Range
0V to +10V Unipolar
(See Note 1.)
±10V Bipolar
Factory configured

Maximum Input Without Damage
±Supply

Input Impedance
100 MΩ // 10 pF typical

Input Bias Current
±100 pA maximum

THROUGHPUT

Conversion Time
2.0 μs maximum

Conversion Rate
500,000 samples per second

ACCURACY

Resolution
16-bits

Differential Non-linearity
±1/4 LSB typical,
±3/4 LSB maximum

Monotonicity
Guaranteed; no missing codes

Quantization Error
±1/2 LSB

Relative Accuracy
±0.0015% FSR typical (See Note 2.)
±0.0025% FSR maximum (See Note 2.)

Absolute Accuracy (Includes Reference Accuracy)
±0.004% FSR maximum. The Internal Reference (and offset) may be adjusted against a standard source traceable to the National Bureau of Standards for even better Absolute Accuracy

Noise
Unipolar: 45 μV rms maximum
Bipolar: 70 μV rms maximum

STABILITY

Differential Non-linearity Tempco
±1 ppm/°C FSR maximum

Offset Tempco
Unipolar: ±3 ppm/°C maximum
Bipolar: ±5 ppm/°C maximum

Gain Tempco
±5 ppm FSR/°C maximum

Power Supply Sensitivity Gain
±10 ppm/Δ1% each supply, maximum

Offset
±10 ppm/Δ1% each supply, maximum

Warmup Time to Specified Accuracy
10 minutes (See Note 3.)

Recommended Recalibration Interval
6 months

DIGITAL INPUTS/OUTPUTS

INPUTS

Trigger
Negative edge triggered; 1 LSTTL load; 100 ns pulse width minimum, 200 ns maximum; CMOS and 74 LSTTL Compatible (See Note 5.)

Tri-state Control
HI Byte Enable
Logic 1 produces high impedance

LO Byte Enable
Logic 1 produces high impedance CMOS and 74 LSTTL Compatible

OUTPUTS

Data
16 bits data plus B1; Offset Binary or two's complement; See Coding Table; Tri-state CMOS latch (Silicon gate)

Data Output Loading
1 LSTTL load

Transfer (XFER)
Positive edge loads output data latches; data ready after 50 ns delay

Transfer (XFER) Loading
1 LSTTL Load

POWER REQUIREMENTS

+15V ±0.5V
60 mA, typical
−15V ±0.5V
85 mA, typical
+5V ±0.25V
95 mA, typical
−6V ±0.25V
140 mA, typical (See Note 4.)

Note:
At power on, a 200 mA maximum current surge on the ±15V supply lines will occur, and will last for no more than 5 seconds. This surge is caused by the Reference heater circuit when starting "cold".

Note:
The ±15V power supplies must have no more than 5 mV p-p ripple.

T-51-10-16

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +60°C

Storage Temperature Range
−25°C to +70°C

Relative Humidity
0 to 85%, non condensing

Dimensions and Shielding Modupac®
3.00" x 5.00" x 0.44"
(76.2 x 127.0 x 11.17 mm)
RFI 6 sides, EMI 5 sides

INPUT BUFFER AMPLIFIER ONLY

INPUT

Input Voltage Range
0V to +10V Unipolar
±10V Bipolar
Factory configured

Maximum Input Without Damage
±Supply

Input Impedance
100 MΩ // 10 pF typical

Input Bias Current
±100 pA maximum

AC PERFORMANCE

Small Signal Bandwidth
5 MHz typical

Full Power Bandwidth
250 kHz

Non-linearity
±0.001% FSR maximum

Buffer Settling Time
400 ns to ±0.0015% of Full Scale step

Noise
25 μV rms typical,
35 μV rms maximum

Output Drive Capability
1 kΩ // 50 pF; This output is NOT short circuit protected

A/D CONVERTER ONLY

ANALOG INPUT

Input Voltage
0V to +10V unipolar
−10V to +10V bipolar
Factory configured

Input Impedance
1.4 kΩ unipolar
2.8 kΩ bipolar

ACCURACY

Resolution
16 bits

Differential Non-linearity
±1/4 LSB typical,
±3/4 LSB maximum

Monotonicity
Guaranteed; no missing codes

Quantization Error
±1/2 LSB

Relative Accuracy
±0.0015% FSR maximum

Absolute Accuracy
±0.003% FSR maximum

Noise (Including Ref.)
Unipolar: 30 μV rms, maximum
Bipolar: 60 μV rms, maximum

STABILITY

Differential Non-Linearity Tempco
±1 ppm/°C maximum

Offset Tempco
Unipolar: ±1.5 ppm/°C max.
Bipolar: ±4.5 ppm/°C max.

Gain Tempco
±5 ppm/°C maximum

Warmup Time
10 minutes to specified accuracy

Recommended Recalibration Interval
6 months

THROUGHPUT

Conversion Time
1.5 μs maximum

Note 1: Input Voltage range is determined by the A/D Converter. The Buffer Amplifier is a unity gain device.
Note 2: Specified as the maximum deviation from a best fit line. Maximum deviation from a straight line drawn through the full scale end points is ±0.0035%.
Note 3: Time required for internal reference heater to stabilize.
Note 4: −6V may be readily derived from the −15V power supply using a 7906-type three-terminal regulator. See Figure 1.
Note 5: The 100 ns pulse width is recommended where possible.

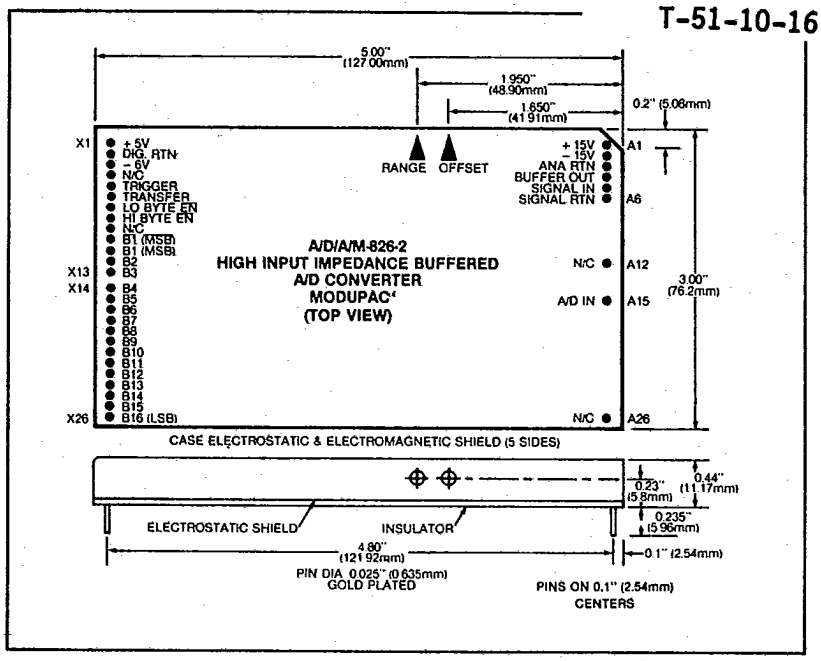

Figure 11. ADAM-826-2 Mechanical & Pinout.