T-45-07-00

National Semiconductor

54F/74F583
4-Bit BCD Adder

General Description

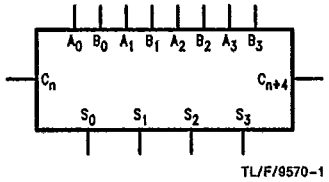
The 'F583 high-speed 4-bit, BCD full adder with internal carry lookahead accepts two 4-bit decimal numbers (A_0–A_3, B_0–B_3) and a Carry Input (C_n). It generates the decimal sum outputs (S_0–S_3), and a Carry Output (C_{n+4}) if the sum is greater than 9. The 'F583 is the functional equivalent of the 82S83.

Features

- Adds two decimal numbers
- Full internal lookahead
- Fast ripple carry for economical expansion
- Sum output delay time 16.5 ns max
- Ripple carry delay time 8.5 ns max
- Input to ripple delay time 14.0 ns max
- Supply current 60 mA max
- Available in SOIC, (300 mil only)

Ordering Code: See Section 5

Logic Symbols



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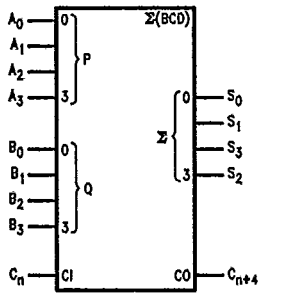
IEEE/IEC



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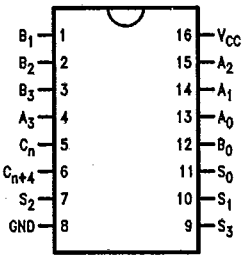
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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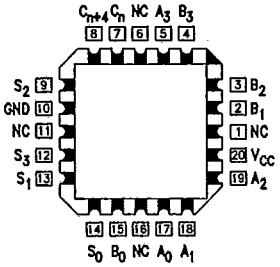
Pin Assignment for LCC



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Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_3	A Operand Inputs	1.0/2.0	20 μA/−1.2 mA
B_0–B_3	B Operand Inputs	1.0/2.0	20 μA/−1.2 mA
C_n	Carry Input	1.0/1.0	20 μA/−0.6 mA
S_0–S_3	Sum Outputs	50/33.3	−1 mA/20 mA
C_{n+4}	Carry Output	50/33.3	−1 mA/20 mA

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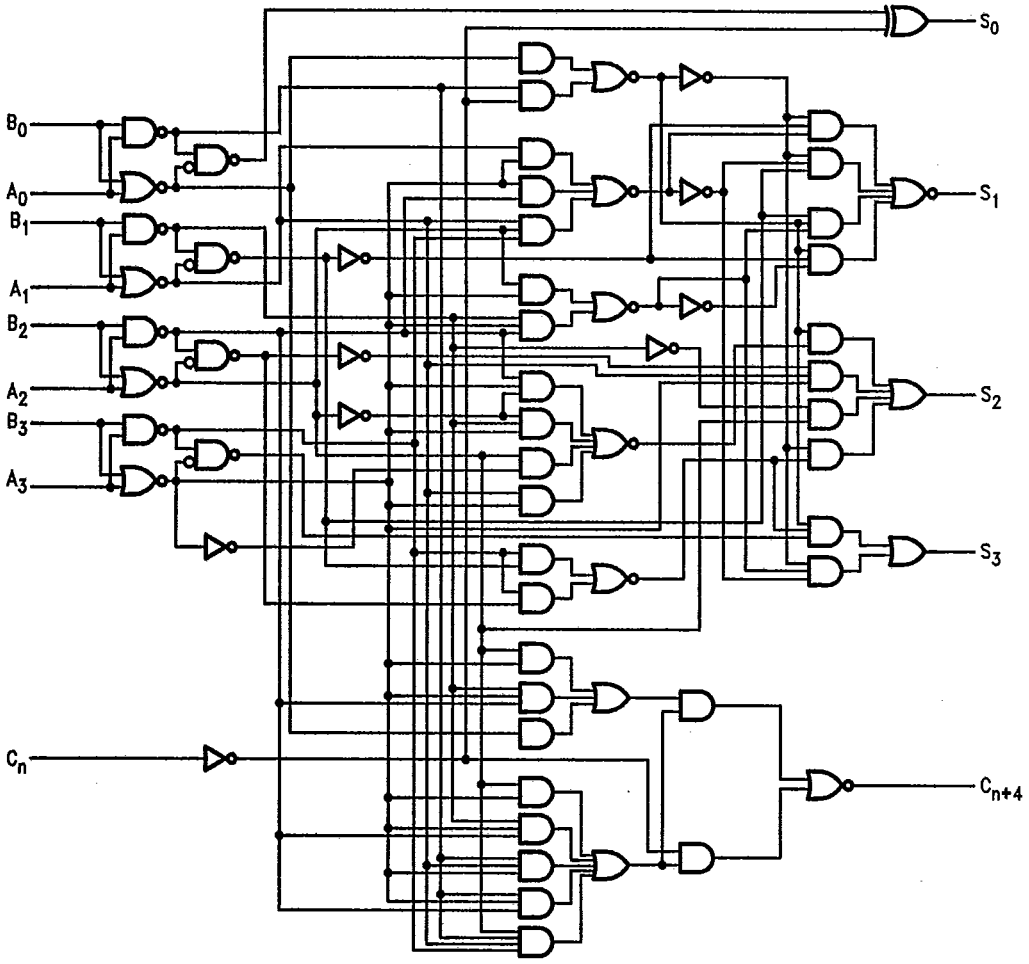
Functional Description

The 'F583 4-bit binary coded (BCD) full adder performs the addition of two decimal numbers (A_0–A_3, B_0–B_3). The look-ahead generates the BCD carry terms internally, allowing the 'F583 to then do BCD addition correctly. For BCD numbers 0 through 9 at A and B inputs, the BCD sum forms at the output. In the addition of two BCD numbers totalling a number greater than 9, a valid BCD number and a carry will result.

For input values larger than 9, the number is converted from binary to BCD. Binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n, and applying any 4-bit binary number to the other set of inputs. If the input is between 0 and 9, a BCD number occurs at the output. If the binary input falls between 10 and 15, a carry term is generated. Both the carry term and the sum are the BCD equivalent of the binary input. Converting binary numbers greater than 16 may be achieved through cascading 'F583s.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current				20	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				100	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (C_n)
					−1.2			V_{IN} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current				250	μA	Max	V_{OUT} = V_{CC}
I_{CCL}	Power Supply Current			40	60	mA	Max	V_O = LOW

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F $T_A, V_{CC} = Mil$, $C_L = 50$ pF		74F $T_A, V_{CC} = Com$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	13.0	16.5	2.5	20.5	2.5	17.5	ns	2-3
t_{PHL}	A_n or B_n to S_n	2.5	11.0	14.0	2.5	19.0	2.5	15.0		
t_{PLH}	Propagation Delay	2.5	6.5	8.5	2.5	10.5	2.5	9.5	ns	2-3
t_{PHL}	C_n to C_{n+4}	2.5	5.0	6.5	2.5	8.5	2.5	7.5		
t_{PLH}	Propagation Delay	4.0	11.0	14.0	4.0	19.5	4.0	15.0	ns	2-3
t_{PHL}	A_n or B_n to C_{n+4}	4.0	8.0	10.5	4.0	13.5	4.0	11.5		