Freescale Semiconductor
Advance Information

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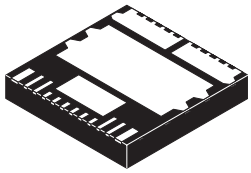
Single Intelligent High-Current Self-Protected Silicon High-Side Switch (2.0 mΩ)

33982B

HIGH-SIDE SWITCH



Bottom View

PNA SUFFIX
98ARL10521D
16-PIN PQFN

The 33982B is a self-protected silicon 2.0 mΩ high-side switch used to replace electromechanical relays, fuses, and discrete devices in power management applications. The 33982B is designed for harsh environments, and it includes self-recovery features. The device is suitable for loads with high inrush current, as well as motors and all types of resistive and inductive loads.

Programming, control, and diagnostics are implemented via the Serial Peripheral Interface (SPI). A dedicated parallel input is available for alternate and Pulse Width Modulation (PWM) control of the output. SPI programmable fault trip thresholds allow the device to be adjusted for optimal performance in the application.

The 33982B is packaged in a power-enhanced 12 x 12 nonleaded PQFN package with exposed tabs.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33982BPNA/R2	-40°C to 125°C	16 PQFN

Features

- Single 2.0 mΩ Max High-Side Switch with Parallel Input or SPI Control
- 6.0 V to 27 V Operating Voltage with Standby Currents < 5.0 µA
- Output Current Monitoring with Two SPI-Selectable Current Ratios
- SPI Control of Overcurrent Limit, Overcurrent Fault Blanking Time, Output-OFF Open Load Detection, Output ON/OFF Control, Watchdog Time-out, Slew Rates, and Fault Status Reporting
- SPI Status Reporting of Overcurrent, Open and Shorted Loads, Overtemperature Shutdown, Undervoltage and Overvoltage Shutdown, Fail-Safe Pin Status, and Program Status
- Enhanced -16 V Reverse Polarity V_{PWR} Protection

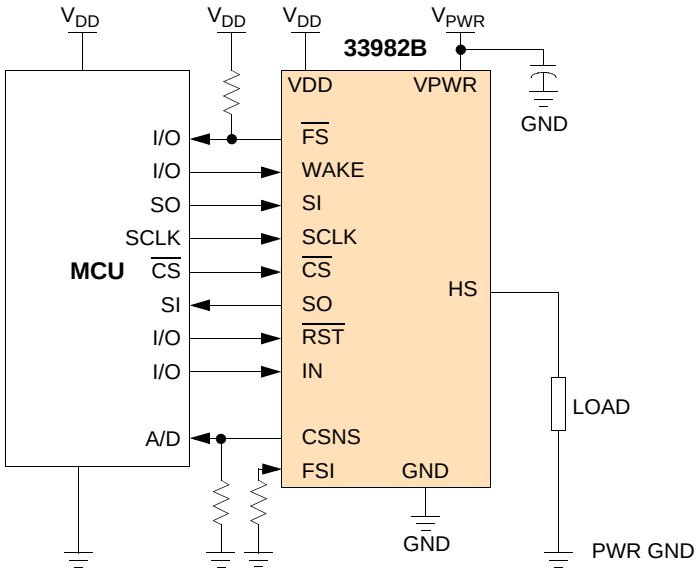


Figure 1. 33982B Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

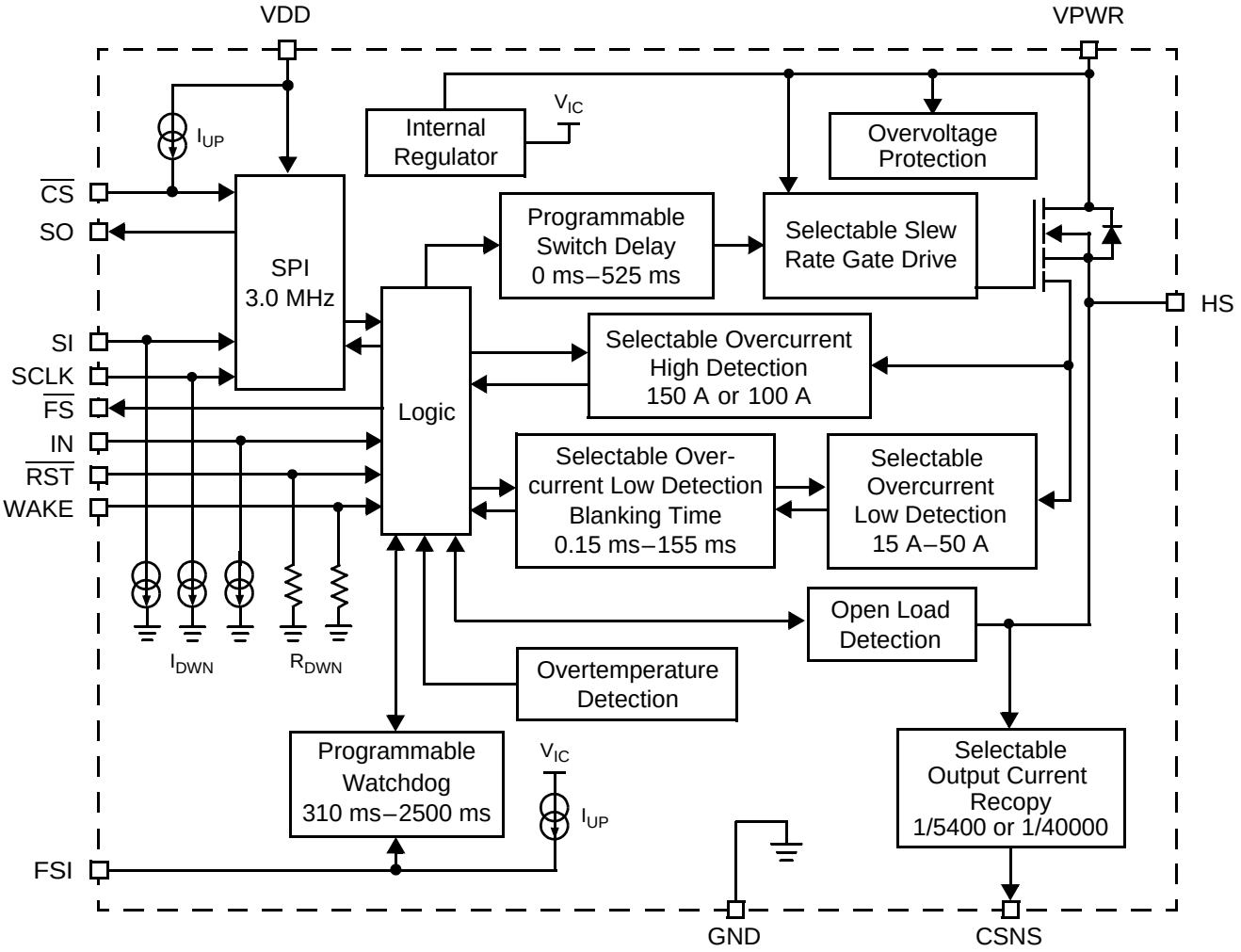


Figure 2. 33982B Simplified Internal Block Diagram

PIN CONNECTIONS

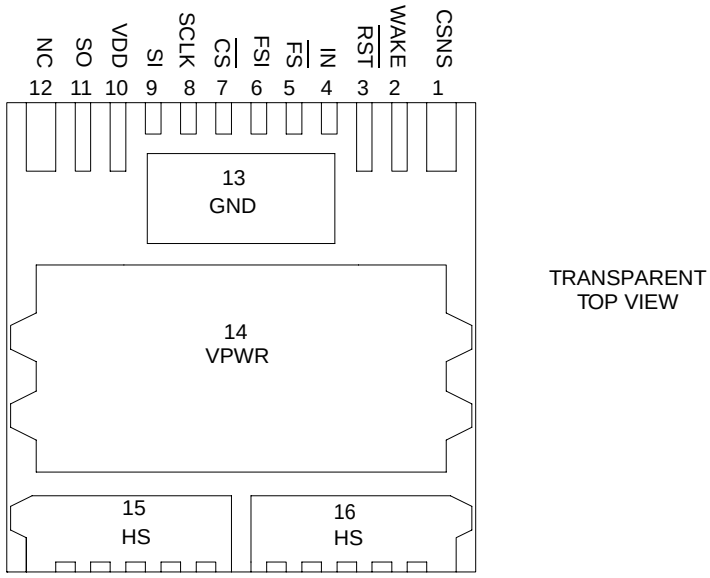


Figure 3. 33982B Pin Connections

Table 1. Pin Definitions

Functional descriptions of many of these pins can be found in the Functional Pin Description section beginning on page 15.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	CSNS	Output	Output Current Monitoring	This pin is used to output a current proportional to the high-side output current and used externally to generate a ground-referenced voltage for the microcontroller to monitor output current.
2	WAKE	Input	Wake	This pin is used to input a Logic [1] signal in order to enable the watchdog timer function.
3	$\overline{RST}$	Input	Reset (Active Low)	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low current sleep mode.
4	IN	Input	Direct Input	The Input pin is used to directly control the output.
5	$\overline{FS}$	Output	Fault Status (Active Low)	This is an open drain configured output requiring an external pullup resistor to V_{DD} for fault reporting.
6	FSI	Input	Fail-Safe Input	The value of the resistance connected between this pin and ground determines the state of the output after a watchdog time-out occurs.
7	$\overline{CS}$	Input	Chip Select (Active Low)	This input pin is connected to a chip select output of a master microcontroller (MCU).
8	SCLK	Input	Serial Clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication.
9	SI	Input	Serial Input	This is a command data input pin connected to the SPI Serial Data Output of the MCU or to the SO pin of the previous device in a daisy chain of devices.
10	VDD	Input	Digital Drain Voltage (Power)	This is an external voltage input pin used to supply power to the SPI circuit.

Table 1. Pin Definitions (continued)

Functional descriptions of many of these pins can be found in the Functional Pin Description section beginning on page 15.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
11	SO	Output	Serial Output	This output pin is connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device in a daisy chain of devices.
12	NC	NC	No Connect	This pin may not be connected.
13	GND	Ground	Ground	This pin is the ground for the logic and analog circuitry of the device.
14	VPWR	Input	Positive Power Supply	This pin connects to the positive power supply and is the source input of operational power for the device.
15, 16	HS	Output	High-Side Output	Protected high-side power output to the load. Output pins must be connected in parallel for operation.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Operating Voltage Range Steady-State	V_{PWR}	 -16 to 41	V
V_{DD} Supply Voltage	V_{DD}	-0.3 to 5.5	V
Input/Output Voltage (1)	V_{IN}, $\overline{RST}$, FSI, CSNS, SI, SCLK, $\overline{CS}$, $\overline{FS}$	-0.3 to 7.0	V
SO Output Voltage (1)	V_{SO}	-0.3 to V_{DD}+0.3	V
WAKE Input Clamp Current	$I_{CL(WAKE)}$	2.5	mA
CSNS Input Clamp Current	$I_{CL(CSNS)}$	10	mA
Output Current (2)	I_{HS}	60	A
Output Voltage Positive Negative	V_{HS}	 41 -15	V
Output Clamp Energy (3)	E_{CL}	1.5	J
ESD Voltage (4) Human Body Model (HBM) Charge Device Model (CDM) Corner Pins (1, 12, 15, 16) All Other Pins (2, 11, 13, 14)	 V_{ESD1} V_{ESD3}	 ±2000 ±750 ±500	V

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Operating Temperature			°C
Ambient	T_A	-40 to 125	
Junction	T_J	-40 to 150	
Storage Temperature	T_{STG}	-55 to 150	°C
Thermal Resistance (5)			°C/W
Junction-to-Case	$R_{\theta JC}$	<1.0	
Junction-to-Ambient	$R_{\theta JA}$	20	
Peak Package Reflow Temperature During Reflow (6), (7)	T_{PPRT}	Note 7	°C

Notes

1. Exceeding this voltage limit may cause permanent damage to the device.
2. Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
3. Active clamp energy using single-pulse method (L = 16 mH, R_L = 0, V_{PWR} = 12 V, T_J = 150°C).
4. ESD1 testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω); ESD3 testing is performed in accordance with the Charge Device Model (CDM), Robotic (Czap = 4.0 pF).
5. Device mounted on a 2s2p test board per JEDEC JESD51-2.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
   Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Battery Supply Voltage Range Full Operational	V_{PWR}	 6.0	 –	 27	V
V_{PWR} Operating Supply Current Output ON, I_{HS} = 0 A	$I_{PWR(ON)}$	 –	 –	 20	mA
VPWR Supply Current Output OFF, Open Load Detection Disabled, WAKE > 0.7 V_{DD}, $\overline{RST}$ = $V_{LOGIC\ HIGH}$	$I_{PWR(SBY)}$	 –	 –	 5.0	mA
Sleep State Supply Current (V_{PWR} < 14 V, $\overline{RST}$ < 0.5 V, WAKE < 0.5 V) T_J = 25°C T_J = 85°C	$I_{PWR(SLEEP)}$	 – –	 – –	 10 50	µA
VDD Supply Voltage	$V_{DD(ON)}$	4.5	5.0	5.5	V
VDD Supply Current No SPI Communication 3.0 MHz SPI Communication	$I_{DD(ON)}$	 – –	 – –	 1.0 5.0	mA
VDD Sleep State Current	$I_{DD(SLEEP)}$	–	–	5.0	µA
Overvoltage Shutdown Threshold	$V_{PWR(OV)}$	28	32	36	V
Overvoltage Shutdown Hysteresis	$V_{PWR(OVHYS)}$	0.2	0.8	1.5	V
Undervoltage Output Shutdown Threshold (8)	$V_{PWR(UV)}$	5.0	5.5	6.0	V
Undervoltage Hysteresis (9)	$V_{PWR(UVHYS)}$	–	0.25	–	V
Undervoltage Power-ON Reset	$V_{PWR(UVPOR)}$	–	–	5.0	V
POWER OUTPUT					
Output Drain-to-Source ON Resistance (I_{HS} = 30 A, T_J = 25°C) V_{PWR} = 6.0 V V_{PWR} = 10 V V_{PWR} = 13 V	$R_{DS(ON)}$	 – – –	 – – –	 3.0 2.0 2.0	mΩ
Output Drain-to-Source ON Resistance (I_{HS} = 30 A, T_J = 150°C) V_{PWR} = 6.0 V V_{PWR} = 10 V V_{PWR} = 13 V	$R_{DS(ON)}$	 – – –	 – – –	 5.1 3.4 3.4	mΩ
Output Source-to-Drain ON Resistance (I_{HS} = 30 A, T_J = 25°C) (10) V_{PWR} = -12 V	$R_{DS(ON)}$	 –	 2.0	 4.0	mΩ

Notes

8. This applies to all internal device logic that is supplied by V_{PWR} and assumes that the external V_{DD} supply is within specification.
9. This applies when the undervoltage fault is not latched (IN = 0).
10. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{PWR}.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
Output Overcurrent High Detection Levels (9.0 V ≤ V_{PWR} ≤ 16 V)					A
SOCH = 0	I_{OCH0}	120	150	180	
SOCH = 1	I_{OCH1}	80	100	120	
Overcurrent Low Detection Levels (SOCL[2:0])					A
000	I_{OCL0}	41	50	59	
001	I_{OCL1}	36	45	54	
010	I_{OCL2}	32	40	48	
011	I_{OCL3}	29	35	41	
100	I_{OCL4}	25	30	35	
101	I_{OCL5}	20	25	30	
110	I_{OCL6}	16	20	24	
111	I_{OCL7}	12	15	18	
Current Sense Ratio (9.0 V ≤ V_{PWR} ≤ 16 V, CSNS ≤ 4.5 V)					–
DICR D2 = 0	C_{SR0}	–	1/5400	–	
DICR D2 = 1	C_{SR1}	–	1/40000	–	
Current Sense Ratio (C_{SR0}) Accuracy	C_{SR0_ACC}				%
Output Current					
10 A		-20	–	20	
20 A		-14	–	14	
25 A		-13	–	13	
30 A		-12	–	12	
40 A		-13	–	13	
50 A		-13	–	13	
Current Sense Ratio (C_{SR1}) Accuracy	C_{SR1_ACC}				%
Output Current					
10 A		-25	–	25	
20 A		-19	–	19	
25 A		-18	–	18	
30 A		-17	–	17	
40 A		-18	–	18	
50 A		-18	–	18	
Current Sense Clamp Voltage	$V_{CL(CSNS)}$				V
CSNS Open, I_{HS} = 59.0 A		4.5	6.0	7.0	
Open Load Detection Current (11)	I_{OLDC}	30	–	100	µA
Output Fault Detection Threshold	$V_{OLD(THRES)}$				V
Output Programmed OFF		2.0	3.0	4.0	

Notes

11. Output OFF Open Load Detection Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
Output Negative Clamp Voltage 0.5 A ≤ I_{HS} ≤ 2.0 A, Output OFF	V_{CL}	 -20	 –	 -15	V
Overtemperature Shutdown (12)	T_{SD}	160	175	190	°C
Overtemperature Shutdown Hysteresis (12)	$T_{SD(HYS)}$	5.0	–	20	°C
CONTROL INTERFACE					
Input Logic High Voltage (13)	V_{IH}	0.7 V_{DD}	–	–	V
Input Logic Low Voltage (13)	V_{IL}	–	–	0.2V_{DD}	V
Input Logic Voltage Hysteresis (14)	$V_{IN(HYS)}$	100	600	1200	mV
Input Logic Pulldown Current (SCLK, IN, SI)	I_{DWN}	5.0	–	20	µA
$\overline{RST}$ Input Voltage Range	V_{RST}	4.5	5.0	5.5	V
SO, $\overline{FS}$ Tri-State Capacitance (15)	C_{SO}	–	–	20	pF
Input Logic Pulldown Resistor ($\overline{RST}$) and WAKE	R_{DWN}	100	200	400	kΩ
Input Capacitance (15)	C_{IN}	–	4.0	12	pF
WAKE Input Clamp Voltage (16) $I_{CL(WAKE)}$ < 2.5 mA	$V_{CL(WAKE)}$	 7.0	 –	 14	V
WAKE Input Forward Voltage $I_{CL(WAKE)}$ = -2.5 mA	$V_{F(WAKE)}$	 -2.0	 –	 -0.3	V
SO High-State Output Voltage I_{OH} = 1.0 mA	V_{SOH}	 0.8V_{DD}	 –	 –	V
$\overline{FS}$, SO Low-State Output Voltage I_{OL} = -1.6 mA	V_{SOL}	 –	 0.2	 0.4	V
SO Tri-State Leakage Current $\overline{CS}$ ≥ 0.7 V_{DD}	$I_{SO(LEAK)}$	 -5.0	 0.0	 5.0	µA
Input Logic Pullup Current (17) $\overline{CS}$, V_{IN} > 0.7V_{DD}	I_{UP}	 5.0	 –	 20	µA
FSI Input Pin External Pulldown Resistance FSI Disabled, HS Indeterminate FSI Enabled, HS OFF FSI Enabled, HS ON	RFS RFSdis RFSoff RFSon	 – 6.0 30	 0.0 10 –	 1.0 14 –	kΩ

Notes

12. Guaranteed by process monitoring. Not production tested.
13. Upper and lower logic threshold voltage range applies to SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN, and WAKE input signals. The WAKE and $\overline{RST}$ signals may be supplied by a derived voltage reference to V_{PWR}.
14. No hysteresis on FSI and wake pins. Parameter is guaranteed by process monitoring but is not production tested.
15. Input capacitance of SI, $\overline{CS}$, SCLK, $\overline{RST}$, and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
16. The current must be limited by a series resistance when using voltages > 7.0 V.
17. Pullup current is with $\overline{CS}$ OPEN. $\overline{CS}$ has an active internal pullup to V_{DD}.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_A ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING					
Output Rising Slow Slew Rate A (DICR D3 = 0) (18) 9.0 V < V_{PWR} < 16 V	SR_{RA_SLOW}	0.2	0.6	1.2	V/µs
Output Rising Slow Slew Rate B (DICR D3 = 0) (19) 9.0 V < V_{PWR} < 16 V	SR_{RB_SLOW}	0.03	0.1	0.3	V/µs
Output Rising Fast Slew Rate A (DICR D3 = 1) (18) 9.0 V < V_{PWR} < 16 V	SR_{RA_FAST}	0.4	1.0	4.0	V/µs
Output Rising Fast Slew Rate B (DICR D3 = 1) (19) 9.0 V < V_{PWR} < 16 V	SR_{RB_FAST}	0.03	0.1	1.2	V/µs
Output Falling Slow Slew Rate A (DICR D3 = 0) (18) 9.0 V < V_{PWR} < 16 V	SR_{FA_SLOW}	0.2	0.6	1.2	V/µs
Output Falling Slow Slew Rate B (DICR D3 = 0) (19) 9.0 V < V_{PWR} < 16 V	SR_{FB_SLOW}	0.03	0.1	0.3	V/µs
Output Falling Fast Slew Rate A (DICR D3 = 1) (18) 9.0 V < V_{PWR} < 16 V	SR_{FA_FAST}	0.8	2.0	4.0	V/µs
Output Falling Fast Slew Rate B (DICR D3 = 1) (19) 9.0 V < V_{PWR} < 16 V	SR_{FB_FAST}	0.1	0.35	1.2	V/µs
Output Turn-ON Delay Time in Fast/Slow Slew Rate (20) DICR = 0, DICR = 1	$t_{DLY(ON)}$	1.0	18	100	µs
Output Turn-OFF Delay Time in Slow Slew Rate Mode (21) DICR = 0	$t_{DLY\_SLOW(OFF)}$	20	230	500	µs
Output Turn-OFF Delay Time in Fast Slew Rate Mode (21) DICR = 1	$t_{DLY\_FAST(OFF)}$	10	60	200	µs
Direct Input Switching Frequency (DICR D3 = 0)	f_{PWM}	–	300	–	Hz

Notes

18. Rise and Fall Slew Rates A measured across a 5.0 Ω resistive load at high-side output = 0.5 V to V_{PWR}-3.5 V. These parameters are guaranteed by process monitoring.
19. Rise and Fall Slow Slew Rates B measured across a 5.0 Ω resistive load at high-side output = V_{PWR}-3.5 V to V_{PWR}-0.5 V. These parameters are guaranteed by process monitoring.
20. Turn-ON delay time measured from rising edge of any signal (IN, SCLK, $\overline{CS}$) that would turn the output ON to V_{HS} = 0.5 V with R_L = 5.0 Ω resistive load.
21. Turn-OFF delay time measured from falling edge of any signal (IN, SCLK, $\overline{CS}$) that would turn the output OFF to V_{HS} = V_{PWR}-0.5 V with R_L = 5.0 Ω resistive load.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_A ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING (CONTINUED)					
Overcurrent Low Detection Blanking Time (OCLT[1:0])					ms
00	t_{OCL0}	108	155	202	
01	t_{OCL1}	7.0	10	13	
10	t_{OCL2}	0.8	1.2	1.6	
11	t_{OCL3}	0.08	0.15	0.25	
Overcurrent High Detection Blanking Time	t_{OCH}	1.0	10	20	µs
$\overline{CS}$ to CSNS Valid Time (22)	t_{CNSVAL}	–	–	10	µs
Output Switching Delay Time (OSD[2:0])					ms
000	t_{OSD0}	–	0.0	–	
001	t_{OSD1}	52	75	95	
010	t_{OSD2}	105	150	195	
011	t_{OSD3}	157	225	293	
100	t_{OSD4}	210	300	390	
101	t_{OSD5}	262	375	488	
110	t_{OSD6}	315	450	585	
111	t_{OSD7}	367	525	683	
Watchdog Time-out (WD[1:0]) (23)					ms
00	t_{WDTO0}	434	620	806	
01	t_{WDTO1}	207	310	403	
10	t_{WDTO2}	1750	2500	3250	
11	t_{WDTO3}	875	1250	1625	
SPI INTERFACE CHARACTERISTICS					
Recommended Frequency of SPI Operation	f_{SPI}	–	–	3.0	MHz
Required Low State Duration for $\overline{RST}$ (24)	$t_{W\overline{RST}}$	–	50	167	ns

Notes
22. Time necessary for the CSNS to be within ±5% of the targeted value.
23. Watchdog time-out delay measured from the rising edge of WAKE to $\overline{RST}$ from a sleep state condition to output turn-ON with the output driven OFF and FSI floating. The values shown are for WDR setting of [00]. The accuracy of t_{WDTO} is consistent for all configured watchdog timeouts.
24. $\overline{RST}$ low duration measured with outputs enabled and going to OFF or disabled condition.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_A ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE CHARACTERISTICS					
Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (25)	$t_{\overline{CS}}$	–	–	300	ns
Rising Edge of $\overline{RST}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (25)	t_{ENBL}	–	–	5.0	µs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time) (25)	t_{LEAD}	–	50	167	ns
Required High State Duration of SCLK (Required Setup Time) (25)	t_{WSCLKH}	–	–	167	ns
Required Low State Duration of SCLK (Required Setup Time) (25)	t_{WSCLKL}	–	–	167	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time) (25)	t_{LAG}	–	50	167	ns
SI to Falling Edge of SCLK (Required Setup Time) (26)	$t_{SI(SU)}$	–	25	83	ns
Falling Edge of SCLK to SI (Required Setup Time) (26)	$t_{SI(HOLD)}$	–	25	83	ns
SO Rise Time C_L = 200 pF	t_{RSO}	–	25	50	ns
SO Fall Time C_L = 200 pF	t_{FSO}	–	25	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time (26)	t_{RSI}	–	–	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time (26)	t_{FSI}	–	–	50	ns
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (27)	$t_{SO(EN)}$	–	–	145	ns
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (28)	$t_{SO(DIS)}$	–	65	145	ns
Time from Rising Edge of SCLK to SO Data Valid (29) 0.2 V_{DD} ≤ SO ≤ 0.8 V_{DD}, C_L = 200 pF	t_{VALID}	–	65	105	ns

Notes
25. Maximum setup time required for the 33982B is the minimum guaranteed time needed from the microcontroller.
26. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
27. Time required for output status data to be available for use at SO. 1.0 kΩ on pullup on $\overline{CS}$.
28. Time required for output status data to be terminated at SO. 1.0 kΩ on pullup on $\overline{CS}$.
29. Time required to obtain valid data out from SO following the rise of SCLK.

TIMING DIAGRAMS

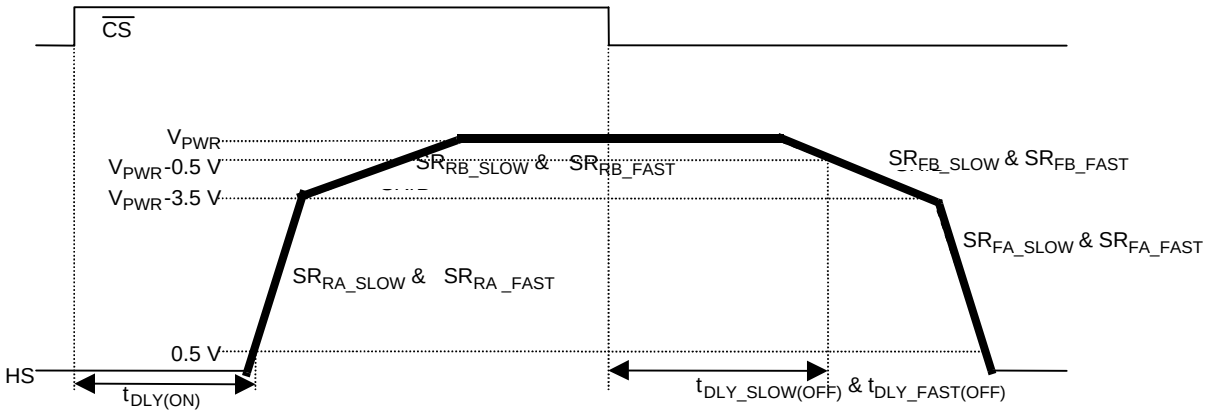


Figure 4. Output Slew Rate and Time Delays

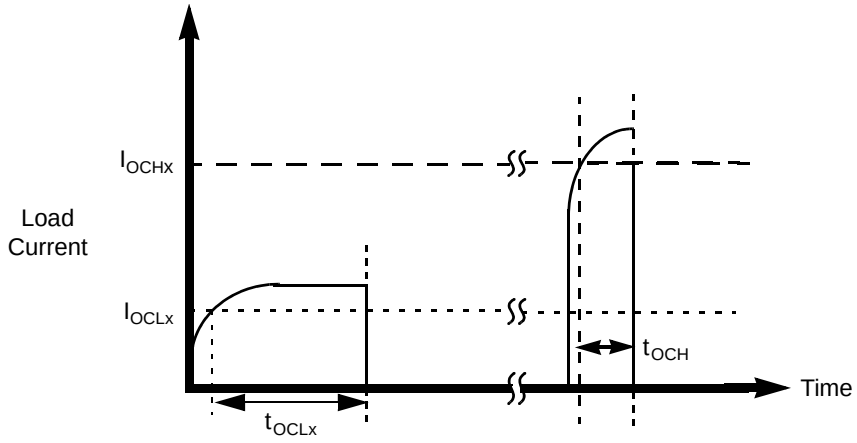


Figure 5. Overcurrent Shutdown

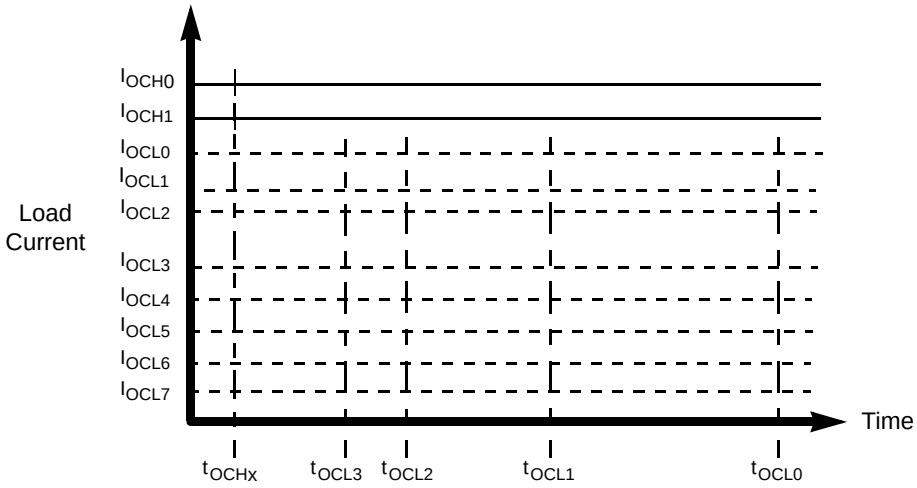


Figure 6. Overcurrent Low and High Detection

Figure 6 illustrates the overcurrent detection level (I_{OCLX}, I_{OCHX}) the device can reach for each overcurrent detection blanking time (t_{OCHX}, t_{OCLX}):

- During t_{OCHX}, the device can reach up to Ioch0 overcurrent level.
- During t_{OCL3} or t_{OCL2} or t_{OCL1} or t_{OCL0}, the device can be programmed to detect up to Iocl0.

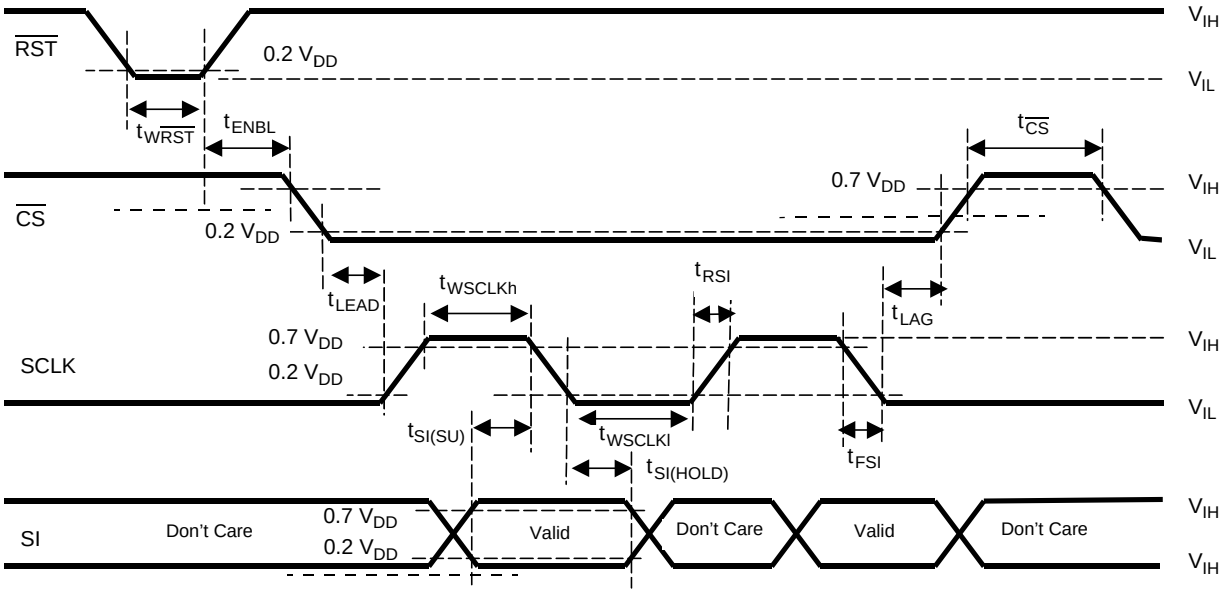


Figure 7. Input Timing Switching Characteristics

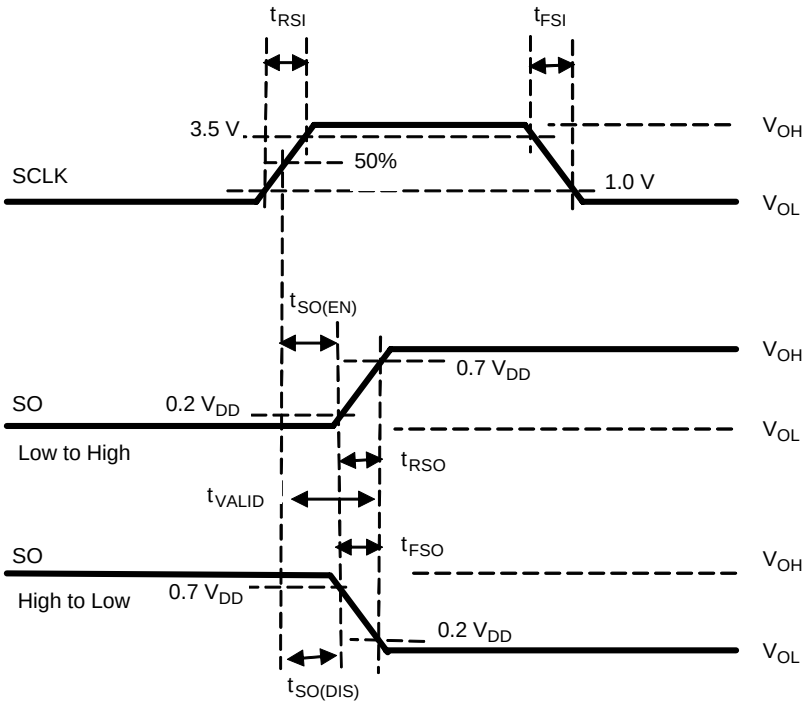


Figure 8. SCLK Waveform and Valid SO Data Delay Time

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33982B is a self-protected silicon 2.0 mΩ high-side switch used to replace electromechanical relays, fuses, and discrete devices in power management applications. The 33982B is designed for harsh environments, including self-recovery features. The device is suitable for loads with high inrush current, as well as motors and all types of resistive and inductive loads.

Programming, control, and diagnostics are implemented via the Serial Peripheral Interface (SPI). A dedicated parallel input is available for alternate and pulse width modulation (PWM) control of the output. SPI programmable fault trip thresholds allow the device to be adjusted for optimal performance in the application.

The 33982B is packaged in a power-enhanced 12 x 12 nonleaded PQFN package with exposed tabs.

FUNCTIONAL PIN DESCRIPTION

OUTPUT CURRENT MONITORING (CSNS)

The CSNS pin outputs a current proportional to the high-side output current and used externally to generate a ground-referenced voltage for the microcontroller to monitor output current.

WAKE (WAKE)

This pin is used to input a Logic [1] signal in order to enable the watchdog timer function. An internal clamp protects this pin from high damaging voltages when the output is current limited with an external resistor. This input has a passive internal pulldown.

RESET ($\overline{\text{RST}}$)

This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low current sleep mode. The pin also starts the watchdog timer when transitioning from logic LOW to logic HIGH. This pin should not be allowed to be logic HIGH until V_{DD} is in regulation. This pin has a passive internal pulldown.

DIRECT IN (IN)

The Input pin is used to directly control the output. This input has an active internal pulldown current source and requires CMOS logic levels. This input may be configured via SPI.

FAULT STATUS ($\overline{\text{FS}}$)

This is an open drain configured output requiring an external pullup resistor to V_{DD} for fault reporting. When a device fault condition is detected, this pin is active LOW. Specific device diagnostic faults are reported via the SPI SO pin.

FAIL-SAFE INPUT (FSI)

The value of the resistance connected between this pin and ground determines the state of the output after a watchdog time-out occurs. Depending on the resistance value, either the output is OFF or ON. When the FSI pin is connected to GND, the watchdog circuit and fail-safe operation are disabled. This pin incorporates an active internal pullup current source.

CHIP SELECT ($\overline{\text{CS}}$)

This input pin is connected to a chip select output of a master microcontroller (MCU). The MCU determines which device is addressed (selected) to receive data by pulling the $\overline{\text{CS}}$ pin of the selected device logic LOW, enabling SPI communication with the device. Other *unselected* devices on the serial link having their $\overline{\text{CS}}$ pins pulled up logic HIGH disregard the SPI communication data sent. This pin incorporates an active internal pullup current source.

SERIAL CLOCK (SCLK)

This input pin is connected to the MCU providing the required bit shift clock for SPI communication. It transitions one time per bit transferred at an operating frequency, f_{SPI}, defined by the communication interface. The 50 percent duty cycle CMOS-level serial clock signal is idle between command transfers. The signal is used to shift data into and out of the device. This input has an active internal pulldown current source.

SERIAL INTERFACE (SI)

This is a command data input pin connected to the SPI Serial Data Output of the MCU or to the SO pin of the previous device in a daisy chain of devices. The input requires CMOS logic level signals and incorporates an active internal pulldown current source. Device control is facilitated by the input's receiving the MSB first of a serial 8-bit control command. The MCU ensures data is available upon the falling edge of SCLK. The logic state of SI present upon the rising edge of SCLK loads that bit command into the internal command shift register.

DIGITAL DRAIN VOLTAGE POWER (VDD)

This is an external voltage input pin used to supply power to the SPI circuit. In the event V_{DD} is lost, an internal supply provides power to a portion of the logic, ensuring limited functionality of the device. All device configuration registers are reset.

SERIAL OUTPUT (SO)

This output pin is connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device in a daisy chain of devices. This output will remain tri-stated (high impedance OFF condition) so long as the $\overline{CS}$ pin of the device is logic HIGH. SO is only active when the $\overline{CS}$ pin of the device is asserted logic LOW. The generated SO output signals are CMOS logic levels. SO output data is available on the falling edge of SCLK and transitions immediately on the rising edge of SCLK.

POSITIVE POWER SUPPLY (VPWR)

This pin connects to the positive power supply and is the source input of operational power for the device. The VPWR pin is a backside surface mount tab of the package.

HIGH-SIDE OUTPUT (HS)

This pin protects high-side power output to the load. Output pins must be connected in parallel for operation.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

The 33982B has four operating modes: Sleep, Normal, Fault, and Fail-Safe. Table 5 summarizes details contained in succeeding paragraphs.

Table 5. Fail-Safe Operation and Transitions to Other 33982B Modes

Mode	$\overline{FS}$	WAKE	RST	WDTO	Comments
Sleep	x	0	0	x	Device is in Sleep mode. All outputs are OFF.
Normal	1	x	1	No	Normal mode. Watchdog is active if enabled.
Fault	0	1	x	No	The device is currently in Fault mode. The faulted output is OFF.
	0	x	1		
Fail-Safe	1	0	1	Yes	Watchdog has timed out and the device is in Fail-Safe mode. The output is as configured with the RFS resistor connected to FSI. $\overline{RST}$ and WAKE must be transitioned to Logic [0] simultaneously to bring the device out of the Fail-Safe mode or momentarily tied the FSI pin to ground.
	1	1	1		
	1	0	1		
	1	1	0		

x = Don't care.

SLEEP MODE

The default mode of the 33982B is the Sleep mode. This is the state of the device after first applying battery voltage (V_{PWR}), prior to any I/O transitions. This is also the state of the device when the WAKE and $\overline{RST}$ are both Logic [0]. In the Sleep mode, the output and all unused internal circuitry, such as the internal 5.0 V regulator, are off to minimize current draw. In addition, all SPI-configurable features of the device are as if set to Logic [0]. The device will transition to the Normal or Fail-Safe operating modes based on the WAKE and $\overline{RST}$ inputs as defined in Table 5.

NORMAL MODE

The 33982B is in Normal mode when:

- V_{PWR} is within the normal voltage range.
- $\overline{RST}$ pin is Logic [1].
- No fault has occurred.

FAIL-SAFE MODE AND WATCHDOG

If the FSI input is not grounded, the watchdog time-out detection is active when either the WAKE or $\overline{RST}$ input pin transitions from Logic [0] to Logic [1]. The WAKE input is capable of being pulled up to V_{PWR} with a series of limiting resistance that limits the internal clamp current.

The watchdog time-out is a multiple of an internal oscillator and is specified in Table 14. As long as the WD bit (D7) of an incoming SPI message is toggled within the minimum watchdog time-out period (WDTO), based on the programmed value of the WDR the device will operate normally. If an internal watchdog time-out occurs before the WD bit, the device will revert to a Fail-Safe mode until the device is reinitialized.

During the Fail-Safe mode, the output will be ON or OFF depending upon the resistor RFS connected to the FSI pin, regardless of the state of the various direct inputs and modes (Table 6). In this mode, the SPI register content is retained except for overcurrent high and low detection levels and timing, which are reset to their default value (SOCL, SOCH, OCLT). The watchdog, overvoltage, overtemperature, and overcurrent circuitry (with default value for this one) are fully operational.

Table 6. Output State During Fail-Safe Mode

RFS (kΩ)	High-Side State
0	Fail-Safe Mode Disabled
10	HS OFF
30	HS ON

The Fail-Safe mode can be detected by monitoring the WDTO bit D2 of the WDR register. This bit is Logic [1] when the device is in Fail-Safe mode. The device can be brought out of the Fail-Safe mode by transitioning the WAKE and $\overline{RST}$ pins from Logic [1] to Logic [0] or forcing the FSI pin to Logic [0]. Table 5 summarizes the various methods for resetting the device from the latched Fail-Safe mode.

If the FSI pin is tied to GND, the Watchdog fail-safe operation is disabled.

LOSS OF V_{DD}

If the external 5.0 V supply is not within specification, or even disconnected, all register content is reset. The output can still be driven by the direct input IN. The 33982B uses the battery input to power the output MOSFET-related current sense circuitry and any other internal Logic, providing fail-safe device operation with no V_{DD} supplied. In this state, the watchdog, overvoltage, overtemperature, and overcurrent circuitry are fully operational with default values. Current recopy is active with the default current recopy value.

FAULT MODE

The 33982B indicates the following faults as they occur by driving the $\overline{FS}$ pin to Logic [0]:

- Overtemperature fault
- Overvoltage and undervoltage fault
- Open load fault
- Overcurrent fault (high and low)

The $\overline{FS}$ pin will automatically return to Logic [1] when the fault condition is removed, except for overcurrent and in some cases undervoltage.

Fault information is retained in the fault register and is available (and reset) via the SO pin during the first valid SPI communication (refer to Table 16).

PROTECTION AND DIAGNOSIS FEATURES

OVERTEMPERATURE FAULT (NON-LATCHING)

The 33982B incorporates overtemperature detection and shutdown circuitry in the output structure. Overtemperature detection is enabled when the output is in the ON state.

For the output, an overtemperature fault (OTF) condition results in the faulted output turning OFF until the temperature falls below the $T_{SD(HYS)}$. This cycle will continue indefinitely until action is taken by the MCU to shut OFF the output, or until the offending load is removed.

When experiencing this fault, the OTF fault bit will be set in the status register and cleared after either a valid SPI read or a power reset of the device.

OVERVOLTAGE FAULT (NON-LATCHING)

The 33982B shuts down the output during an overvoltage fault (OVF) condition on the V_{PWR} pin. The output remains in the OFF state until the overvoltage condition is removed. When experiencing this fault, the OVF fault bit is set in bit OD1 and cleared after either a valid SPI read or a power reset of the device.

The overvoltage protection and diagnostic can be disabled through SPI (bit OV_dis).

UNDERVOLTAGE SHUTDOWN (LATCHING OR NON-LATCHING)

The output(s) will latch off at some battery voltage below 6.0 V. As long as the V_{DD} level stays within the normal specified range, the internal logic states within the device will be sustained.

In the case where battery voltage drops below the undervoltage threshold (VPWRUV) output will turn off, $\overline{FS}$ will go to Logic [0], and the fault register UVF bit will be set to 1.

Two cases need to be considered when the battery level recovers:

- If output(s) command is (are) low, $\overline{FS}$ will go to Logic [1] but the UVF bit will remain set to 1 until the next read operation.
- If the output command is ON, then $\overline{FS}$ will remain at Logic [0]. The output must be turned OFF and ON again to re-enable the state of output and release $\overline{FS}$. The UVF bit will remain set to 1 until the next read operation.

The undervoltage protection can be disabled through SPI (bit UV_dis = 1). In this case, the $\overline{FS}$ and UVF bit do not report any undervoltage fault condition and the output state will not be changed as long as the battery voltage does not drop any lower than 2.5 V.

OPEN LOAD FAULT (NON-LATCHING)

The 33982B incorporates open load detection circuitry on the output. Output open load fault (OLF) is detected and reported as a fault condition when the output is disabled (OFF). The open load fault is detected and latched into the status register after the internal gate voltage is pulled low enough to turn OFF the output. The OLF fault bit is set in the status register. If the open load fault is removed, the status register will be cleared after reading the register.

The open load protection can be disabled through SPI (bit OL_dis). It is recommended to disable the open load detection circuitry (OL_dis bit sets to logic [1]) in case of a permanent open load fault condition.

OVERCURRENT FAULT (LATCHING)

The 33982B has eight programmable overcurrent low detection levels (I_{OCL}) and two programmable overcurrent high detection levels (I_{OCH}) for maximum device protection. The two selectable, simultaneously active overcurrent detection levels, defined by I_{OCH} and I_{OCL}, are illustrated in Figure 6. The eight different overcurrent low detection levels (I_{OCL0}:I_{OCL7}) are likewise illustrated in Figure 6.

If the load current level ever reaches the selected overcurrent low detection level and the overcurrent condition exceeds the programmed overcurrent time period (t_{OCx}), the device will latch the output OFF.

If at any time the current reaches the selected I_{OCH} level, then the device will immediately latch the fault and turn OFF the output, regardless of the selected t_{OCL} driver.

For both cases, the device output will stay off indefinitely until the device is commanded OFF and then ON again.

Table 7. Device Behavior in Case of Undervoltage

SPSS (VPWR Batter Voltage)**	State	UV Enable IN=0 (Falling VPWR)	UV Enable IN=0 (Rising VPWR)	UV Enable IN=1 (Falling VPWR)	UV Enable IN=1 (Rising VPWR)	UV Disable IN=X (Falling or Rising VPWR)
VPWR > VPWRUV	Output State	OFF	OFF	ON	OFF	OFF
	$\overline{FS}$ State	1	1	1	0	1
	SPI Fault Register UVF Bit	0	1 until next read	0	1	0
VPWRUV > VPWR > UVPOR	Output State	OFF	OFF	OFF	OFF	OFF
	$\overline{FS}$ State	0	0	0	0	1
	SPI Fault Register UVF Bit	1	1 until next read	1	1	0
UVPOR > VPWR > 2.5 V*	Output State	OFF	OFF	OFF	OFF	OFF
	$\overline{FS}$ State	1	1	1	1	1
	SPI Fault Register UVF Bit	1 until next read	1 until next read	1 until next read	1 until next read	0
2.5 V > VPWR > 0V	Output State	OFF	OFF	OFF	OFF	OFF
	$\overline{FS}$ State	1	1	1	1	1
	SPI Fault Register UVF Bit	1 until next read	1 until next read	1 until next read	1 until next read	0
	Comments	UV fault is not latched	UV fault is not latched		UV fault is latched	

* Typical value; not guaranteed
** While VDD remains within specified range.

REVERSE BATTERY

The output survives the application of reverse voltage as low as -16 V. Under these conditions, the output's gate is enhanced to keep the junction temperature less than 150°C. The ON resistance of the output is fairly similar to that in the Normal mode. No additional passive components are required.

GROUND DISCONNECT PROTECTION

In the event the 33982B ground is disconnected from load ground, the device protects itself and safely turns OFF the output regardless the state of the output at the time of disconnection. A 10 k resistor needs to be added between the wake pin and the rest of the circuitry in order to ensure that the device turns off in case of ground disconnect and to prevent this pin to exceed its maximum ratings.

FUNCTIONAL DEVICE OPERATION

LOGIC COMMANDS AND REGISTERS

SPI PROTOCOL DESCRIPTION

The SPI interface has a full duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Clock (SCLK), Serial Input (SI), Serial Output (SO), and Chip Select ($\overline{CS}$).

The SI/SO pins of the 33982B follow a first-in first-out (D7/D0) protocol with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V CMOS logic levels.

The SPI lines perform the following functions:

SERIAL CLOCK (SCLK)

The SCLK pin clocks the internal shift registers of the 33982B device. The serial input pin (SI) accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (SO) shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important that the SCLK pin be in a logic LOW state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended that the SCLK pin be in a Logic [0] state whenever the device is not accessed ($\overline{CS}$ Logic [1] state). SCLK has an active internal pulldown, I_{DWN}. When $\overline{CS}$ is Logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high impedance). (See Figure 9 and Figure 10.)

SERIAL INTERFACE (SI)

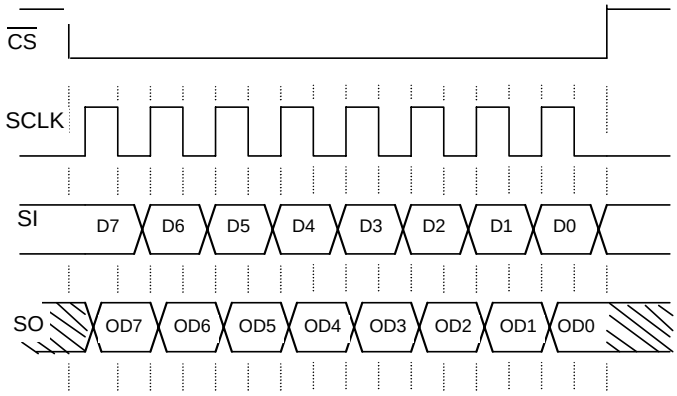
This is a serial interface (SI) command data input pin. SI instruction is read on the falling edge of SCLK. An 8-bit stream of serial data is required on the SI pin, starting with D7 to D0. The internal registers of the 33982B are configured and controlled using a 4-bit addressing scheme, as shown in Table 8. Register addressing and configuration are described in Table 9. The SI input has an active internal pulldown, I_{DWN}.

SERIAL OUTPUT (SO)

The SO pin is a tri-stateable output from the shift register. The SO pin remains in a high-impedance state until the $\overline{CS}$ pin is put into a Logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, and the state of the key inputs. The SO pin changes states on the rising edge of SCLK and reads out on the falling edge of SCLK. Fault and input status descriptions are provided in Table 15.

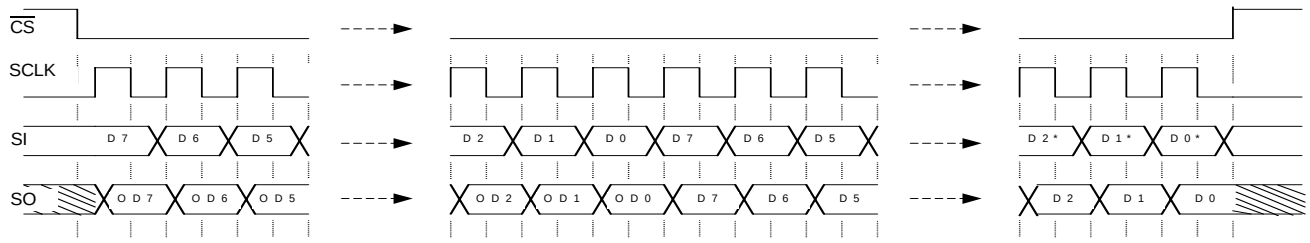
CHIP SELECT ($\overline{CS}$)

The $\overline{CS}$ pin enables communication with the master microcontroller (MCU). When this pin is in a Logic [0] state, the device is capable of transferring information to and receiving information from the MCU. The 33982B latches in data from the input shift registers to the addressed registers on the rising edge of $\overline{CS}$. The device transfers status information from the power output to the shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is Logic [0]. $\overline{CS}$ should transition from a Logic [1] to a Logic [0] state only when SCLK is a Logic [0]. $\overline{CS}$ has an active internal pullup, I_{UP}.



Notes 1. $\overline{RST}$ is a Logic [1] state during the above operation.
2. D7:D0 relate to the most recent ordered entry of data into the device.
3. OD7:OD0 relate to the first 8 bits of ordered fault and status data out of the device.

Figure 9. Single 8-Bit Word SPI Communication



Notes 1. $\overline{RST}$ is a Logic [1] state during the above operation.
2. D7:D0 relate to the most recent ordered entry of data into the device.
3. D7*:D0* relate to the previous 8 bits (last command word) of data that was previously shifted into the device.
4. OD7:OD0 relate to the first 8 bits of ordered fault and status data out of the device.

Figure 10. Multiple 8-Bit Word SPI Communication

SERIAL INPUT COMMUNICATION

SPI communication is accomplished using 8-bit messages. A message is transmitted by the MCU starting with the MSB, D7, and ending with the LSB, D0 (Table 8). Each incoming command message on the SI pin can be interpreted using the following bit assignments: the MSB (D7) is the watchdog bit and in some cases a register address bit; the next three bits, D6:D4, are used to select the command register; and the remaining four bits, D3:D0, are used to configure and control the output and its protection features.

Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable or to confirm transmitted data as long as the messages are all multiples of eight bits. Any attempt made to latch in a message that is not eight bits will be ignored.

The 33982B has defined registers, which are used to configure the device and to control the state of the output.

Table 9, summarizes the SI registers. The registers are addressed via D6:D4 of the incoming SPI word (Table 8).

Table 8. SI Message Bit Assignment

Bit Sig	SI Msg Bit	Message Bit Description
MSB	D7	Watchdog in: toggled to satisfy watchdog requirements; also used as a register address bit.
	D6:D4	Register address bits.
	D3:D1	Used to configure the inputs, outputs, and the device protection features and SO status content.
LSB	D0	Used to configure the inputs, outputs, and the device protection features and SO status content.

Table 9. Serial Input Address and Configuration Bit Map

SI Register	Serial Input Data							
	D7	D6	D5	D4	D3	D2	D1	D0
STATR	x	0	0	0	0	SOA2	SOA1	SOA0
OCR	x	0	0	1	0	0	CSNS $\overline{\text{EN}}$	IN_SPI
SOCHLR	x	0	1	0	SOCH	SOCL2	SOCL1	SOCL0
CDTOLR	x	0	1	1	OL_dis	CD_dis	OCLT1	OCLT0
DICR	x	1	0	0	FAST SR	CSNS high	IN dis	A/O
OSDR	0	1	0	1	0	OSD2	OSD1	OSD0
WDR	1	1	0	1	0	0	WD1	WD0
NAR	0	1	1	0	0	0	0	0
UOVR	1	1	1	0	0	0	UV_dis	OV_dis
TEST	x	1	1	1	Freescale Internal Use (Test)			

x = Don't care.

DEVICE REGISTER ADDRESSING

The following section describes the possible register addresses and their impact on device operation.

Address x000—Status Register (STATR)

The STATR register is used to read the device status and the various configuration register contents without disrupting the device operation or the register contents. The register bits D2, D1, and D0 determine the content of the first eight bits of SO data. In addition to the device status, this feature provides the ability to read the content of the OCR, SOCHLR, CDTOLR, DICR, OSDR, WDR, NAR, and UOVR registers. (Refer to the section entitled Serial Output Communication (Device Status Return Data) beginning on page 24.)

Address x001—Output Control Register (OCR)

The OCR register allows the MCU to control the output through the SPI. Incoming message bit D0 (IN_SPI) reflects the desired states of the high-side output: a Logic [1] enables the output switch and a Logic [0] turns it OFF. A Logic [1] on message bit D1 enables the Current Sense (CSNS) pin. Bits D2 and D3 must be Logic [0]. Bit D7 is used to feed the watchdog if enabled.

Address x010—Select Overcurrent High and Low Register (SOCHLR)

The SOCHLR register allows the MCU to configure the output overcurrent low and high detection levels, respectively. In addition to protecting the device, this slow blow fuse emulation feature can be used to optimize the load requirements to match system characteristics. Bits D2:D0 are used to set the overcurrent low detection level to one of eight possible levels as defined in Table 10. Bit D3 is used to set the overcurrent high detection level to one of two levels as defined in Table 11.

Table 10. Overcurrent Low Detection Levels

SOCL2 (D2)	SOCL1 (D1)	SOCL0 (D0)	Overcurrent Low Detection (Amperes)
0	0	0	50
0	0	1	45
0	1	0	40
0	1	1	35
1	0	0	30
1	0	1	25
1	1	0	20
1	1	1	15

Table 11. Overcurrent High Detection Levels

SOCH (D3)	Overcurrent High Detection (Amperes)
0	150
1	100

Address x011—Current Detection Time and Open Load Register (CDTOLR)

The CDTOLR register is used by the MCU to determine the amount of time the device will allow an overcurrent low condition before output latches OFF occurs. Bits D1 and D0 allow the MCU to select one of four fault blanking times defined in Table 12. Note that these timeouts apply only to the overcurrent low detection levels. If the selected overcurrent high level is reached, the device will latch off within 20 µs.

Table 12. Overcurrent Low Detection Blanking Time

OCLT[1:0]	Timing
00	155 ms
01	10 ms
10	1.2 ms
11	150 µs

A Logic [1] on bit D2 disables the overcurrent low (CD_dis) detection time-out feature. A Logic [1] on bit D3 disables the open load (OL) detection feature.

Address x100—Direct Input Control Register (DICR)

The DICR register is used by the MCU to enable, disable, or configure the direct IN pin control of the output. A Logic [0] on bit D1 will enable the output for direct control by the IN pin. A Logic [1] on bit D1 will disable the output from direct control. While addressing this register, if the input was enabled for

direct control, a Logic [1] for the D0 bit will result in a Boolean AND of the IN pin with its corresponding D0 message bit when addressing the OCR register. Similarly, a Logic [0] on the D0 pin will result in a Boolean OR of the IN pin with the corresponding message bits when addressing the OCR register.

The DICR register is useful if there is a need to independently turn on and off several loads that are PWM'd at the same frequency and duty cycle with only one PWM signal. This type of operation can be accomplished by connecting the pertinent direct IN pins of several devices to a PWM output port from the MCU and configuring each of the outputs to be controlled via their respective direct IN pin. The DICR is then used to Boolean AND the direct IN(s) of each of the outputs with the dedicated SPI bit that also controls the output. Each configured SPI bit can now be used to enable and disable the common PWM signal from controlling its assigned output.

A Logic [1] on bit D2 is used to select the high ratio (C_{SR1}, 1/40000) on the CSNS pin. The default value [0] is used to select the low ratio (C_{SR0}, 1/5400). A Logic [1] on bit D3 is used to select the high-speed slew rate. The default value [0] corresponds to the low speed slew rate.

Address 0101—Output Switching Delay Register (OSDR)

The OSDR register is used to configure the device with a programmable time delay that is active during Output On transitions that are initiated via SPI (not via direct input). Whenever the input is commanded to transition from Logic [0] to Logic [1], the output will be held OFF for the time delay configured in the OSDR register.

The programming of the contents of this register has no effect on device Fail-Safe mode operation. The default value of the OSDR register is 000, equating to no delay, since the switching delay time is 0 ms. This feature allows the user a way to minimize inrush currents, or surges, thereby allowing loads to be synchronously switched ON with a single command.

Table 13 shows the eight selectable output switching delay times, which range from 0 ms to 525 ms.

Table 13. Switching Delay

OSD[2:0] (D2:D0)	Turn ON Delay (ms)
000	0
001	75
010	150
011	225
100	300
101	375
110	450
111	525

Address 1101—Watchdog Register (WDR)

The WDR register is used by the MCU to configure the watchdog time-out. Watchdog time-out is configured using bits D1 and D0 (Table 14). When bits D1 and D0 are programmed for the desired watchdog time-out period, the WD bit (D7) should be toggled as well to ensure that the new time-out period is programmed at the beginning of a new count sequence.

Table 14. Watchdog Time-out

WD[1:0] (D1:D0)	Timing (ms)
00	620
01	310
10	2500
11	1250

Address 0110—No Action Register (NAR)

The NAR register can be used to no-operation fill SPI data packets in a daisy chain SPI configuration. This allows devices to not be affected by commands being clocked over a daisy-chained SPI configuration, and by toggling the WD bit (D7) the watchdog circuitry will continue to be reset while no programming or data readback functions are being requested from the device.

Address 1110—Undervoltage/Overvoltage Register (UOVR)

The UOVR register can be used to disable or enable the overvoltage and/or undervoltage protection. By default ([0]), both protections are active. When disabled, an undervoltage or overvoltage condition fault will not be reported in bits D1 and D0 of the output fault register.

Address x111—TEST

The TEST register is reserved for test and is not accessible with SPI during normal operation.

SERIAL OUTPUT COMMUNICATION (DEVICE STATUS RETURN DATA)

When the $\overline{CS}$ pin is pulled low, the output status register is loaded. Meanwhile, the data is clocked out MSB- (OD7-) first as the new message data is clocked into the SI pin. The first eight bits of data clocking out of the SO, and following a $\overline{CS}$ transition, are dependant upon the previously written SPI word.

Any bits clocked out of the SO pin after the first eight will be representative of the initial message bits clocked into the SI pin since the $\overline{CS}$ pin first transitioned to a Logic [0]. This feature is useful for daisy chaining devices as well as message verification.

A valid message length is determined following a $\overline{CS}$ transition of Logic [0] to Logic [1]. If there is a valid message length, the data is latched into the appropriate registers. A valid message length is a multiple of eight bits. At this time, the SO pin is tri-stated and the fault status register is now able to accept new fault status information.

The output status register correctly reflects the status of the STATR-selected register data at the time the $\overline{CS}$ is pulled to a Logic [0] during SPI communication and/or for the period of time since the last valid SPI communication, with the following exceptions:

- The previous SPI communication was determined to be invalid. In this case, the status will be reported as though the invalid SPI communication never occurred.
- Battery transients below 6.0 V resulting in an under-voltage shutdown of the outputs may result in incorrect data loaded into the status register. The SO data transmitted to the MCU during the first SPI communication following an undervoltage V_{PWR} condition should be ignored.
- The $\overline{RST}$ pin transition from a Logic [0] to Logic [1] while the WAKE pin is at Logic [0] may result in incorrect data loaded into the status register. The SO data transmitted to the MCU during the first SPI communication following this condition should be ignored.

Table 15. Serial Output Bit Map Descriptions

Previous STATR D7, D2, D1, D0				Serial Output Returned Data							
SOA3	SOA2	SOA1	SOA0	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
x	0	0	0	WDin	OTF	OCHF	OCLF	OLF	UVF	OVF	FAULT
x	0	0	1	WDin	0	0	1	0	0	CSNS $\overline{EN}$	IN_SPI
x	0	1	0	WDin	0	1	0	SOCH	SOCL2	SOCL1	SOCL0
x	0	1	1	WDin	0	1	1	OL_dis	CD_dis	OCLT1	OCLT0
x	1	0	0	WDin	1	0	0	Fast SR	CSNS high	IN dis	A/O
0	1	0	1	0	1	0	1	FSM_HS	OSD2	OSD1	OSD0
1	1	0	1	1	1	0	1	0	WDTO	WD1	WD0
0	1	1	0	0	1	1	0	0	IN Pin	FSI Pin	WAKE Pin
1	1	1	0	1	1	1	0	0	0	UV_dis	OV_dis
x	1	1	1	WDin	–	–	–	–	–	–	–

x = Don't care.

SERIAL OUTPUT BIT ASSIGNMENT

The eight bits of serial output data depend on the previous serial input message, as explained in the following paragraphs. Table 15 summarizes the SO register content.

Bit OD7 reflects the state of the watchdog bit (D7) addressed during the prior communication. The contents of bits OD6:OD0 depend upon the bits D2:D0 from the most recent STATR command SOA2:SOA0.

Previous Address SOA[2:0]=000

If the previous three MSBs are 000, bits OD6:OD0 reflect the current state of the Fault register (FLTR) (Table 16).

Previous Address SOA[2:0]=001

The data in bits OD1 and OD0 contain CSNS $\overline{EN}$ and IN_SPI programmed bits, respectively.

Previous Address SOA[2:0]=010

The data in bit OD3 contain the programmed overcurrent high detection level (refer to Table 11), and the data in bits OD2, OD1, and OD0 contain the programmed overcurrent low detection levels (refer to Table 10).

Table 16. Fault Register

OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
x	OTF	OCHF	OCLF	OLF	UVF	OVF	FAULT

OD7 (x) = Don't care.

OD6 (OTF) = Overtemperature Flag.

OD5 (OCHF) = Overcurrent High Flag. (This fault is latched.)

OD4 (OCLF) = Overcurrent Low Flag. (This fault is latched.)

OD3 (OLF) = Open Load Flag.

OD2 (UVF) = Undervoltage Flag. (This fault is latched or not latched.)

OD1 (OVF) = Overvoltage Flag.

OD0 (FAULT) = This flag reports a fault and is reset by a read operation.

Note The $\overline{FS}$ pin reports a fault and is reset by a new Switch-ON command (via SPI or direct input IN).

Previous Address SOA[2:0]=011

The data returned in bits OD1 and OD0 are current values for the overcurrent fault blanking time, illustrated in Table 12. Bit OD2 reports when the overcurrent detection time-out feature is active. OD3 reports whether the open load circuitry is active.

Previous Address SOA[2:0]=100

The returned data contain the programmed values in the DICR.

Previous Address SOA[2:0]=101

- SOA3 = 0. The returned data contain the programmed values in the OSDR. Bit OD3 (FSM_HS) reflects the state of the output in the Fail-Safe mode after a watchdog timeout occurs.
- SOA3 = 1. The returned data contain the programmed values in the WDR. Bit OD2 (WDTO) reflects the status of the watchdog circuitry. If WDTO bit is Logic [1], the watchdog has timed out and the device is in Fail-Safe mode. If WDTO is Logic [0], the device is in Normal mode (assuming device is powered and not in the Sleep mode), with the watchdog either enabled or disabled.

Previous Address SOA[2:0]=110

- SOA3 = 0. OD2, OD1, and OD0 return the state of the IN, FSI, and WAKE pins, respectively (Table 17).

Table 17. Pin Register

OD2	OD1	OD0
IN Pin	FSI Pin	WAKE Pin

- SOA3 = 1. The returned data contains the programmed values in the UOVR register. Bit OD1 reflects the state of the undervoltage protection, while bit OD0 reflects the state of the overvoltage protection (refer to Table 15).

Previous Address SOA[2:0]=111

Null Data. No previous register Read Back command received, so bits OD2, OD1, and OD0 are null, or 000.

TYPICAL APPLICATIONS

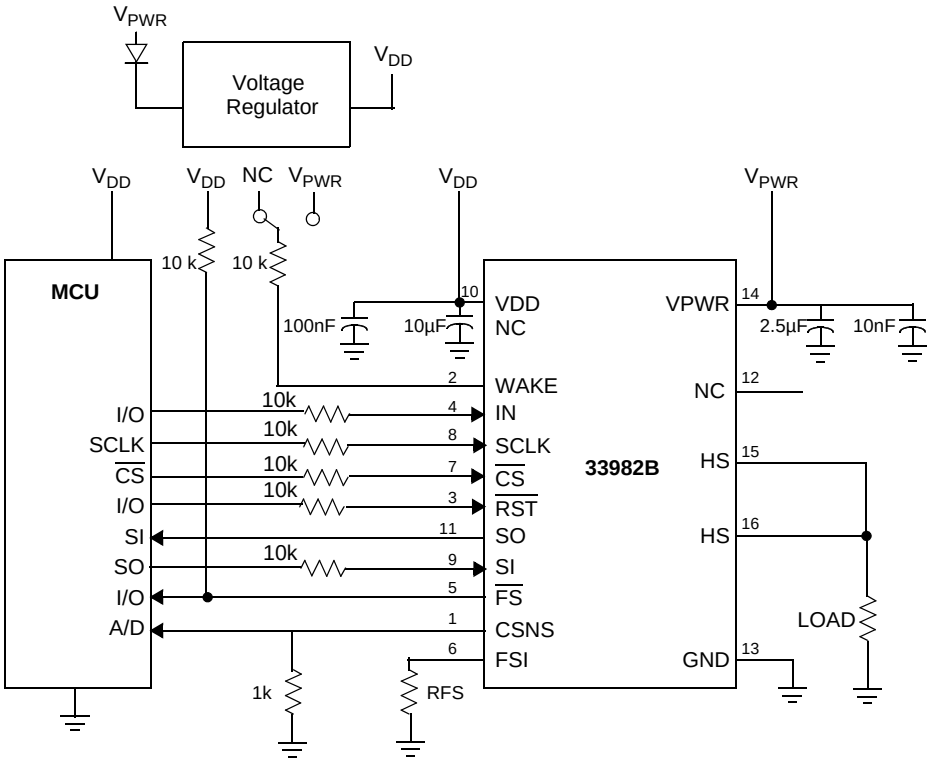


Figure 11. Typical Applications

PACKAGING

SOLDERING INFORMATION

SOLDERING INFORMATION

The 33982B is packaged in a surface mount power package intended to be soldered directly on the printed circuit board.

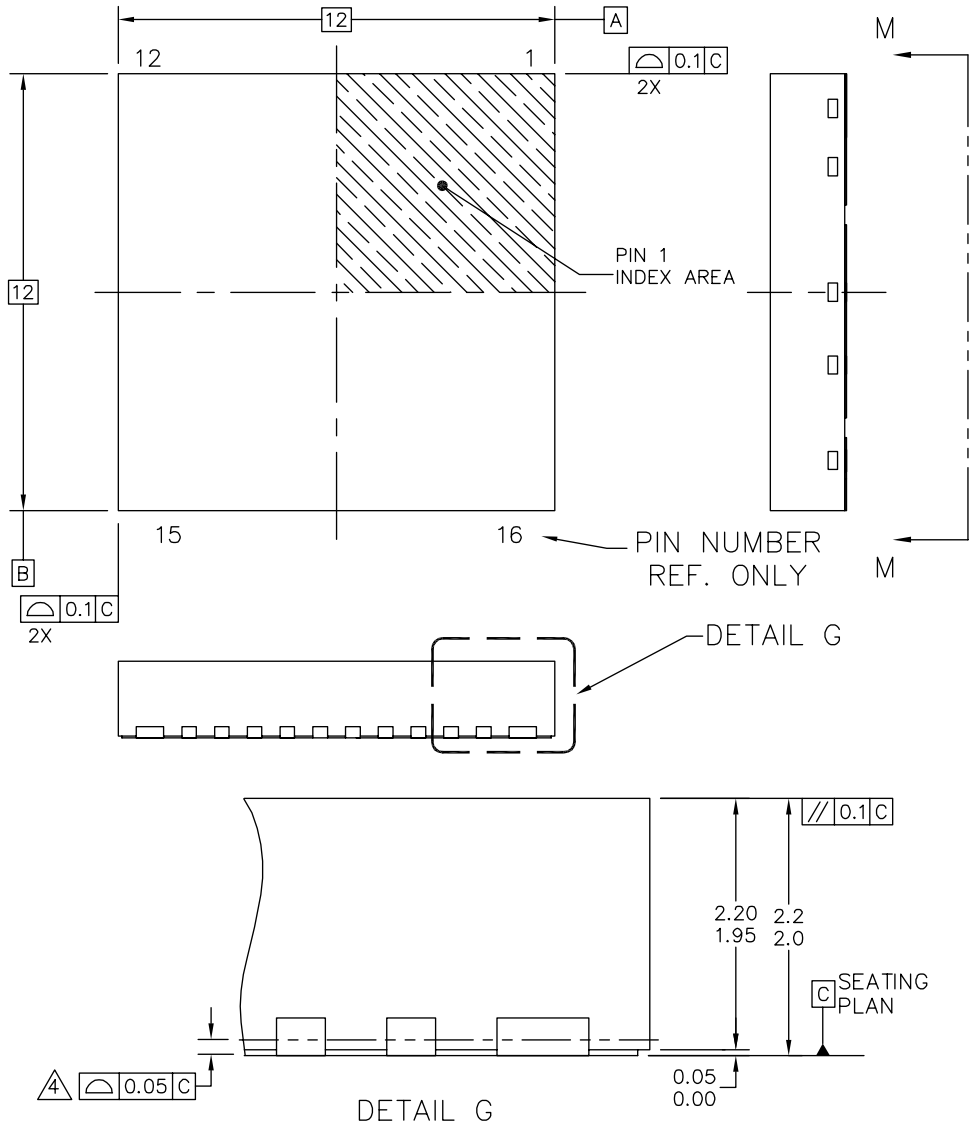
The 33982B was qualified in accordance with JEDEC standards JESD22-A113-B and J-STD-020A. The recommended reflow conditions are as follows:

- Convection: 225°C +5.0/-0°C
- Vapor Phase Reflow (VPR): 215°C to 219°C
- Infrared (IR)/Convection: 225°C +5.0/-0°C

The maximum peak temperature during the soldering process should not exceed 230°C. The time at maximum temperature should range from 10 s to 40 s maximum.

PACKAGE DIMENSIONS

For the most current revision of the package, visit www.freescale.com and perform a keyword search on 98ARL10596D.



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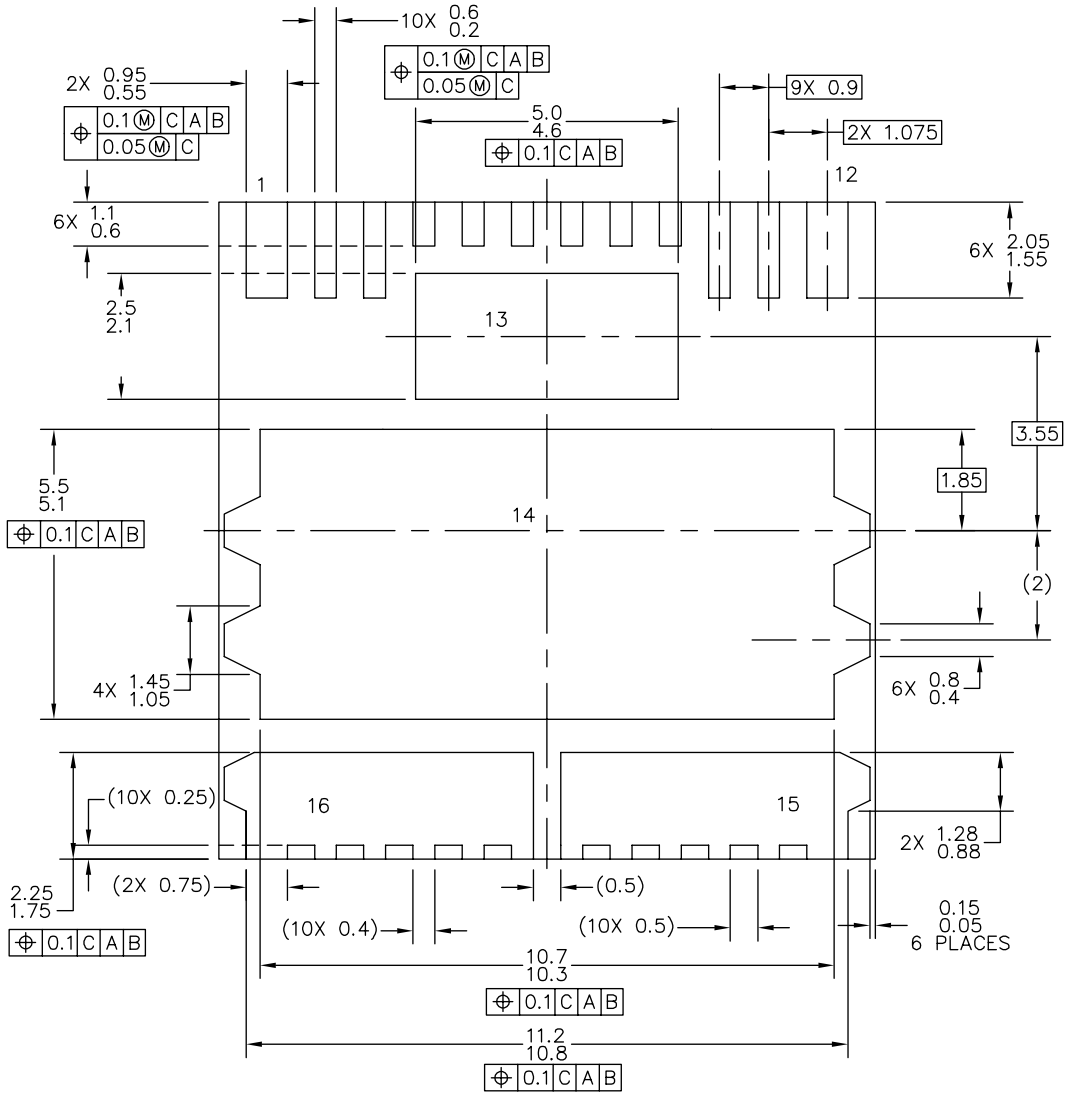
	CASE NUMBER: 1402-02	27 APR 2005
	STANDARD: NON-JEDEC	

PNA SUFFIX
16-PIN PQFN
NONLEADED PACKAGE
98ARL10521D
ISSUE C

33982

PACKAGE DIMENSIONS (CONTINUED)



VIEW M–M

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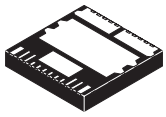
ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 3.0)

33982

High-Side Switch



PNA SUFFIX
98ARL10521D
16-PIN PQFN
12 mm x 12 mm

Note For package dimensions, refer to the 33982B data sheet.

Introduction

This thermal addendum is provided as a supplement to the MC33982B technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Packaging and Thermal Considerations

This package is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

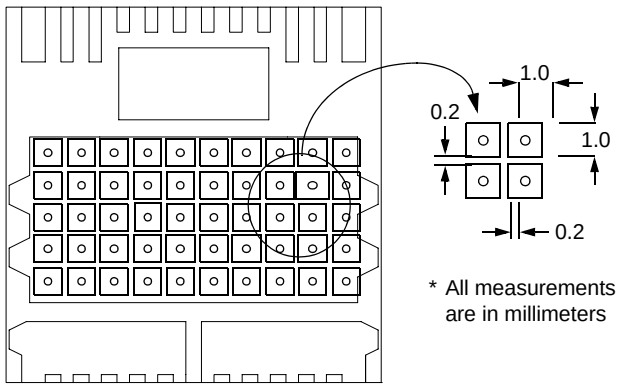
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 18. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1), (2)	20	16	39
$R_{\theta JBmn}$ (2), (3)	6	2.0	26
$R_{\theta JAmn}$ (1), (4)	53	40	73
$R_{\theta JCmn}$ (5)	<0.5	0.0	1.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



Note: Recommended via diameter is 0.5 mm. PTH (plated through hole) via must be plugged / filled with epoxy or solder mask in order to minimize void formation and to avoid any solder wicking into the via.

Figure 12. Surface Mount for Power PQFN with Exposed Pads

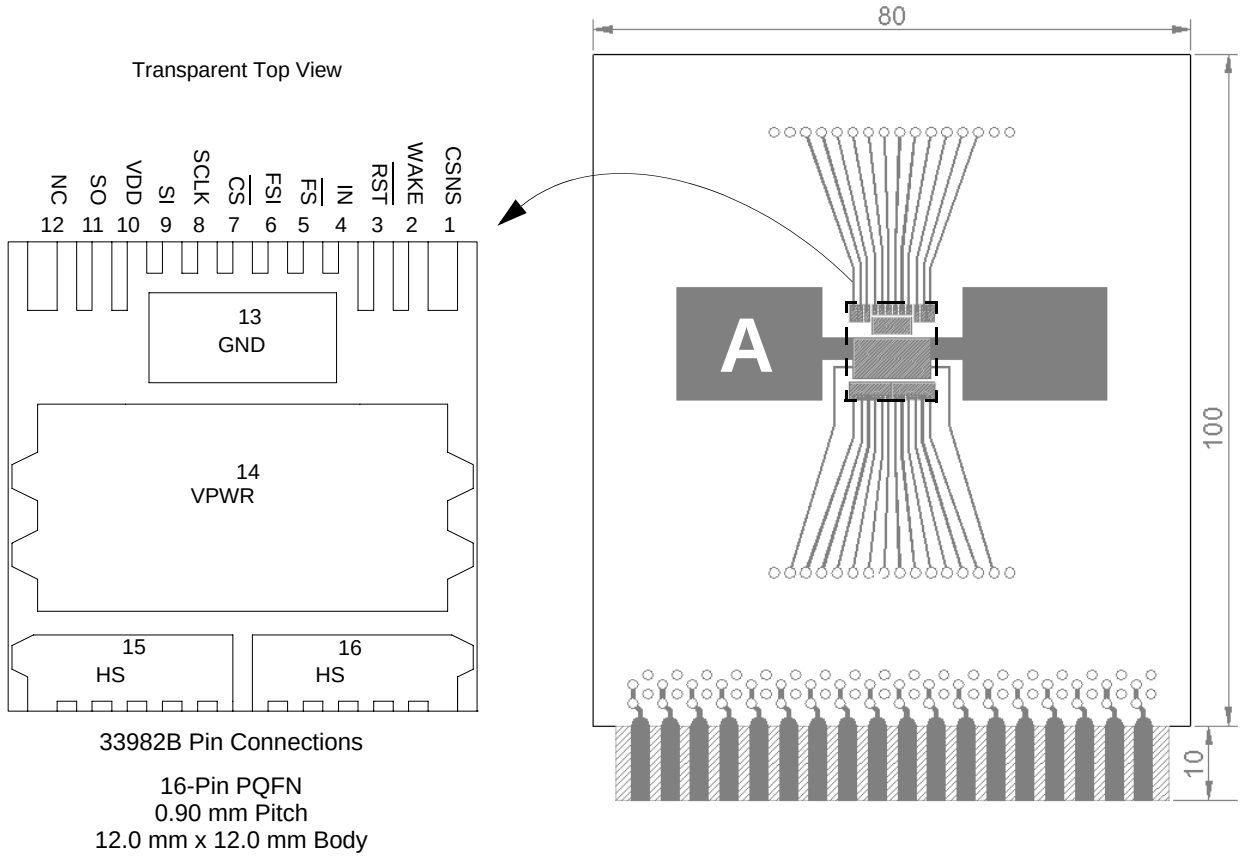


Figure 13. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area A:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 19. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$	0	55	42	74
	300	41	32	66
	600	39	29	65

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

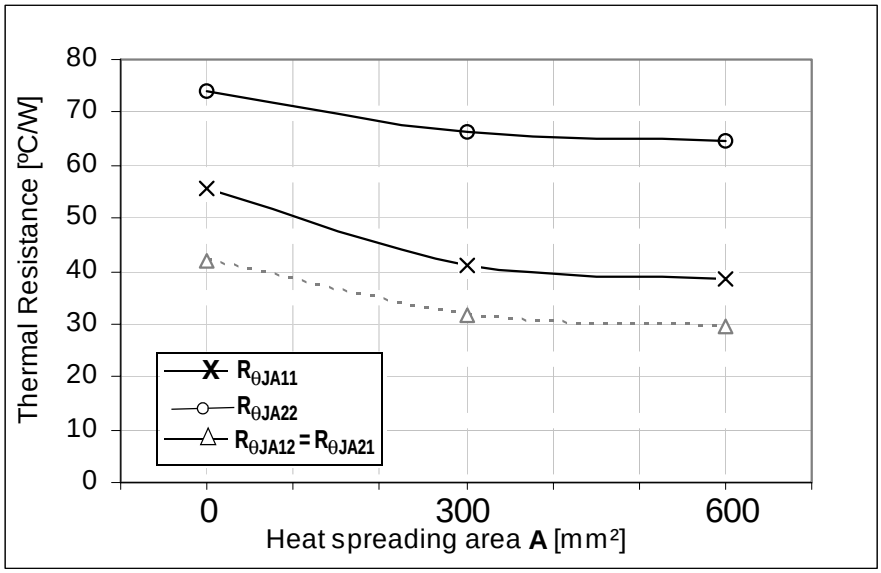


Figure 14. Device on Thermal Test Board $R_{\theta JA}$

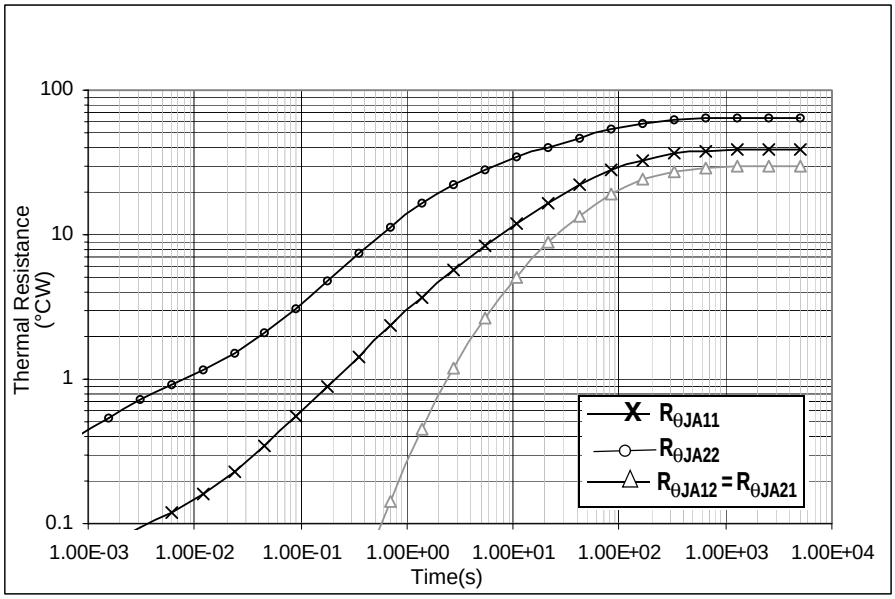


Figure 15. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
10.0	2/2006	• Implemented Revision History page • Deletion of MC33982 part number, replaced with MC33982B.
11.0	5/2006	• Corrected Pin Connections to the proper case outline • Added final sentence to Open Load Fault (Non-Latching) • Corrected heading labels on Input Timing Switching Characteristics • Changed labels in the Typical Applications drawing • Corrected Package Dimensions to Revision C • Added Thermal Addendum (Rev 3.0).
12.0	1/2007	• Added RoHS logo to the data sheet

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