

YAMAHA® LSI

YTM403C

MD9624 (FAX/DATA/VOICE LSI)

■ OUTLINE

The YTM403C is a single-chip MODEM LSI that can be used both as a facsimile MODEM and as a data MODEM.

As a facsimile MODEM, it has a built-in 9600/7200/4800/2400/300 bps half-duplex synchronous (CCITT V.29, V.27ter, V.21ch2) data pump function, and is the most suitable MODEM for G3 facsimile machines.

As a data MODEM, it has a built-in 2400/1200/600/300 bps asynchronous full-duplex data pump function (CCITT V.22bis, V.22, V.21, BELL 212A, 103), and is best suited for data transmission applications such as a personal computer communications and data base retrieval.

In addition to the built-in data pump functions, the YTM403C has a USART function which allows HDLC framing processes and start-stop processing independently. The USART function is indispensable for ECM (error correction mode) compatible G3 facsimiles. The YTM403C also provides built-in ADC and DAC functions for VOICE recording and reproducing compatibilities through external accessing and VOICE data compression, and expansion functions for telephone line VOICE recording and reproduction independently. A power down function is also built-in to the YTM403C, which is indispensable for saving when the machine is not in use. Substantial power of modems used with portable facsimile units and laptop personal computers while YTM403C is not in use. All of the functions of the YTM403C are controlled by external micro-processors, which are not restricted, but are selectively connectable to external terminals.

■ FEATURES

Communication compatibility

- CCITT V.29, V.27ter, V.26bis, V.23, V22bis, V.22 (A/B), V.21
- Bell 212A, 202, 103

Communication speed

- Synchronous half-duplex communication: 9600/7200/4800/2400/1200/300bps
- Asynchronous full-duplex communication: 2400/1200/600/300bps
- Modified full-duplex communication: 4800 (75) /1200 (75) bps

Built-in VOICE function

- Sampling frequency: 9600 Hz
- 16-bit PCM
- 4-bit ADPCM (YAMAHA system)

YAMAHA CORPORATION

YTM403C CATALOG
CATALOG No.: LSI-4TM4032
1993. 11

- ☐ Built-in scrambler/descrambler: V.29/V.27ter/V.22bis/V.22/212A
- ☐ Built-in training sequencer: V.29/V.27ter
- ☐ Built-in handshake sequencer: V.22bis/V.22/212A
- ☐ Built-in asynchronous/synchronous and synchronous/asynchronous conversion function
 - CCITT V.22bis/V.22 compatibility
 - Bell 212A compatibility
 - Character length: 8, 9, 10 and 11 bits
- ☐ Built-in equalizer function
 - Sending subscriber cable equalizer (3 types)
 - Receiving subscriber cable equalizer (3 types)
 - Adaptive automatic equalizer
- ☐ DTE interface
 - Serial interface (V.24)
 - Parallel interface (microprocessor bus)
 - USART function (HDLC framing, start-stop framing)
- ☐ Built-in programmable tone generating function
 - Simultaneous 4 tone generation capability
 - Programmable frequency and level
 - Useful for sending guard tone, call progress tone and DTMF tone
- ☐ Built-in programmable tone detection function
 - Programmable center frequency, bandwidth and level (11 channels)
 - Allows call progress tone and DTMF detection capability
- ☐ Built-in guard tone notch filter: V.22bis/V.22
- ☐ Built-in training signal detection function: V.29/V.27ter
- ☐ Built-in S1 signal sending/detection function: V.22bis
- ☐ Built-in V.21ch2 flag sequence detection function
- ☐ Transmission clock selection capability: Internal clock/external clock/slave mode
- ☐ Reception dynamic range: 0~50dBm
- ☐ Control capability for carrier detection level
- ☐ Built-in AGC (Mode control capability)
- ☐ Sending level control capability: -6~∞dBm
- ☐ Built-in transmit/receive band pass filter
- ☐ Built-in ADC/DAC: External control ability
- ☐ Eye pattern output capability
- ☐ Built-in loopback connection function
 - Remote digital loopback
 - Local digital loopback
 - Local analog loopback

General purpose I/O port: for NCU control use

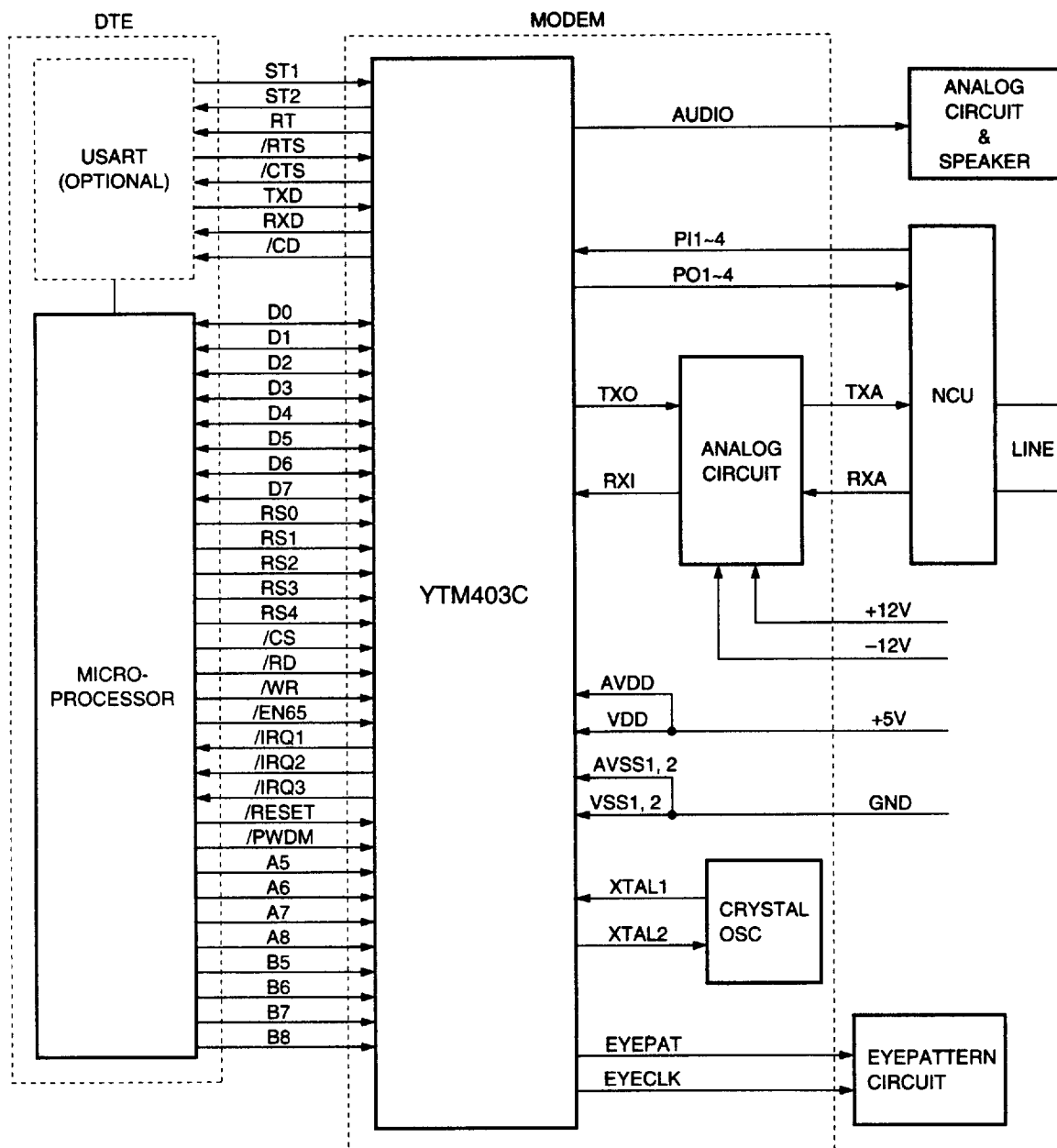
Power down mode/ power save mode

Low power consumption of CMOS

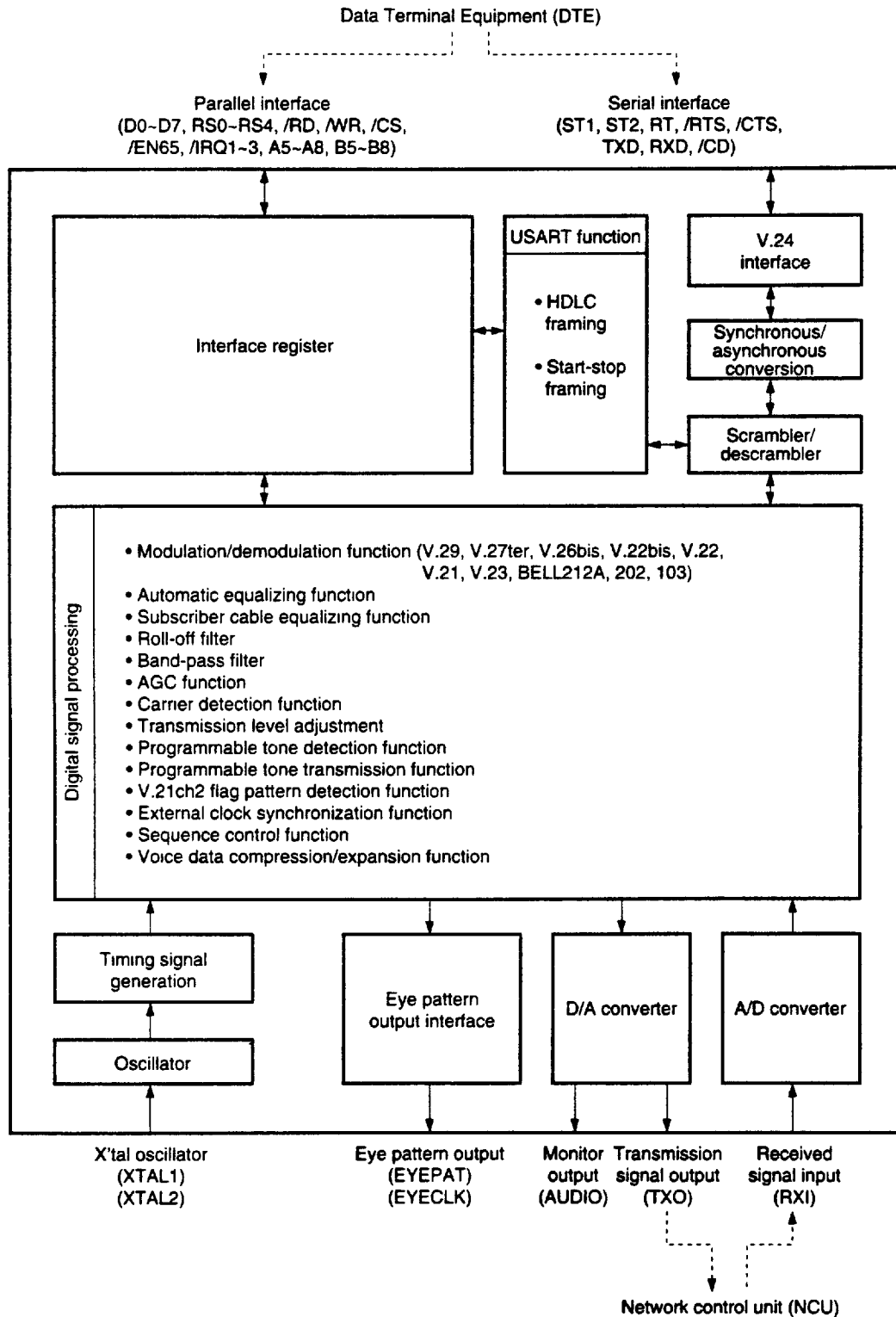
+5V single power supply

Package: 64-pin QFP/ 64-pin SDIP/ 64-pin TQFP

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



Other inputs/outputs General purpose inputs (PI1~PI4)
and outputs (PO1~PO4)
I/O-Reset input (/RESET)
I/O-Test input (/TEST)
Power down input (/PWDM)

■ OPERATION MODE AND COMMUNICATION PROTOCOL

The YTM403C has the following operating modes:

- 9600 bps half-duplex communication: V.29
- 7200 bps half-duplex communication: V.29
- 4800 bps half-duplex communication: V.29/V.27ter
- 2400 bps half-duplex communication: V.27ter/V.26bis
- 1200 bps half-duplex communication: V.26bis/V.23/Bell202
- 600 bps half-duplex communication: V.23
- 300 bps half-duplex communication: V.21ch2
- 75 bps half-duplex communication: V.23/V.26bis/V.27ter
- 150 bps half-duplex communication: V.23/V.26bis/V.27ter
(150 bps is outside the scope of CCITT recommendation)

- 2400 bps full-duplex communication: V.22bis
- 1200 bps full-duplex communication: V.22 (A, B) /Bell1212A
- 600 bps full-duplex communication: V.22 (A, B)
- 300 bps full-duplex communication: V.21/ Bell1103

PCM (VOICE) record and playback 16-bits resolution

ADPCM record and playback: YAMAHA 16-bit → 4-bit compression

Table 1 shows the communication protocol specifications applicable to the YTM403C.

Table 1 Communication protocols

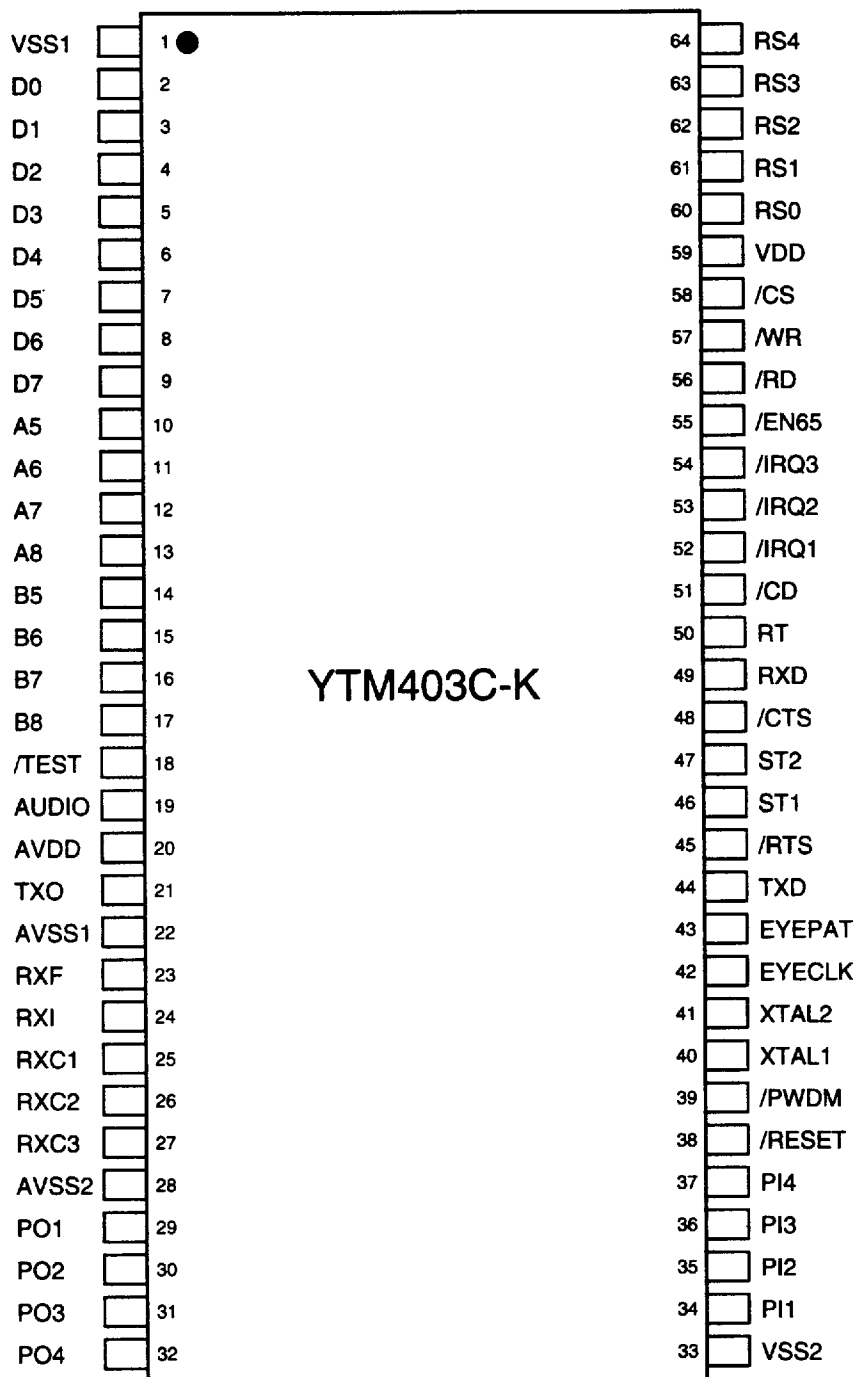
Communication protocol		Transmission speed (bps)	Modulation speed (Baud)	Carrier frequency (Hz)		Modulation method	Communication method
CCITT V.29		9600	2400	1700		16-QAM	Half-duplex (two-wire) Synchronous
		7200	2400			8-QAM	
		4800	2400			4-QAM	
CCITT V.27ter		4800	1600	1800		8-PSK	
		2400	1200			4-PSK	
CCITT V.26bis		2400	1200	1800		4-PSK	
		1200	1200			2-PSK	
CCITT V.23		1200	1200	Space Mark	2100 1300	FSK	Half-duplex (two-wire)
		600	600	Space Mark	1700 1300	FSK	
		* 150	150	Space Mark	450 390	FSK	Half-duplex (two-wire) Backward
		75	75	Space Mark	450 390	FSK	
BELL 202		1200	1200	Space Mark	1200 2200	FSK	Half-duplex (two-wire)
CCITT V.22bis		2400	600	Low ch High ch	1200 2400	16-QAM	Full-duplex (two-wire)
CCITT V.22		1200	600	Low ch High ch	1200 2400	4-QAM	
		600	600	Low ch High ch	1200 2400	2-QAM	
CCITT V.21	ch1	300	300	Space Mark	1180 980	FSK	
	ch2	300	300	Space Mark	1850 1650	FSK	
BELL 212A		1200	600	Low ch High ch	1200 2400	4-QAM	
BELL 103	ch1	300	300	Space Mark	1070 1270	FSK	
	ch2	300	300	Space Mark	2025 2225	FSK	

* : 150 bps is outside the scope of CCITT recommendation

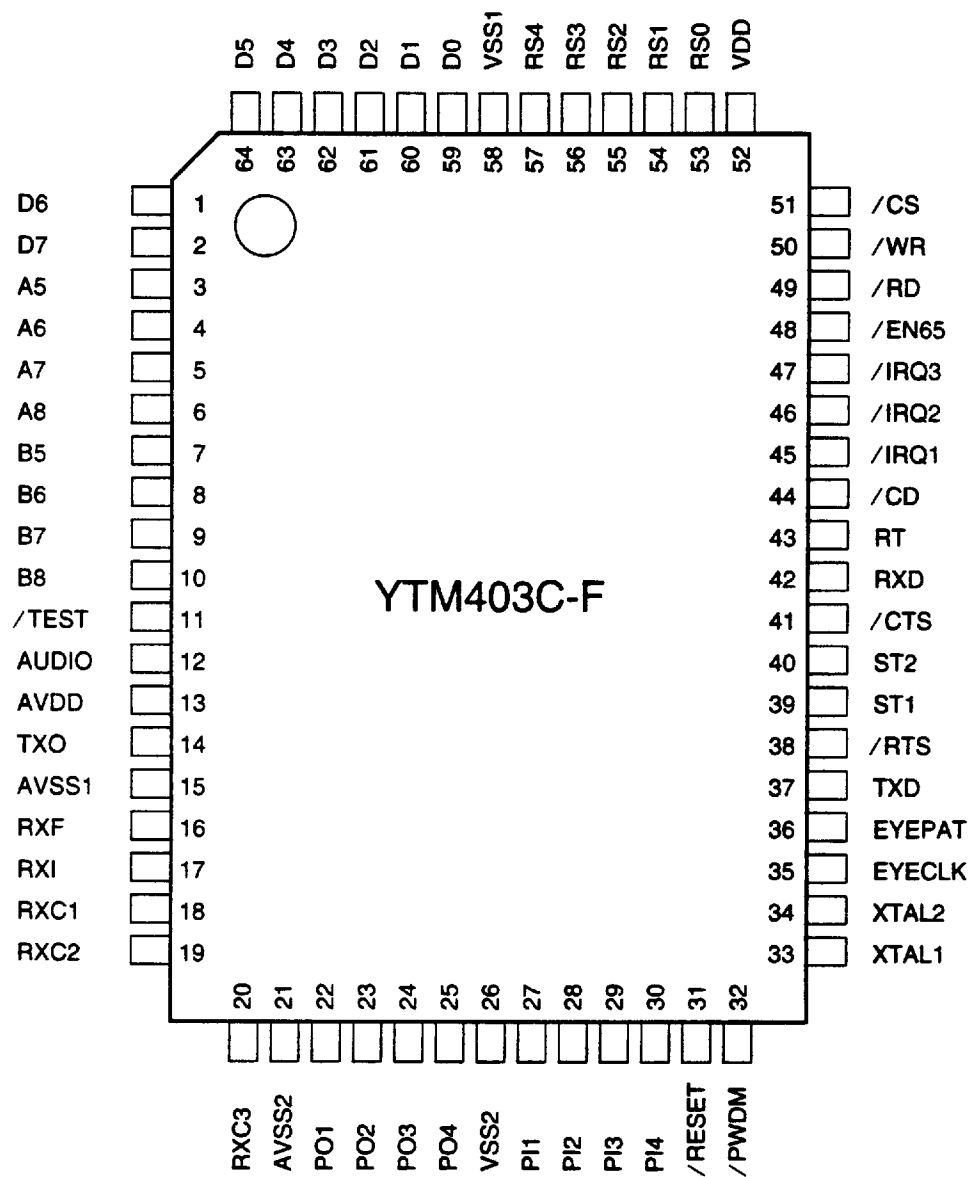
DESCRIPTION OF PINS

1. Pin assignment

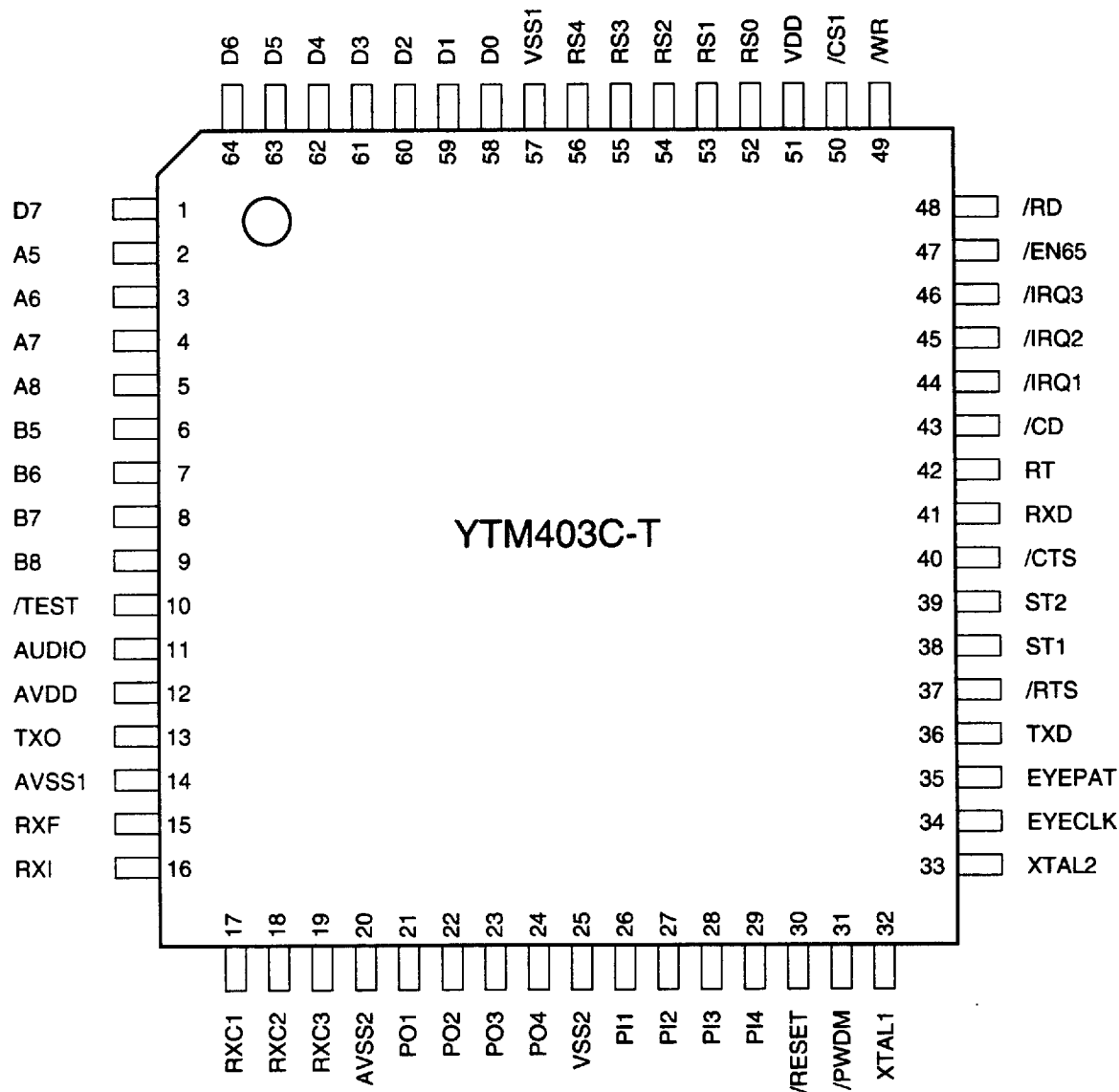
□ 64-pin SDIP



64-pin QFP



64-pin TQFP



2. Function Assignment to Pins

Pin name	Pin No.			TYPE	Function
	SDIP	QFP	TQFP		
RS0-RS4	60-64	53-57	52-56	DI	Interface register selective input (5 bits)
A5-A8, B5-B8	10-13, 14-17	3-6, 7-10	2-5, 6-9	DIO	Address decoder input/test input/output (When A input and B input are the same and pin /CS is LOW, the register can be accessed.)
D0-D7	2-9	59-64 1, 2	58-64 1	DIO	Data bus (8 bits)
/EN65	55	48	47	DI	Microprocessor selective input (LOW: 6520 type, HIGH: 80 type)
/RD	56	49	48	DI	(/EN65: HIGH) register read strobe input (/EN65: LOW) strobe pulse input
/WR	57	50	49	DI	(/EN65: HIGH) register write strobe input (/EN65: LOW) R/R input
/CS	58	51	50	DI	Chip select input
/IRQ1	52	45	44	DOD	Transmission interrupt request output (open-drain output)
/IRQ2	53	46	45	DOD	Reception interrupt request output (open-drain output)
/IRQ3	54	47	46	DOD	General interrupt request output (open-drain output)
/TEST	18	11	10	DIP	Test input (pull-up resistor incorporated)
TXD	44	37	36	DIP	Transmit data input (pull-up resistor incorporated)
RXD	49	42	41	DO	Receive data output
/RTS	45	38	37	DIP	Request to send input (pull-up resistor incorporated)
/CTS	48	41	40	DO	Clear to send output
/CD	51	44	43	DO	Data channel receive carrier detection output
ST1	46	39	38	DIP	Transmit data clock input (pull-up resistor incorporated)
ST2	47	40	39	DO	Transmit data clock output
RT	50	43	42	DO	Receive data clock output
RXI	24	17	16	AI	Receive signal input
RXC1	25	18	17	AO	AD conversion capacitor pin
RXC2	26	19	18	AO	AD conversion capacitor pin
RXC3	27	20	19	AO	AD conversion capacitor pin
RXF	23	16	15	AO	AD conversion output
TXO	21	14	13	AO	Transmit signal output (1 bit DAC output)
AUDIO	19	12	11	AO	Receive signal monitor output (1 bit DAC output)
PO1	29	22	21	DO	General purpose output port 1
PO2	30	23	22	DO	General purpose output port 2
PO3	31	24	23	DO	General purpose output port 3
PO4	32	25	24	DO	General purpose output port 4
PI1	34	27	26	DI	General purpose input port 1
PI2	35	28	27	DI	General purpose input port 2
PI3	36	29	28	DI	General purpose input port 3
PI4	37	30	29	DI	General purpose input port 4

Pin name	Pin No.			TYPE	Function
	SDIP	QFP	TQFP		
EYEPAT	43	36	35	DO	Eye pattern data output
EYECLK	42	35	34	DO	Eye pattern clock output
VDD	59	52	51	PWR	Digital +5V source
VSS1	1	58	57	GND	Digital ground 1
VSS2	33	26	25	GND	Digital ground 2
AVDD	20	13	12	PWR	Analog +5V source
AVSS1	22	15	14	GND	Analog ground 1
AVSS2	28	21	20	GND	Analog ground 2
/RESET	38	31	30	DI	Reset input
/PWDM	39	32	31	DI	Power down mode setting input
XTAL1	40	33	32	XI	Crystal oscillator pin or external oscillator clock input
XTAL2	41	34	33	XO	Crystal oscillator pin

NOTE:

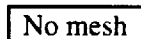
Type symbols

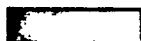
- DI Digital input
- DO Digital output
- DIP Pull-up resistor incorporated digital input
- DOD Open drain output
- DIO Digital input/output
- AI Digital input
- AO Analog output
- PWR Power supply
- GND Ground
- XI, XO Crystal oscillator connection

■ INTERFACE REGISTER MAP

RS4-RS0	Reg. No.		bit 7 (MSB)	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0 (LSB)
11111	1F	D	TXCONF							
11110	1E	D	TXINIT	—	TXTDIS	TXEPT	TXCBL2	TXCBL1	TXCLK2	TXCLK1
11101	1D	D	RTS	B202	—	—	—	TXMHD	SDIS	TXS1
11100	1C	D	CTS	TXE	—	—	—	—	—	—
11011	1B	U	THDLC2	THDLC1	TXRUN2	TXRUN1	TXHDIE	TXABRT	TXFCS	TXFLAG
11010	1A	U	TXASYN	TXOSP	TXCHR2	TXCHR1	—	—	TXPON	TXPODD
11001	19	U	TXREQ	TXRQIE	TXPDM	LB3	LB2	LB1	TXBRK	TXD8
11000	18	U	TXDATA							
10111	17	D	RXCONF							
10110	16	D	RXINIT	—	RXTDIS	—	RXCBL2	RXCBL1	—	—
10101	15	D	—	—	—	—	EQHD	EQRS	DDIS	S1/P2IE
10100	14	D	CDET	FCD	SOD	TDET	SDDET	SMDET	UMDET	S1/P2DET
10011	13	U	RHDLC2	RHDLC1	—	—	RXHDIE	RXABRT	RXCRC	RXFLAG
10010	12	U	RXASYN	RXOSP	RXCHR2	RXCHR1	—	—	RXPON	RXPODD
10001	11	U	RXREQ	RXRQIE	RXDSEL	RXOVRN	RXPERR	RXFERR	BDET	RXD8
10000	10	U	RXDATA							
01111	0F	D	XRAMRQ	XRAMIE	XRAMW	XBYTE	XTIME	XBAUD	XRAMA9	XRAMA8
01110	0E	D	XRAMA							
01101	0D	D	XRAMDM							
01100	0C	D	XRAMDL							
01011	0B	D	YRAMRQ	YRAMIE	YRAMW	YBYTE	YTIME	YBAUD	YRAMA9	YRAMA8
01010	0A	D	YRAMA							
01001	09	D	YRAMDM							
01000	08	D	YRAMDL							
00111	07	D	TONE4	TONE3	TONE2	TONE1	—	—	—	AGC1
00110	06	D	AHS	AUDIO	—	FRSP	GC4	GC3	GC2	GC1
00101	05	D	TIME4	TIME3	TIME2	TIME1	—	FR3	FR2	FR1
00100	04	D	COL4	COL3	COL2	COL1	ROW4	ROW3	ROW2	ROW1
00011	03	D	TIME4E	TIME3E	TIME2E	TIME1E	TIME1R	TIME1E	—	—
00010	02	D	—	—	—	—	—	—	—	—
00001	01	¥	SRESET	PWRSV	PI2IE	PI1IE	PO4	PO3	PO2	PO1
00000	00	¥	WRBUSY	IA1	IA2	IA3	PI4	PI3	PI2	PI1

NOTE: For the bits indicated by —, “0” must always be written.

 : Control bit

 : Status bit

 : Bit with both control bit and status bit functions

 : Bit that causes an interrupt

D : DSP-related register

U : USART circuit-related register

¥ : Registers composed of asynchronous circuits, and remain operational even during the power save mode.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (VSS1=VSS2=AVSS1=AVSS2=0V)

Item	Symbol	Rating		Unit
		min.	max.	
Source voltage	V _{DD}	-0.5	+7.0	V
Input voltage	V _I	-0.5	V _{DD} +0.5	V
Output voltage	V _O	-0.5	V _{DD} +0.5	V
Storage temperature	T _{stg}	-50	+125	°C

(The electrical characteristics are all target specifications.)

2. Recommended Operating Conditions (VSS1=VSS2=AVSS1=AVSS2=0V)

Item	Symbol	Rating			Unit
		min.	typ.	max.	
Source voltage	V _{DD}	4.5	5.0	5.5	V
Operational ambient temperature	T _{op}	-40	25	+85	°C
Clock frequency	f _{CLK}	19.6588	19.6608	19.6628	MHz

(The electrical characteristics are all target specifications.)

3. DC Characteristics

(Where not otherwise specified, the recommended operating conditions apply)

Item		Symbol	Applicable pin type and measuring condition	Rating			Unit
				min.	typ.	max.	
High-level input voltage		V _{DIH}	DI, DIP, DIO	2.0	—	—	V
Low-level input voltage		V _{DIL}	DI, DIP, DIO	—	—	0.8	V
Input leak current (*1)		I _{LDIH}	DI	-10	—	+10	μA
Pull-up current (*1)		I _{PU}	DIP	-20	—	-200	μA
Input capacitance (*1)		C _I	DI, DIP	—	10	—	pF
High-level output voltage		V _{DOH}	DO, DIO @2.0 mA	V _{DD} -1.0	—	—	V
Low-level output voltage		V _{DOL}		—	—	0.4	V
Open-drain output lowlevel current		I _{DOD}	DOD@0.4V	—	—	4.0	mA
Output leak current (*1)		I _{LOUT}	DIO, DOD At HI-Z	-10	—	+10	μA
Output capacitance (*1)		C _O	DO, DIO, DOD	—	15	—	pF
High-level clock input voltage		V _{CLKH}	XI (*2)	V _{DD} -1.0	—	—	V
Low-level clock input voltage		V _{CLKL}	XI (*2)	—	—	1.0	V
Clock input leak current (*1)		I _{LCLK}	XI (*2)	-100	—	+100	μA
Clock input capacitance (*1)		C _{LI}	XI (*2)	—	15	—	pF
Analog input voltage range		V _{AI}	AI	0.0	—	V _{DD}	V
Analog input leak current		I _{LAI}	AI	-1	—	+1	mA
Analog output voltage range		V _{AO}	AO	0.0	—	V _{DD}	V
Source current (*3)	Normal operation	I _{DD}	PWR, GND	—	70	100	mA
	Power save	I _{PSV}	PWR, GND	—	200	500	μA
	Power down	I _{PWN}	PWR, GND	—	5	50	μA

(The electrical characteristics are all target specifications)

(*1) Under operational ambient temperature T_{op}=25°C, and source voltage V_{DD}=5.0V

(*2) When external clock is input

(*3) The source current (type) is under source voltage V_{DD}=5.0V, and operational ambient temperature T_{op}=25°C, and (max) is under V_{DD}=5.2V, T_{op}=recommended condition.

4. AC Characterintics

(Where not otherwise specified, the recommended operating conditions apply)

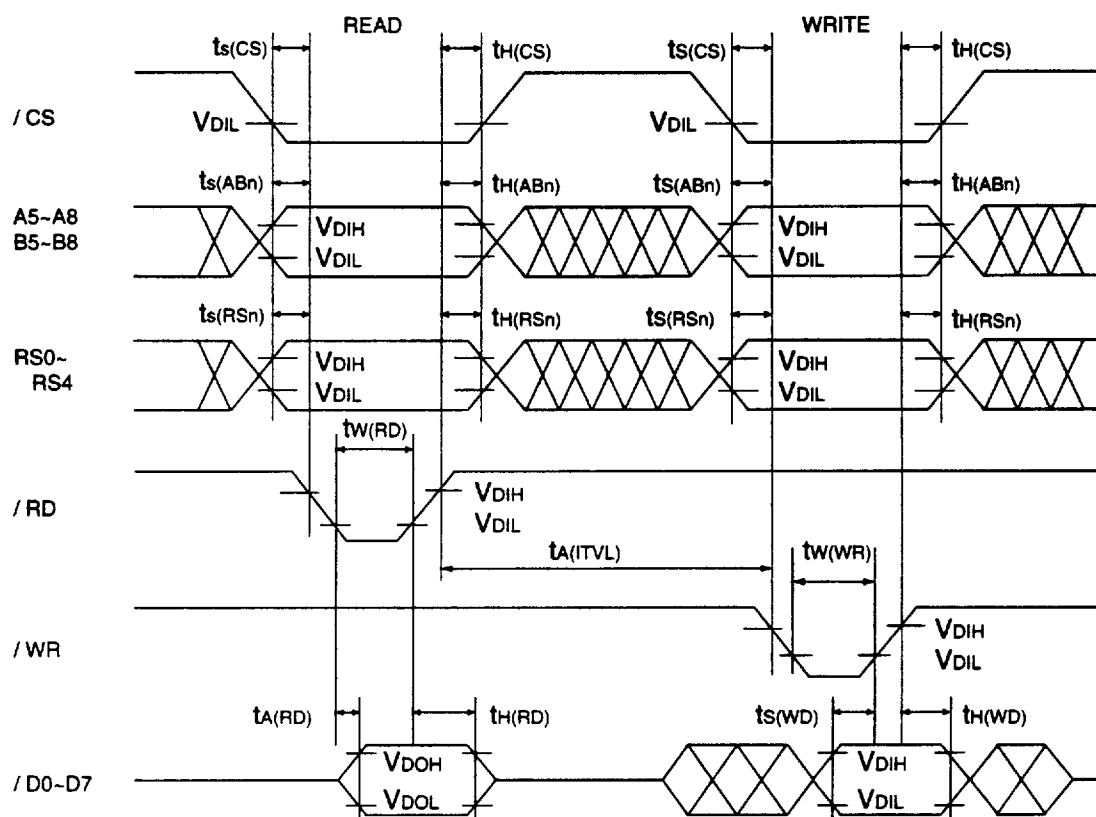
Item	Symbol	Condition	Rating			Unit
			min.	typ.	max.	
Reset input pulse width	$t_{W(RESET)}$		1.0	—	—	ms
/CS set-up time	$t_{S(CS)}$		0	—	—	ns
/CS hold time	$t_{H(CS)}$		0	—	—	ns
ABn set-up time	$t_{S(ABn)}$		10	—	—	ns
ABn hold time	$t_{H(ABn)}$		10	—	—	ns
RSn set-up time	$t_{S(RSn)}$		10	—	—	ns
RSn hold time	$t_{H(RSn)}$		10	—	—	ns
Write data setup time	$t_{S(WD)}$		30	—	—	ns
Write data hold time	$t_{H(WD)}$		10	—	—	ns
Write strobe pulse width	$t_{W(WR)}$		60	—	—	ns
Read data access time	$t_{A(RD)}$		—	—	80	ns
Read data hold time	$t_{H(RD)}$		10	—	50	ns
Read strobe pulse width	$t_{A(RD)}$		60	—	—	ns
Read/write access interval	$t_{A(ITVL)}$	(*1)	1	—	—	μs

(The electrical characteristics are all target specifications)

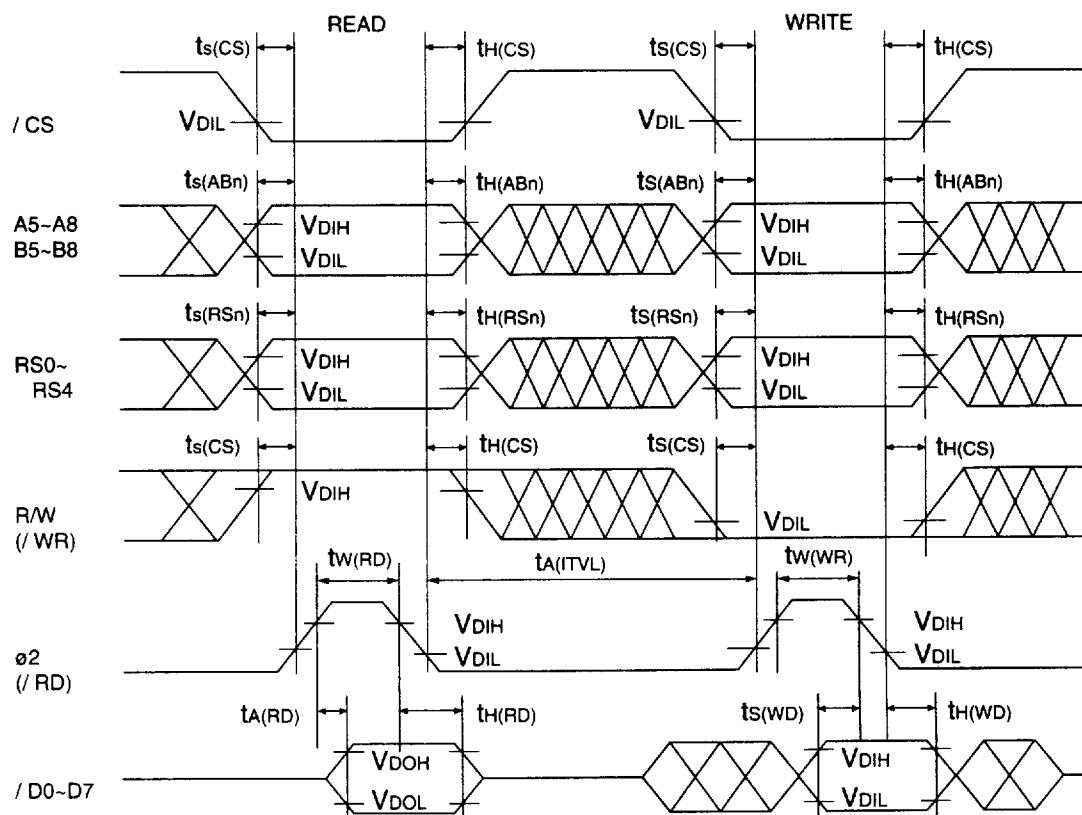
(*1) Interface register access interval

5. AC Characteristics Timing Chart

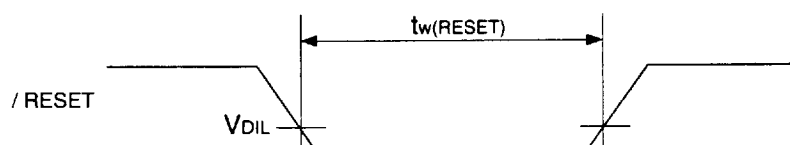
(a) 80 type mode (/EN65 = HIGH)



(b) 6502 type (68 type) mode (/EN65 = LOW)



(c) Resetting



The specifications of this product are subject to improvement changes without prior notice.

— AGENCY —

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