

**1024 BIT (256 X 4) STATIC MOS RAM
 WITH SEPARATE I/O**

DESCRIPTION The μPD2101AL is a 256 word by 4 bit static random access memory requiring no clocks or refreshing. It features high speed, low cost, and simplicity of interfacing.

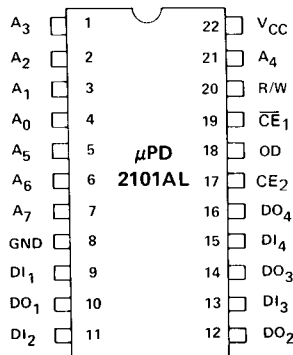
It is directly TTL compatible in all respects; inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bidirectional logic in a common I/O system. Output data is the same polarity as input data, and readout is non-destructive.

The μPD2101AL family of devices offers access times from 450 ns to 250 ns with a typical standby mode power dissipation of only 36 mW.

The use of NEC's N-channel silicon gate MOS process, with its excellent protection from contamination, permits the use of a low cost 22 pin plastic package in providing a high performance, high reliability MOS circuit at a most cost effective price level. The μPD2101AL is pin-compatible with the μPD5101 CMOS static RAM.

- FEATURES**
- 256 x 4 Organizations to Meet Needs for Small System Memories
 - Access Time – 250 to 450 nsec max
 - Directly TTL Compatible – All Inputs and Output
 - Static MOS – No Clocks or Refreshing Required
 - Simple Memory Expansion – Chip Enable Input
 - Low Standby Power – 36 mW typ.
 - Low Cost Packaging – 22 Pin Plastic Dual-In-Line Configuration
 - Low Operating Power
 - Three-State Output – OR-Tie Capability
 - Output Disable Provided for Ease of Use in Common Data Bus Systems

PIN CONFIGURATION



PIN NAMES

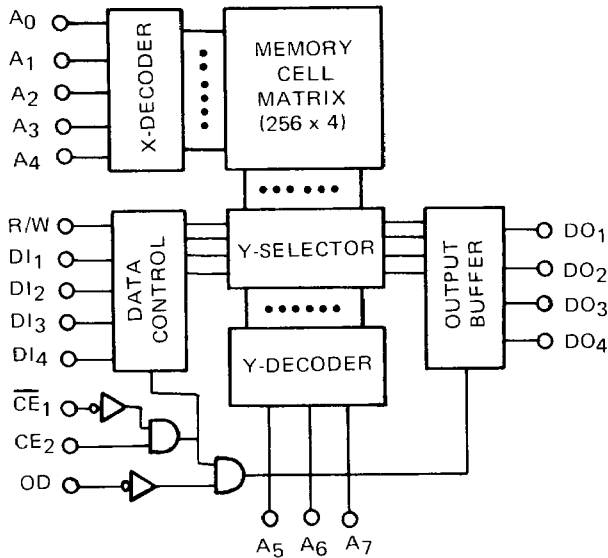
DI ₁	DI ₄	DATA INPUT	CE ₂	CHIP ENABLE 2
A ₀ -A ₇		ADDRESS INPUTS	OD	OUTPUT DISABLE
R/W		READ/WRITE INPUT	DO ₁ DO ₄	DATA OUTPUT
CE ₁		CHIP ENABLE 1	V _{CC}	POWER (+5V)

OPERATION MODES

CE ₁	CE ₂	OD	CHIP	OUTPUT MODE
0	1	0	Selected	Data Out
0	1	1		High Impedance
Others			No Selected	

μ PD2101AL

BLOCK DIAGRAM



Operating Temperature	-10°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltage V _{CC}	-0.5 to +7 Volts

ABSOLUTE MAXIMUM RATINGS*

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

T_a = -10°C to +70°C, V_{CC} = +5V ± 5%.

DC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V _{IH}	+2.0		V _{CC}	V	
Input Low Voltage	V _{IL}	-0.5		+0.8	V	
Output High Voltage	V _{OH}	+2.4			V	I _{OH} = -100 μA
Output Low Voltage	V _{OL}			+0.4	V	I _{OL} = +2.1 mA
Input Leakage Current High	I _{LIH}			+10	μA	V _I = V _{CC}
Input Leakage Current Low	I _{LIL}			-10	μA	V _I = 0V
Output Leakage Current High	I _{LOH}			+10	μA	V _O = +2.4V to V _{CC} CE ₁ = +2.0V
Output Leakage Current Low	I _{LOL}			-10	μA	V _O = +0.4V CE ₁ = +2.0V
Power Supply Current	I _{CC1}			+60	mA	V _I = +5.25V I _O = 0 mA T _a = +25°C *
Power Supply Current	I _{CC2}			+70	mA	V _I = +5.25V I _O = 0 mA T _a = -10°C to +70°C

AC CHARACTERISTICS

READ CYCLE

T_a = -10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Read Cycle Time	t _{RC}	450			350			250			ns
Access Time	t _A			450			350			250	ns
Chip Enable to Output	t _{CO}			180			150			130	ns
Output Disable to Output	t _{OD}			150			130			120	ns
Data Output to High Z State	t _{DF*}	0		130	0		115	0		100	ns
Previous Read Data Valid After Change of Address	t _{OH}	40			40			40			ns

*t_{DF} is with respect to the trailing edge of \overline{CE}_1 , CE₂, or OD, whichever occurs first.

WRITE CYCLE

T_a = -10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Write Cycle Time	t _{WC}	450			350			250			ns
Write Delay	t _{AW}	20			20			20			ns
Chip Enable to Write	t _{CW}	180			150			130			ns
Data Setup Time	t _{DW}	180			150			130			ns
Data Hold Time	t _{DH}	0			0			0			ns
Write Pulse Width	t _{WP}	160			130			120			ns
Write Recovery	t _{WR}	0			0			0			ns
Output Disable Setup	t _{DS}	20			20			10			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

T_a = -10°C to +70°C

STANDBY CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. ^①	MAX.		
V _{CC} in Standby	V _{PD}	1.5			V	
\overline{CE}_1 Bias in Standby	V _{CES}	2.0			V	2.0V ≤ V _{PD} ≤ 5.25V
		V _{PD}			V	1.5V ≤ V _{PD} < 2.0V
Standby Current Drain	I _{PD1}		24	36	mA	All Inputs = V _{PD1} = 1.5V
Standby Current Drain	I _{PD2}		30	45	mA	All Inputs = V _{PD2} = 2.0V
Chip Deselect to Standby Time	t _{CP}	0			ns	
Standby Recovery Time	t _R		t _{RC} ^②		ns	

Notes: ① Typical values are for T_a = 25°C and nominal supply voltage.

② t_R = t_{RC} (Read Cycle Time).

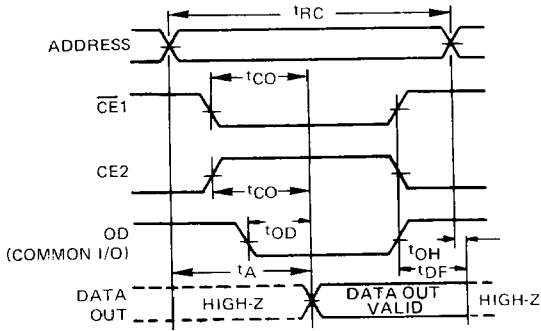
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CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C _{IN}			8	pf	V _I = 0V
Output Capacitance	C _{OUT}			12	pf	V _O = 0V

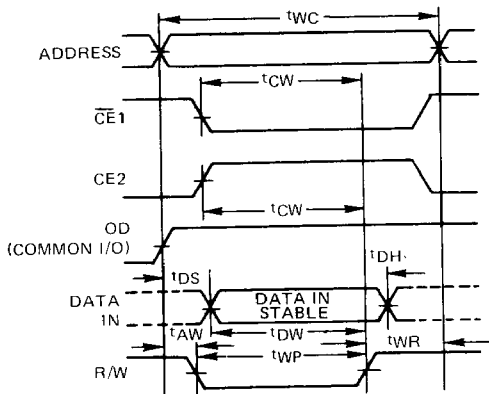
READ CYCLE

TIMING WAVEFORMS



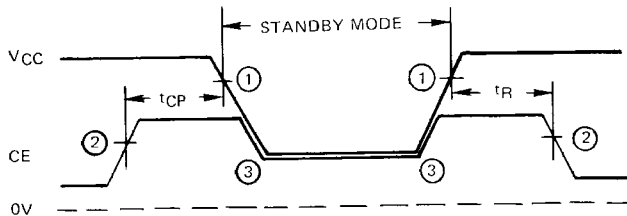
- Notes: ① OD should be tied low for separate I/O operation.
 ② R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS



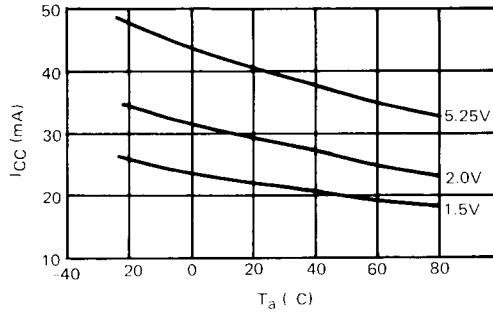
- Notes: ① 4.75V
 ② 2.0V
 ③ 1.5V

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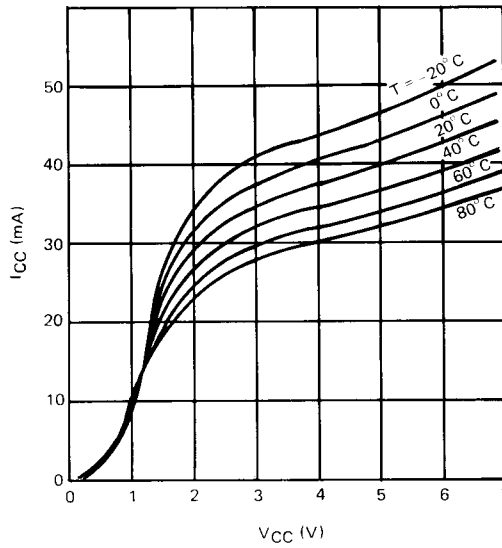
Input Pulse Levels	+0.8V to +2.0V	AC CONDITIONS OF TEST
Input Pulse Rise and Fall Times	20 ns	
Timing Measurement Reference Level	1.5V	
Output Load	1 TTL + 100 pF	

TYPICAL OPERATING CHARACTERISTICS

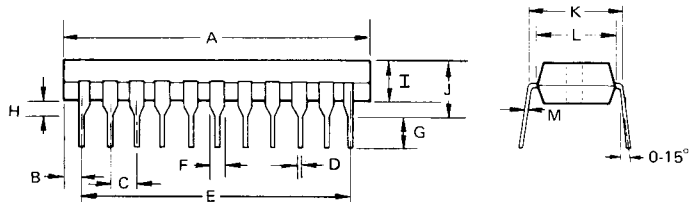
I_{CC} VS T_a



I_{CC} VS V_{CC}



PACKAGE OUTLINE
μPD2101ALC



ITEM	MILLIMETERS	INCHES
A	28.0 MAX	1.10 MAX
B	1.4 MAX	0.025
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.7 MAX	0.18 MAX
J	6.7 MAX	0.26 MAX
K	10.16	0.40
L	8.5	0.33
M	0.25 ^{+0.10} _{0.05}	0.01 ^{+0.004} _{0.002}

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