LINEAR SYSTEMS

SST5912
MONOLITHIC DUAL
N-CHANNEL JFET

micross

Linear Systems replaces discontinued Siliconix & National SST5912

The SST5912 are monolithic dual JFETs. The monolithic dual chip design reduces parasitics and gives better performance at very high frequencies while ensuring extremely tight matching. These devices are an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications. The SST5912 is a direct replacement for discontinued Siliconix and National SST5912.

The 8 Pin SOIC provides ease of manufacturing, and the symmetrical pinout prevents improper orientation. (See Packaging Information).

SST5912 Applications:

- Wideband Differential Amps
- High-Speed,Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES	
Improved Direct Replacement for SILICONIX & NATIONAL SST5912	
LOW NOISE (10KHz)	e_n~ 4nV/√Hz
HIGH TRANSCONDUCTANCE (100MHz)	g_{fs} ≥ 4000µS

ABSOLUTE MAXIMUM RATINGS [1]
@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	-55°C to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation (Total)	500mW
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain	-25V
Gate to Source	-25V

MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\|V_{GS1} - V_{GS2}\|$	Differential Gate to Source Cutoff Voltage	--	--	15	mV	V_{DG} = 10V, I_D = 5mA
$\Delta\|V_{GS1} - V_{GS2}\| / \Delta T$	Differential Gate to Source Cutoff Voltage Change with Temperature	--	--	40	µV/°C	V_{DG} = 10V, I_D = 5mA T_A = -55°C to +125°C
I_{DSS1} / I_{DSS2}	Gate to Source Saturation Current Ratio	0.95	--	1	%	V_{DS} = 10V, V_{GS} = 0V
$\|I_{G1} - I_{G2}\|$	Differential Gate Current	--	--	20	nA	V_{DG} = 10V, I_D = 5mA T_A = +125°C
g_{fs1} / g_{fs2}	Forward Transconductance Ratio[2]	0.95	--	1	%	V_{DS} = 10V, I_D = 5mA, f = 1kHz
CMRR	Common Mode Rejection Ratio	--	85	--	dB	V_{DG} = 5V to 10V, I_D = 5mA

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-25	--		V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-1	--	-5		V_{DS} = 10V, I_D = 1nA
$V_{GS(F)}$	Gate to Source Forward Voltage	--	0.7	--		I_G = 1mA, V_{DS} = 0V
V_{GS}	Gate to Source Voltage	-0.3	--	-4		V_{DG} = 10V, I_G = 5mA
I_{DSS}	Gate to Source Saturation Current[3]	7	--	40	mA	V_{DS} = 10V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current[3]	--	-1	-50	pA	V_{GS} = -15V, V_{DS} = 0V
I_G	Gate Operating Current	--	-1	-50		V_{DG} = 10V, I_D = 5mA
g_{fs}	Forward Transconductance	4000	--	10000	µS	V_{DG} = 10V, I_D= 5mA
		4000	--	10000		
g_{os}	Output Conductance	--	--	100		
		--	--	150		
C_{ISS}	Input Capacitance	--	--	5	pF	V_{DG} = 10V, I_D = 5mA, f = 1MHz
C_{RSS}	Reverse Transfer Capacitance	--	--	1.2		
NF	Noise Figure	--	--	1	dB	V_{DG} = 10V, I_D = 5mA, f = 10kHz, R_G = 100KΩ
e_n	Equivalent Input Noise Voltage	--	7	20	nV/√Hz	V_{DG} = 10V, I_D = 5mA, f = 100Hz
		--	4	10		V_{DG} = 10V, I_D = 5mA, f = 10kHz

Notes: 1. Absolute Maximum ratings are limiting values above which serviceability may be impaired 2. Pulse Test: PW ≤ 300µs Duty Cycle ≤ 3%
3. Assumes smaller value in numerator

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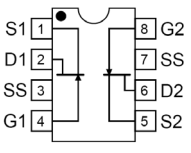
Please contact Micross for full package and die dimensions:

Email: chipcomponents@micross.com
Web: www.micross.com/distribution.aspx

Available Packages:

SST5912 in SOIC
SST5912 available as bare die

SOIC-A



SOIC-B