NEC

TFT COLOR LCD MODULE

NL3224AC35-06

13.9cm (5.5 Type)
QVGA

DATA SHEET

(4th edition)

All information is subject to change without notice.

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INTRODUCTION

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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Military systems, aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems (medical equipment, etc.) and any other equipment

The quality grade of this product is ***"Standard"*** unless otherwise specified in this document. If customers intend to use this product for applications other than those specified for ***"Standard"*** quality grade, they should contact NEC Corporation sales representative in advance.

Anti-radioactive design is not implemented in this product.

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CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

NL3224AC35-06 module is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight unit.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATIONS

- Car navigation system
- Display terminal for control system

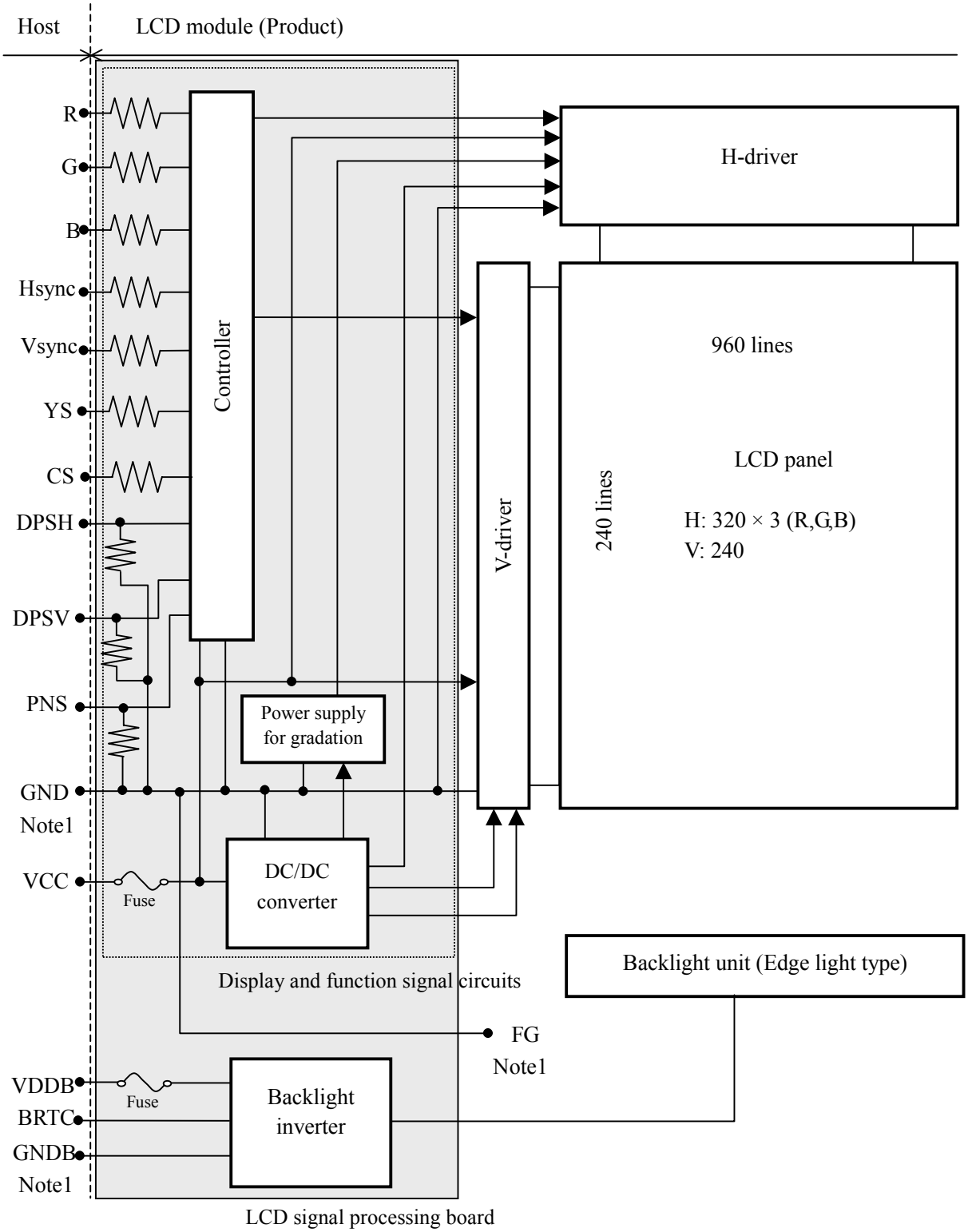
1.3 FEATURES

- High luminance
- Low reflection
- Analog RGB signals
- Select of pixel number (Select function of vertical display line)
- Reversible-scan direction
- Edge light type

2. GENERAL SPECIFICATIONS

Display area	111.4 (W) × 83.5 (H) mm (typ.)
Diagonal size of display	13.9 cm (5.5 inches)
Drive system	a-Si TFT active matrix
Display color	Full color
Pixel	*At QVGA display mode* 320 (H) × 240 (V) pixels *At QVGA- display mode* 320 (H) × 234 (V) pixels
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe
Dot pitch	0.1160 (W) × 0.3480 (H) mm
Pixel pitch	0.3480 (W) × 0.3480 (H) mm
Module size	134.0 (W) × 110.0 (H) × 16.0 (D) mm (typ.)
Weight	285 g (typ.)
Contrast ratio	85:1 (typ.)
Viewing angle	*At the contrast ratio 10:1* • Horizontal: Left side 50° (typ.), Right side 50° (typ.) • Vertical: Up side 25° (typ.), Down side 25° (typ.)
Designed viewing direction	*At DPSH: normal scan and DPSV: normal scan* • Viewing direction without image reversal: up side (2 and 10 o'clock) • Viewing direction with contrast peak: down side 0° to 5° (6 o'clock) • Viewing angle with optimum grayscale (γ=2.2): normal axis
Polarizer surface	Antiglare treatment
Polarizer pencil-hardness	2H (min.) [by JIS K5400]
Color gamut	*At LCD panel center* 50 % (typ.) [against NTSC color space]
Response time	16 ms (typ.)
Luminance	250 cd/m^2 (typ.)
Signal system	Analog RGB signals, Dot clock (CLK), Composite video-synchronous signal (CS), Horizontal synchronous signal (Hsync), Vertical synchronous signal (Vsync)
Supply voltage	Display and function signal circuits: 9.5V Backlight inverter: 9.5V
Backlight	Edge light type: 1 cold cathode fluorescent lamps Replaceable parts • Lamps for backlight unit: Type No. 55LHS-3L • Signal processing board: Type No. 55PWB22
Power consumption	*At maximum luminance and checkered flag pattern* 8.0 W (typ.)

3. BLOCK DIAGRAM



Note1: GND is connected to FG (Frame ground). GNDB is not connected to FG. GND and GNDB should be connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	134.0 ± 0.5 (W) × 110.0 ± 0.5 (H) × 16.0 ± 0.5 (D)	Note1	mm
Display area	111.4 ± 0.5 (W) × 83.5 ± 0.5 (H)	Note1	mm
Weight	285 (typ.), 330 (max.)		g

Note1: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	Display and function signal circuits	VCC	-0.5 to +20.0	V	Ta = 25°C
	Backlight inverter	VDDB	-0.5 to +20.0	V	
Input voltage for signals	Display signals for visual Note1	VDV	-2.5 to +2.5	V	
	Function signals Note2	VF	-0.5 to +5.5	V	
	BRTC signal	VBC	-0.5 to +5.5	V	Ta = 25°C VDDB = 9.5V
Output voltage for signals	Display signals for sync Note3	VDS	-0.5 to +5.5	V	-
Storage temperature		Tst	-40 to +95	°C	
Operating temperature	Front surface	TopF	-30 to +85	°C	
	Rear surface	TopR	-30 to +85	°C	
Relative humidity Note4		RH	≤ 95	%	Ta ≤ 55°C
			≤ 90	%	55 < Ta ≤ 60°C
			≤ 76	%	60 < Ta ≤ 65°C
			≤ 64	%	65 < Ta ≤ 70°C
			≤ 55	%	70 < Ta ≤ 75°C
			≤ 46	%	75 < Ta ≤ 80°C
			≤ 40	%	80 < Ta ≤ 85°C
Absolute humidity Note4		AH	≤ 44 Note5	g/m^3	Ta > 85°C

Note1: Display signals for visual are CLK, CS, YS, R, G and B.

Note2: Function signals are DPSH, DPSV, PNS, CD, CH, CB, SIR, SIG and SIB.

Note3: Display signals for syncs are Hsync and Vsync

Note4: No condensation

Note5: Ta = 85°C, RH = 40%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Driving for display and function signal circuits on LCD signal processing board

(Ta = 25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply voltage		VCC	8.5	9.5	10.5	V	-
Power supply current		ICC	-	200 Note1	300	mA	VCC = 9.5V
Input voltage for YS signals		VDVY	-	1.0	-	V	CMOS level
Input voltage for CS signals		VDVC	-	1.0	-	V	Impedance = 75Ω
Input voltage for CLK signals	Low	VDVKL	0	-	0.9	V	CMOS level
	High	VDVKH	3.2	-	5.0	V	
Input voltage for DPSH or DPSV signals	Low	VFDL	0	-	0.9	V	
	High	VFDH	3.2	-	5.0	V	
Input voltage for PNS signal	Low	VFPL	0	-	0.9	V	
	High	VFPH	3.2	-	5.0	V	
Input voltage for CD, CH or CB signals	Low	VFCL	0	-	0.9	V	
	High	VFCH	3.2	-	5.0	V	
Input voltage for SIR, SIG or SIB signals	Low	VFSL	0	-	0.9	V	
	High	VFSH	3.2	-	5.0	V	
Output voltage for Hsync or Vsync signals	Low	VDSL	0	-	0.3	V	
	High	VDSH	0.75	-	1.0	V	

Note1: Checkered flag pattern [by EIAJ ED-2522]

4.3.2 Driving for backlight inverter on LCD signal processing board

(Ta = 25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply voltage		VDDB	8.5	9.5	10.5	V	-
Power supply current		IDDB	-	640	800	mA	at maximum luminance, VDDB = 9.5V Note1
Input voltage for BRTC signal	Low	VBCL	0	-	0.5	V	-
	High	VBCH	1.2	-	3.5	V	

Note1: The power supply lines (VDDB and GNDB) occurs large ripple voltage while luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power source lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit.

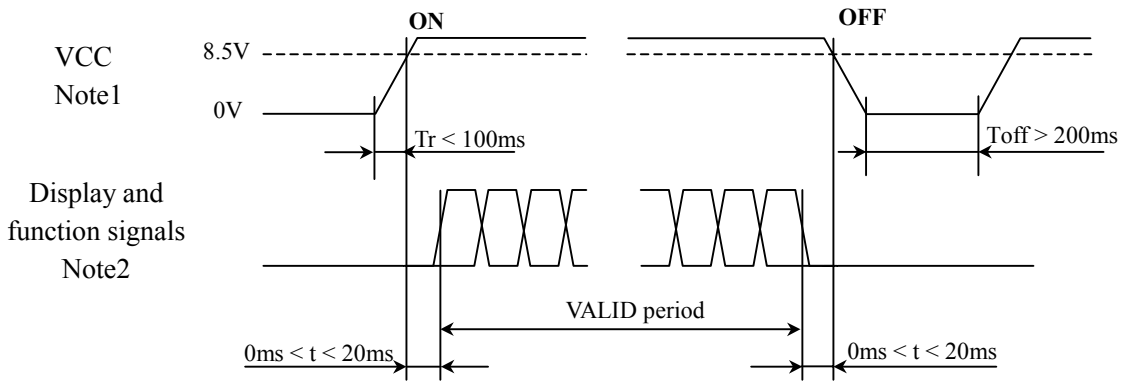
4.3.3 Fuses

Fusing line	Fuse		Rating	Fusing current Note1
	Type	Supplier		
VCC	CCP2E25TE	KOA Corporation	1.0 A	2.5 A
			72 V	
VDDB	CCP2E25TE	KOA Corporation	1.0 A	2.5 A
			72 V	

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

4.4 SUPPLY VOLTAGE SEQUENCE

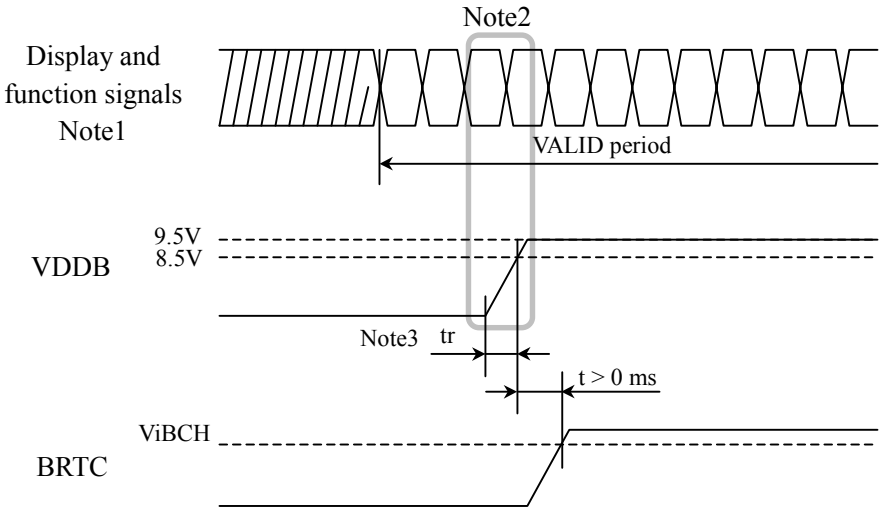
4.4.1 Sequence for display and function signal circuits on LCD signal processing board



Note1: In terms of voltage variation (voltage drop) while VCC rising edge is below 8.5V in "VCC = 9.5V", a protection circuit may work, and then this product may not work.

Note2: Display (CLK, CS, YS, Hsync, Vsync, R, G, B) and function (DPSH, DPSV, PNS, CD, CH, CB, SIR, SIG, SIB) signals must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.
If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VCC.

4.4.2 Sequence for backlight inverter on LCD signal processing board



Note1: These are the display and function signals for LCD signal processing board.

Note2: The backlight power voltage (VDDB) should be inputted within the valid period of display signals, in order to avoid unstable data display.

Note3: The tr should be less than 800ms when BRTC terminal [Socket: CN1, Pin No.: 1] (See "4.5.1 Display signal circuits and backlight inverter on LCD signal processing board ".) is Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

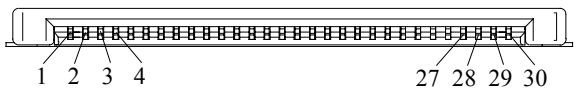
4.5.1 Display signal circuits and backlight inverter on LCD signal processing board

CN1 socket (LCD module side): IL-402-30S-S1L-SA (Japan Aviation Electronics Industry Limited)
Adaptable plug: SUMI CARD 1.0mm pitches, 30 lines (Sumitomo Electric Industries, Ltd.)

Pin No.	Symbol	Signal	Remarks
1	BRTC	Backlight ON/OFF signal	ON: 1.2V (Dark) to 3.5V (Bright), OFF: less than 0.5V
2	VDDB	Power supply for backlight	-
3	VDDB	Power supply for backlight	
4	GNDB	Backlight inverter ground	
5	GNDB	Backlight inverter ground	
6	GND	Ground	
7	GND	Ground	
8	VCC	Power supply	
9	VCC	Power supply	
10	CS	Composite video-synchronous	Signal level: 1.0Vp-p, 75Ω
11	GND	Ground	-
12	R	Red data	
13	GND	Ground	
14	G	Green data	
15	GND	Ground	
16	B	Blue data	
17	GND	Ground	
18	YS	Select of display signal mode	Analog RGB mode: High or Open, Composite mode: Low
19	NC	Non connection	-
20	NC	Non connection	
21	Vsync	Vertical synchronous output	
22	Hsync	Horizontal synchronous output	
23	DCO	DC output voltage	DC +5.0V output
24	CD	Control of color depth	0V (Pale) to 5.0V (Deep) Note1
25	CH	Control of hue	0V (Red-tinged) to 5.0V (Green-tinged) Note1
26	CB	Control of color brightness	0V (Bright) to 5.0V (Dark) Note1
27	GND	Ground	-
28	SIR	Superimpose for red data	ON: High, OFF: Low or Open
29	SIG	Superimpose for green data	
30	SIB	Superimpose for blue data	

Note1: This function can use only when composite mode. These terminals should be open when using of analog RGB mode.

CN1: Figure of socket



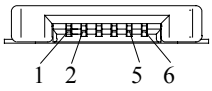
4.5.2 Function signal circuits on LCD signal processing board

CN2 socket (LCD module side): IL-402-6S-S1L-SA (Japan Aviation Electronics Industry Limited)
Adaptable plug: SUMI CARD 1.0mm pitches, 6 lines (Sumitomo Electric Industries, Ltd.)

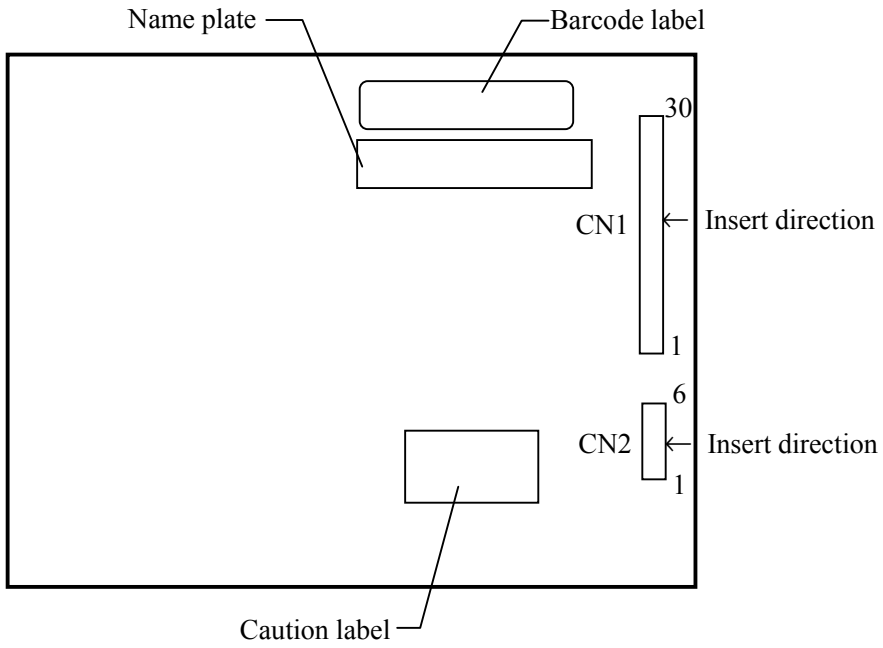
Pin No.	Symbol	Signal	Remarks
1	GND	Ground	-
2	DPSH	Select of scan direction (Horizontal)	Normal scan: Low or Open. Reverse scan: High Note1
3	DPSV	Select of scan direction (Vertical)	
4	PNS	Select of pixel number	QVGA mode: High, QVGA- mode: Low or Open
5	NC	Non connection	-
6	GND	Ground	

Note1: See "4.7 SCANNING DIRECTIONS".

CN2: Figure of socket



4.5.3 Positions of sockets



4.6 DISPLAY POSITIONS

The following table is the coordinates per pixel (See figure of "4.7 SCANNING DIRECTIONS".).

C(0, 0)	C(1, 0)	•••	C(X, 0)	•••	C(318, 0)	C(319, 0)
C(0, 1)	C(1, 1)	•••	C(X, 1)	•••	C(318, 1)	C(319, 1)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
C(0, Y)	C(1, Y)	•••	C(X, Y)	•••	C(318, Y)	C(319, Y)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
C(0,238)	C(1,238)	•••	C(X,238)	•••	C(318,238)	C(319,238)
C(0,239)	C(1,239)	•••	C(X,239)	•••	C(318,239)	C(319,239)

4.7 SCANNING DIRECTIONS

4.7.1 QVGA display mode

The following figures are seen from a front view. Also the arrow shows the direction of scan.

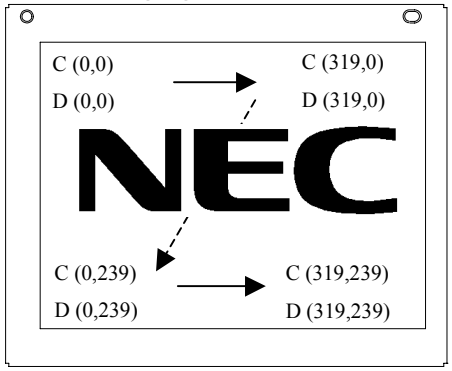


Figure 1. DPSH: Normal scan, DPSV: Normal scan

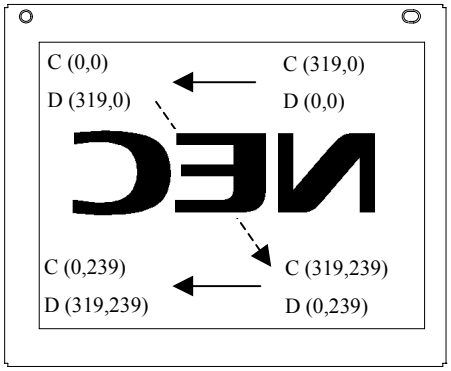


Figure 2. DPSH: Reverse scan, DPSV: Normal scan

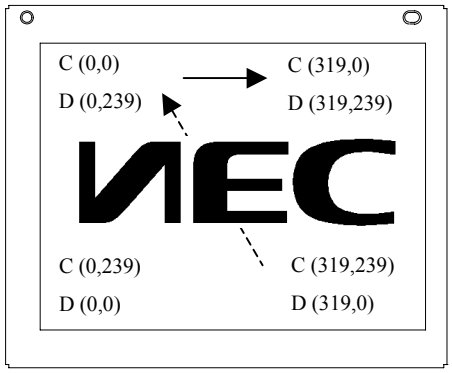


Figure 3. DPSH: Normal scan, DPSV: Reverse scan

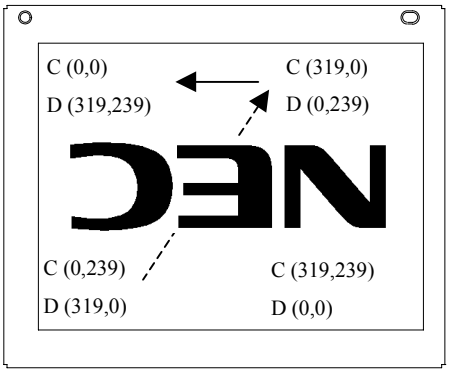


Figure 4. DPSH: Reverse scan, DPSV: Reverse scan

Note1: Meaning of C (X, Y) and D (X, Y)

C (X, Y): The coordinates of the display position (See "4.6 DISPLAY POSITIONS".)

D (X, Y): The data number of QVGA input signal for LCD signal processing board

Note2: Normal scan: Low or Open, Reverse scan: High

4.7.2 QVGA- display mode

The following figures are seen from a front view. Also the arrow shows the direction of scan.

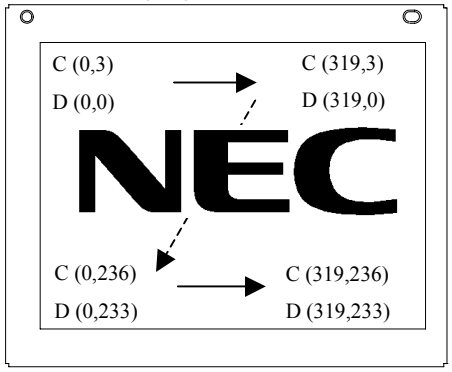


Figure 1. DPSH: Normal scan, DPSV: Normal scan

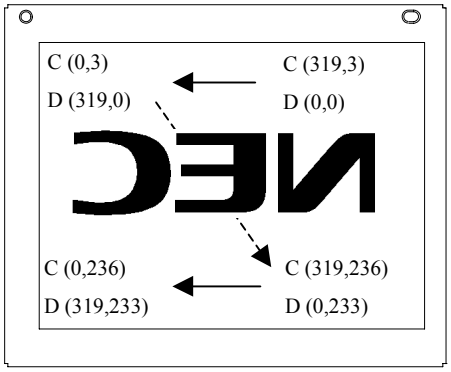


Figure 2. DPSH: Reverse scan, DPSV: Normal scan

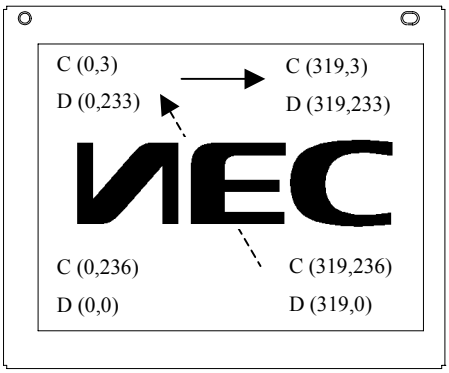


Figure 3. DPSH: Normal scan, DPSV: Reverse scan

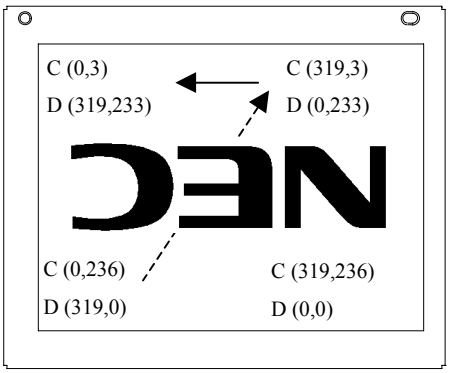


Figure 4. DPSH: Reverse scan, DPSV: Reverse scan

Note1: Meaning of C (X, Y) and D (X, Y)

C (X, Y): The coordinates of the display position (See "4.6 DISPLAY POSITIONS".)

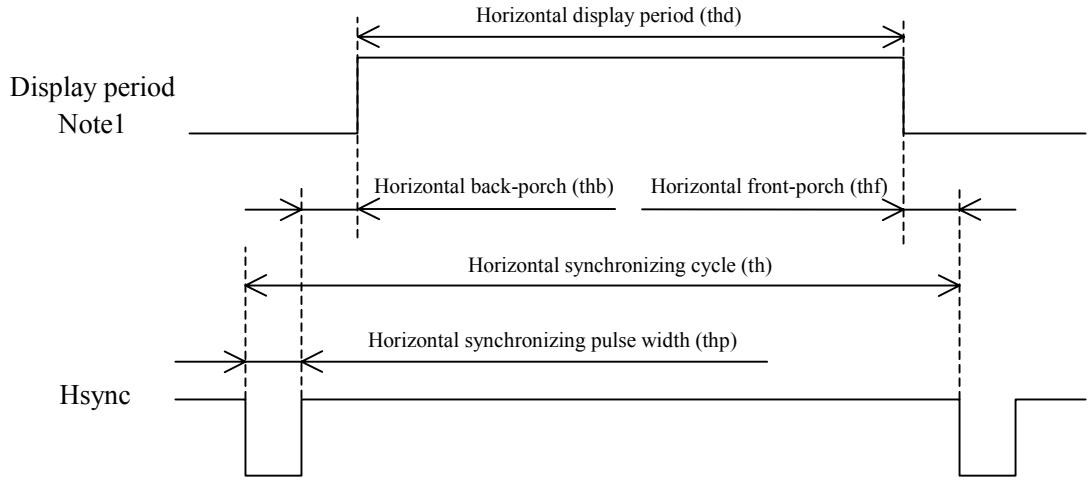
D (X, Y): The data number of QVGA- input signal for LCD signal processing board

Note2: Normal scan: Low or Open, Reverse scan: High

4.8 INPUT SIGNAL TIMINGS FOR DISPLAY SIGNAL ON SIGNAL PROCESSING BOARD

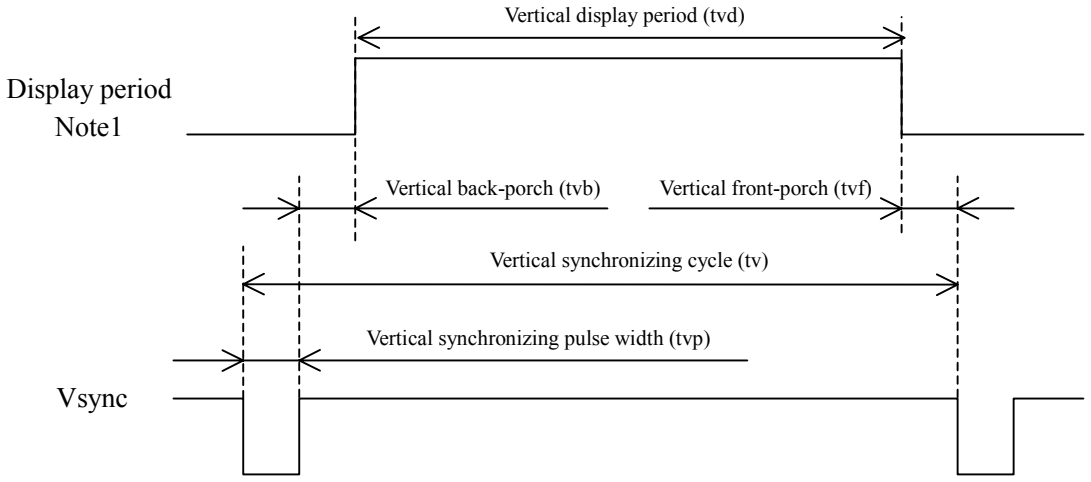
4.8.1 Outline of input signal timings for analog RGB mode

• Horizontal signal



Note1: This diagram indicates virtual signal for set up to timing.

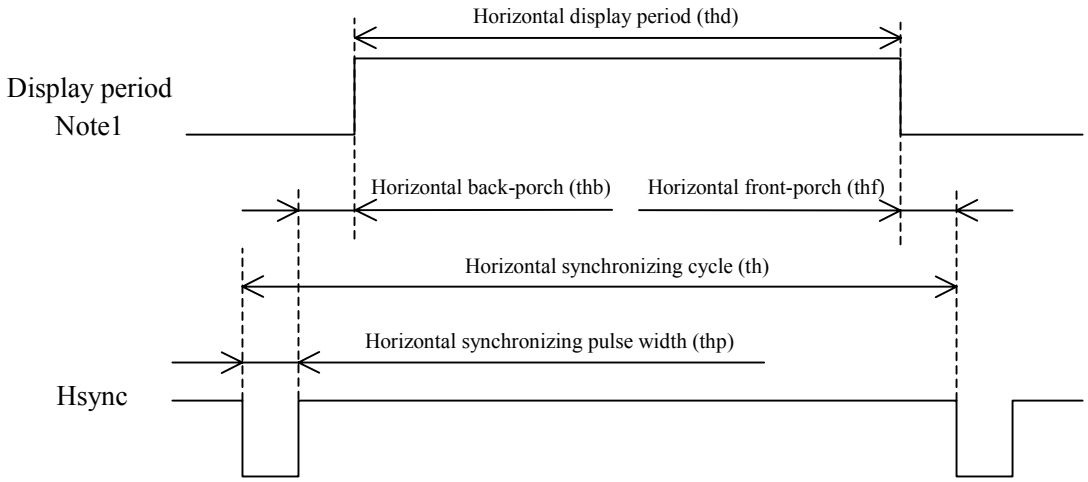
• Vertical signal



Note1: This diagram indicates virtual signal for set up to timing.

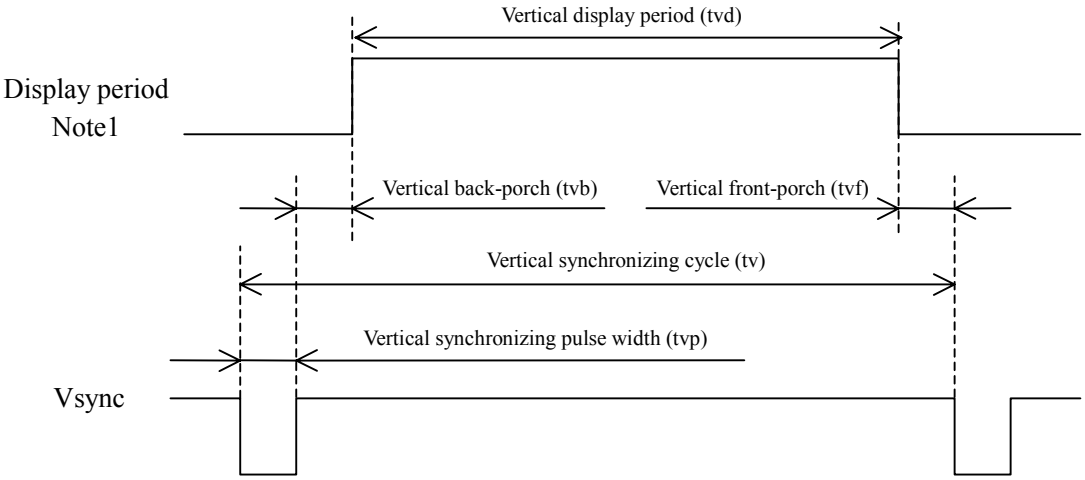
4.8.2 Outline of input signal timings for composite mode

- Horizontal signal



Note1: This diagram indicates virtual signal for set up to timing.

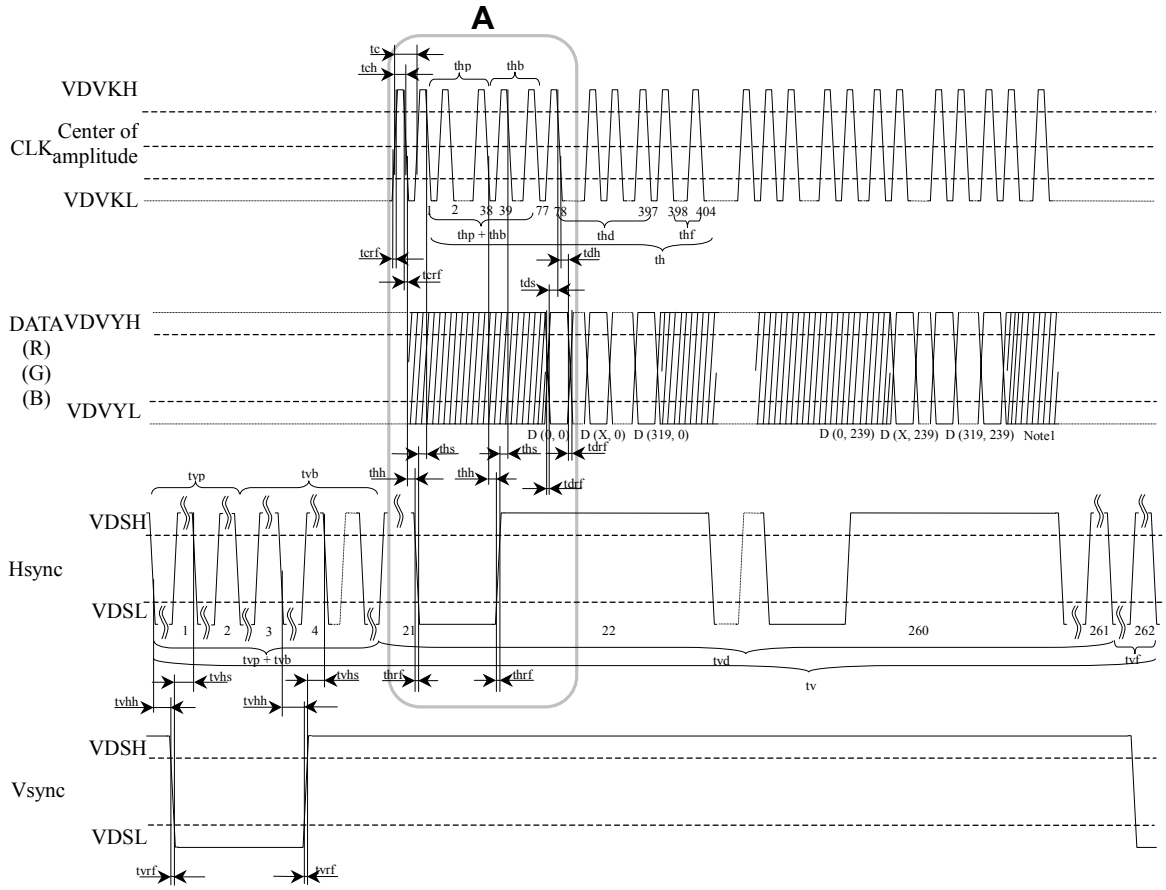
- Vertical signal



Note1: This diagram indicates virtual signal for set up to timing.

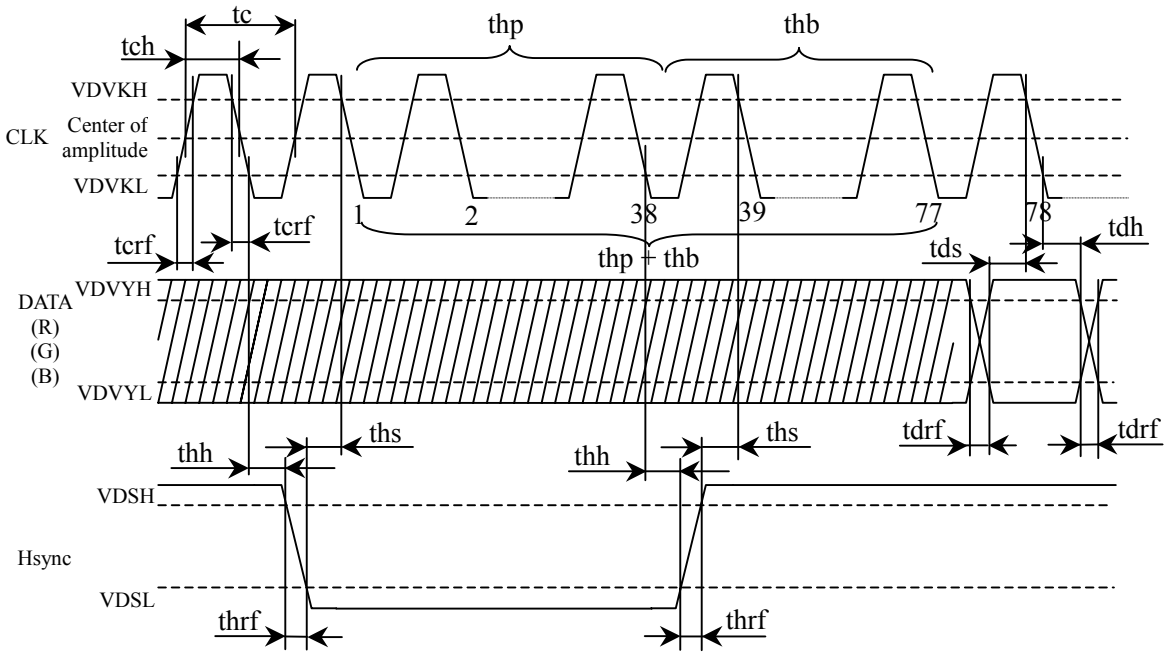
4.8.3 Detailed QVGA input signal timing chart for analog RGB mode

• Outline chart



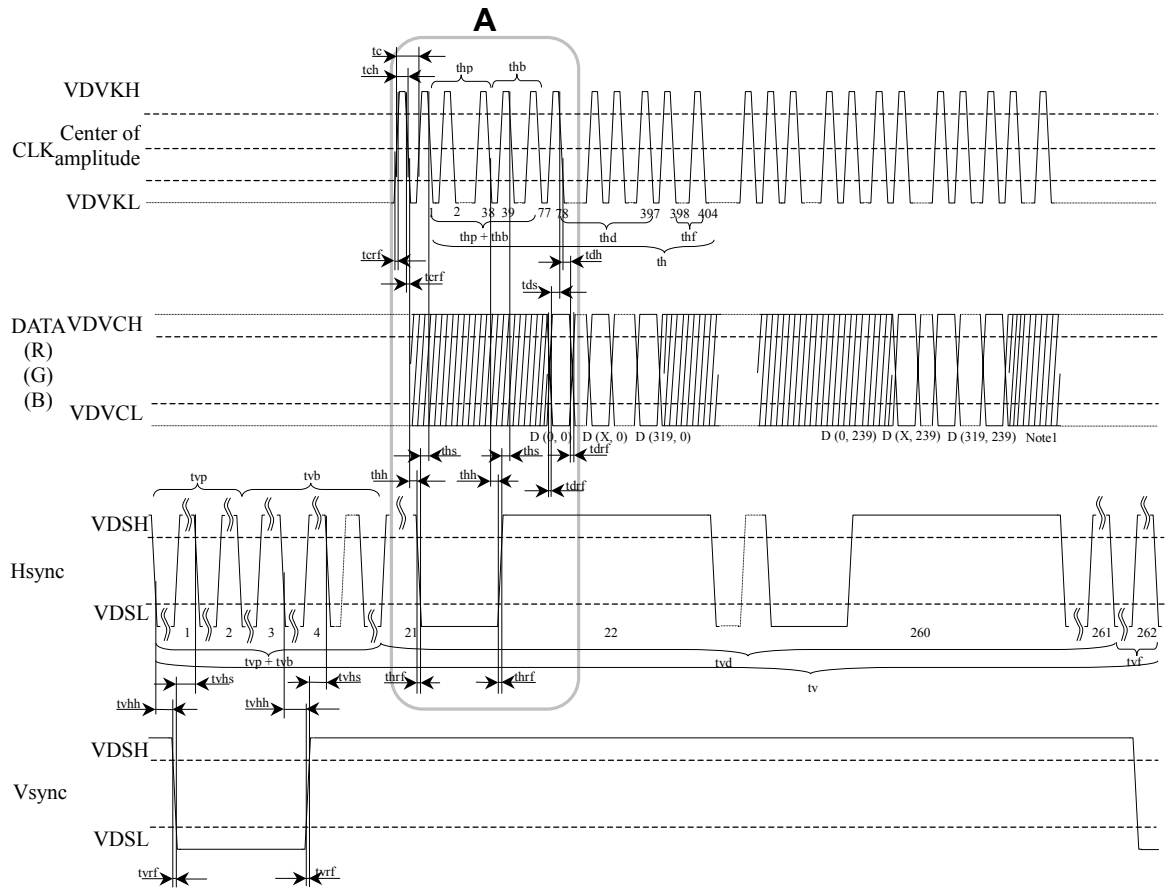
Note1: X is data number from 1 to 318. See "4.7.1 QVGA display mode".

• Detail of **A** part



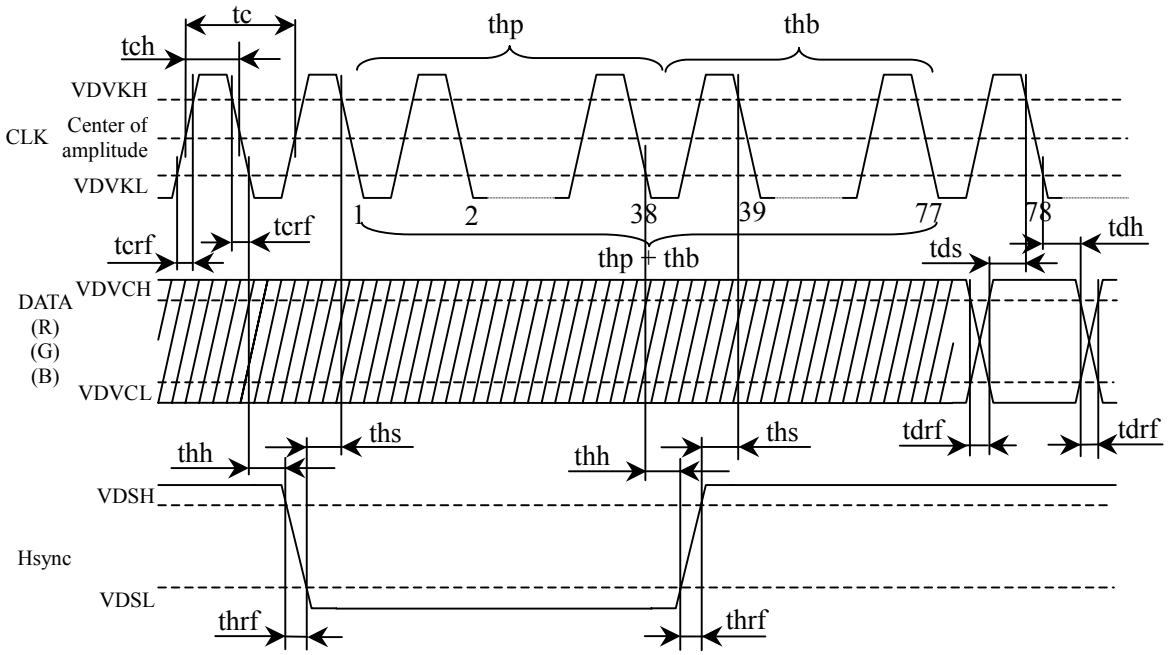
4.8.4 Detailed QVGA input signal timing chart for composite mode

• Outline chart



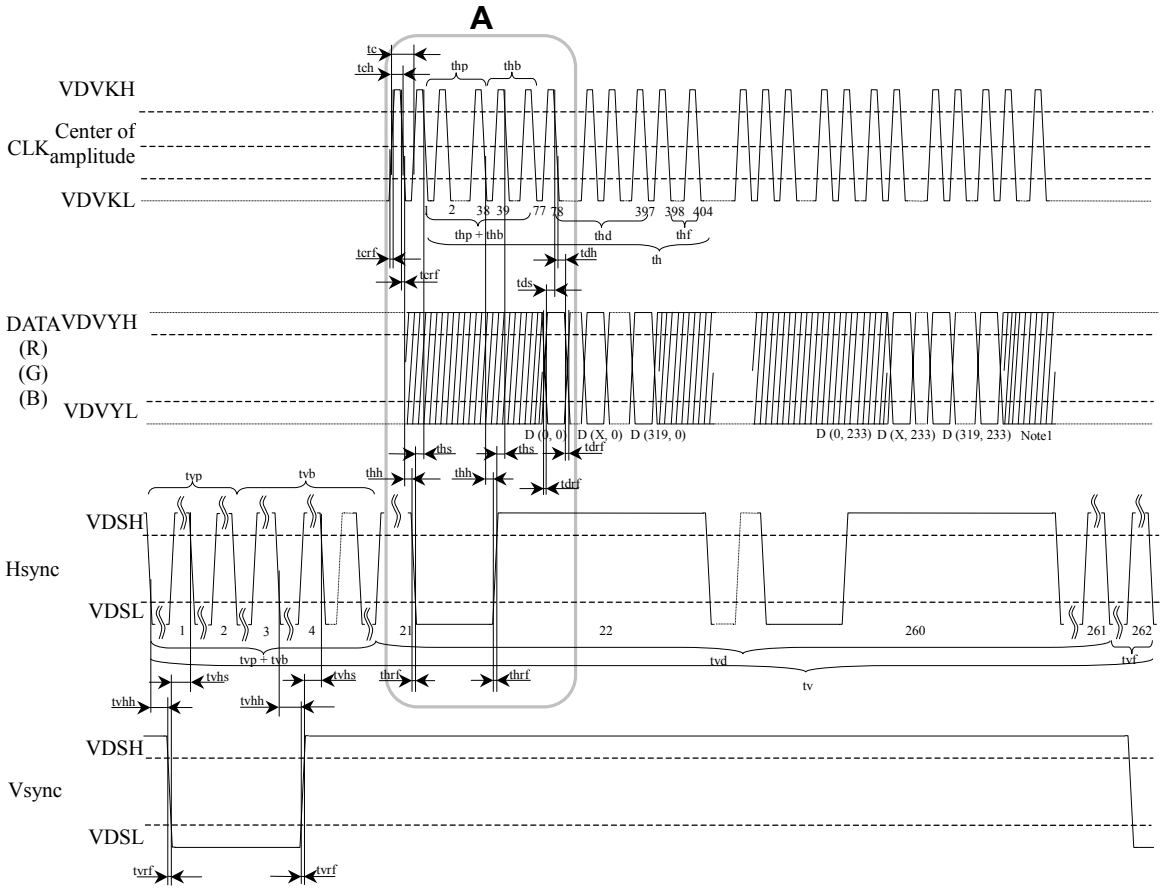
Note1: X is data number from 1 to 318. See "4.7.1 QVGA display mode".

• Detail of **A** part



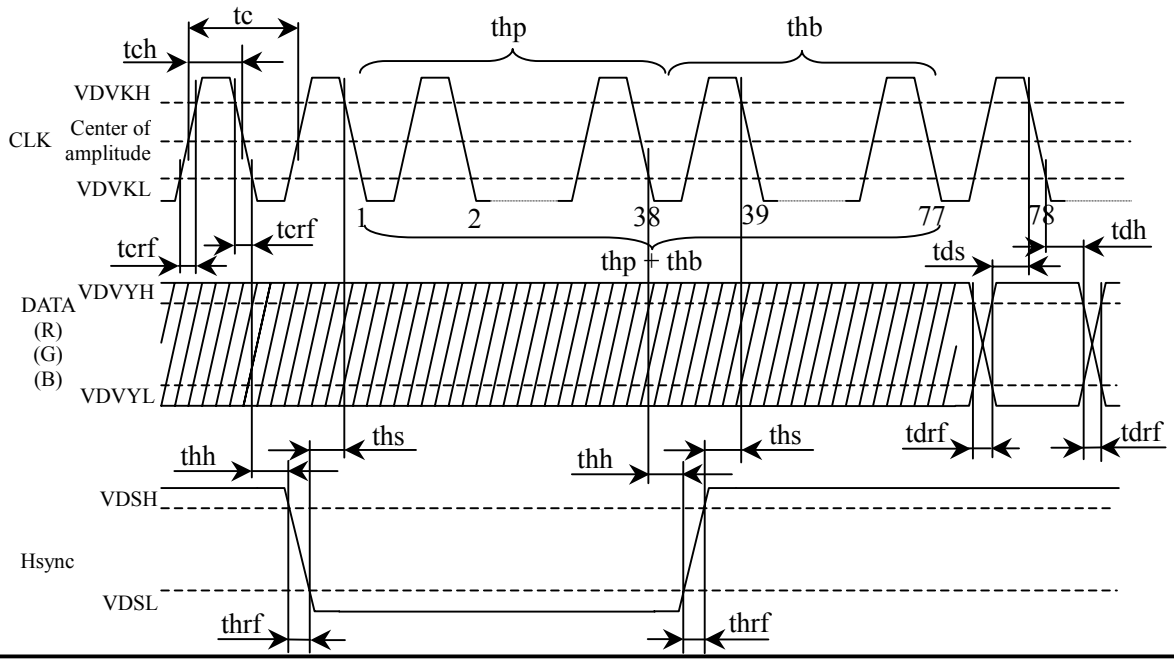
4.8.5 Detailed QVGA- input signal timing chart for analog RGB mode

- Outline chart



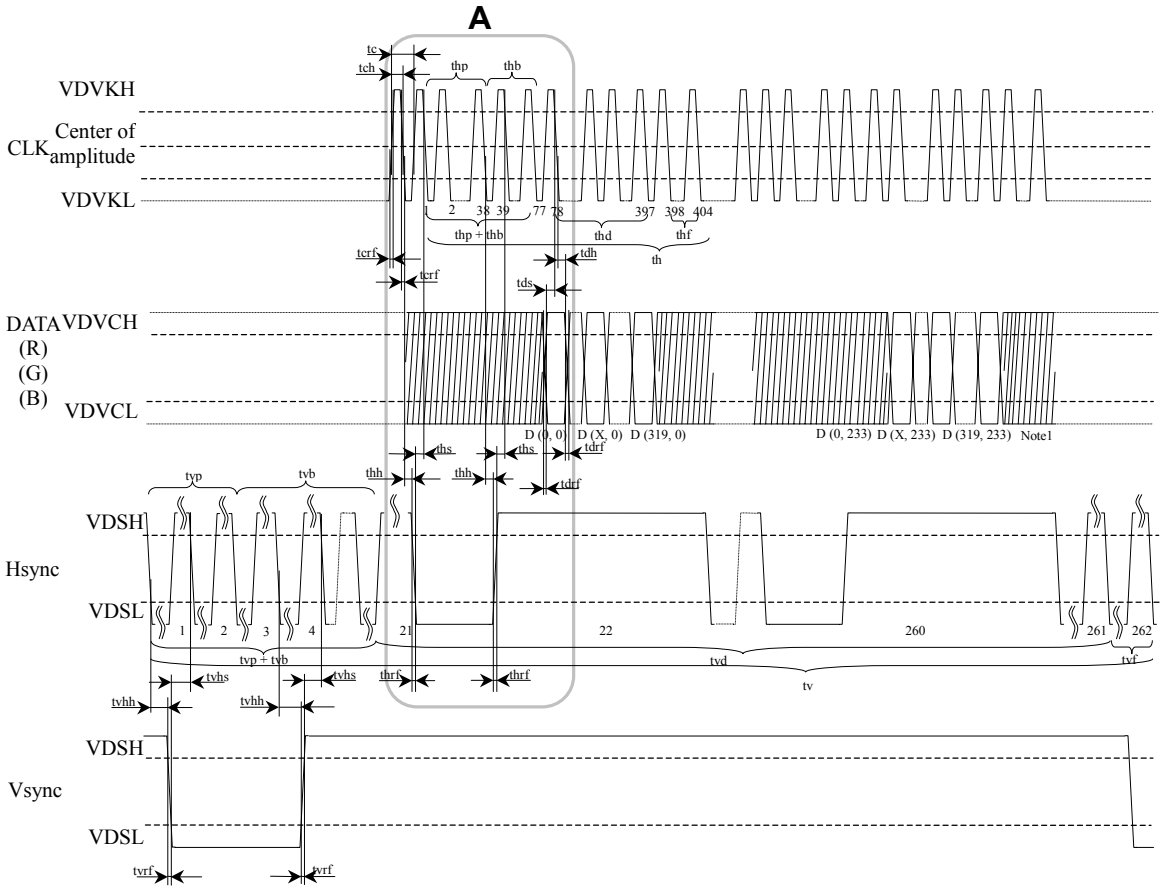
Note1: X is data number from 1 to 318. See "4.7.2 QVGA- display mode".

- Detail of **A** part



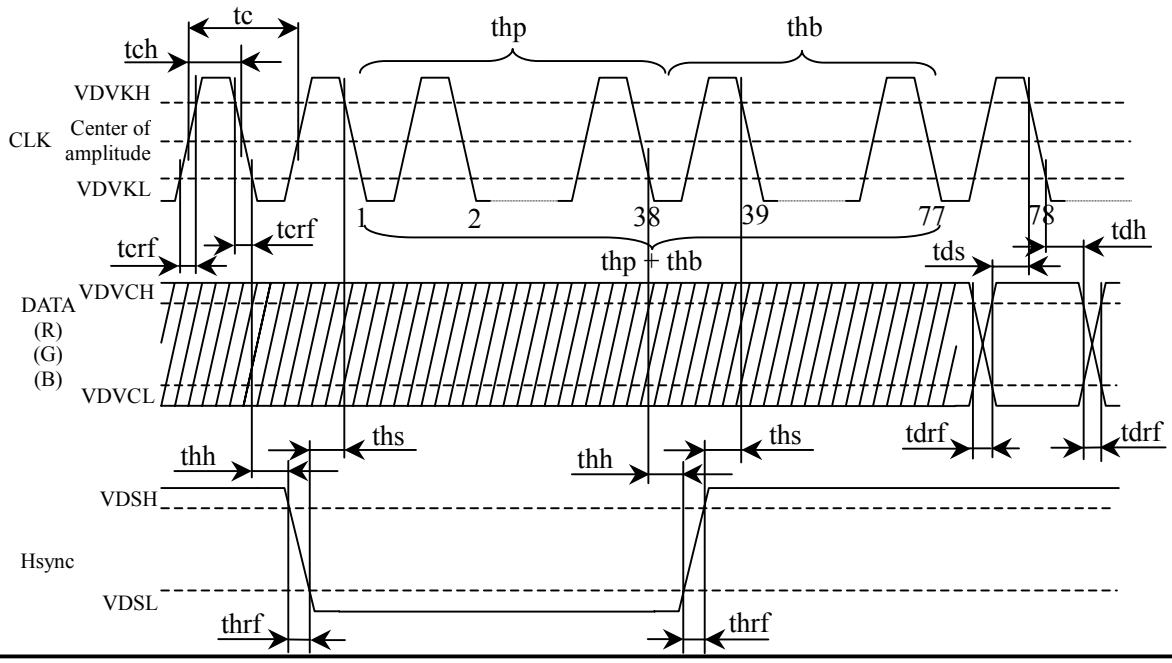
4.8.6 Detailed QVGA- input signal timing chart for composite mode

• Outline chart



Note1: X is data number from 1 to 318. See "4.7.2 QVGA- display mode".

• Detail of **A** part



4.8.7 Timing characteristics of QVGA display for analog RGB mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency		tcf	-	6.4	-	MHz	157.3 ns (typ.) Note1
	Duty		tcd	0.4	-	0.6	-	Note1
	Rise time, Fall time		tcrf	-	-	10	ns	-
DATA	CLK-DATA	Setup time	tds	10	-	-	ns	
		Hold time	tdh	10	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	
Hsync	Cycle		th	61.7	63.6	65.5	μs	31.4 kHz (typ.)
				404			CLK	Note2
	Display period		thd	320			CLK	
	Front-porch		thf	7			CLK	
	Pulse width		thp	-	38	-	CLK	
	Back-porch		thb	-	39	-	CLK	
	Total of pulse width and back-porch		thp + thb	77			CLK	Note2, Note3
	CLK- Hsync	Setup time	ths	10	-	-	ns	-
		Hold time	thh	10	-	-	ns	
	Rise time, Fall time		thrf	-	-	10	ns	
Vsync	Cycle		tv	15.8	16.7	17.5	ms	59.9 Hz (typ.)
				262			H	Note2
	Display period		tvd	240			H	
	Front-porch		tvf	1			H	
	Pulse width		tvp	2	-	20	H	
	Back-porch		tvb	1	-	19	H	
	Total of pulse width and back-porch		tvp + tvb	21			H	Note2, Note3
	Vsync-Hsync	Setup time	tvhs	10	-	-	ns	Note2
		Hold time	tvhh	1	-	-	CLK	-
	Rise time, Fall time		tvrf	-	-	10	ns	

Note1: Definition of parameters is as follows.

tcf = 1/tc, tcd = tch/tc = tch×tcd

Note2: Definition of parameters is as follows.

tc = 1CLK, th = 1H

Note3: Keep tvp + tvb and thp + thb within the table. If it is out of specification, display position will be shifted to right/left side or up/down.

4.8.8 Timing characteristics of QVGA display for composite mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency		tcf	-	6.4	-	MHz	157.3 ns (typ.) Note1
	Duty		tcd	0.4	-	0.6	-	Note1
	Rise time, Fall time		tcrf	-	-	10	ns	-
DATA	CLK-DATA	Setup time	tds	10	-	-	ns	
		Hold time	tdh	10	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	
Hsync	Cycle		th	61.7	63.6	65.5	μs	31.4 kHz (typ.)
				404			CLK	Note2
	Display period		thd	320			CLK	
	Front-porch		thf	7			CLK	
	Pulse width		thp	-	38	-	CLK	
	Back-porch		thb	-	39	-	CLK	
	Total of pulse width and back-porch		thp + thb	77			CLK	Note2, Note3
	CLK- Hsync	Setup time	ths	10	-	-	ns	-
		Hold time	thh	10	-	-	ns	
	Rise time, Fall time		thrf	-	-	10	ns	
Vsync	Cycle		tv	15.8	16.7	17.5	ms	59.9 Hz (typ.)
				262			H	Note2
	Display period		tvd	240			H	
	Front-porch		tvf	1			H	
	Pulse width		tvp	2	-	20	H	
	Back-porch		tvb	1	-	19	H	
	Total of pulse width and back-porch		tvp + tvb	21			H	Note2, Note3
	Vsync-Hsync	Setup time	tvhs	10	-	-	ns	Note2
		Hold time	tvhh	1	-	-	CLK	-
	Rise time, Fall time		tvrf	-	-	10	ns	

Note1: Definition of parameters is as follows.

tcf = 1/tc, tcd = tch/tc = tch×tcd

Note2: Definition of parameters is as follows.

tc = 1CLK, th = 1H

Note3: Keep tvp + tvb and thp + thb within the table. If it is out of specification, display position will be shifted to right/left side or up/down.

4.8.9 Timing characteristics of QVGA- display for analog RGB mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency		tcf	-	6.4	-	MHz	157.3 ns (typ.) Note1
	Duty		tcd	0.4	-	0.6	-	Note1
	Rise time, Fall time		tcrf	-	-	10	ns	-
DATA	CLK-DATA	Setup time	tds	10	-	-	ns	
		Hold time	tdh	10	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	
Hsync	Cycle		th	61.7	63.6	65.5	μs	31.4 kHz (typ.)
				404			CLK	Note2
	Display period		thd	320			CLK	
	Front-porch		thf	7			CLK	
	Pulse width		thp	-	38	-	CLK	
	Back-porch		thb	-	39	-	CLK	
	Total of pulse width and back-porch		thp + thb	77			CLK	Note2, Note3
	CLK- Hsync	Setup time	ths	10	-	-	ns	-
		Hold time	thh	10	-	-	ns	
	Rise time, Fall time		thrf	-	-	10	ns	
Vsync	Cycle		tv	15.8	16.7	17.5	ms	59.9 Hz (typ.)
				262			H	Note2
	Display period		tvd	234			H	
	Front-porch		tvf	1			H	
	Pulse width		tvp	2	-	20	H	
	Back-porch		tvb	1	-	19	H	
	Total of pulse width and back-porch		tvp + tvb	21			H	Note2, Note3
	Vsync-Hsync	Setup time	tvhs	10	-	-	ns	Note2
		Hold time	tvhh	1	-	-	CLK	-
	Rise time, Fall time		tvrf	-	-	10	ns	

Note1: Definition of parameters is as follows.

tcf = 1/tc, tcd = tch/tc = tch×tcd

Note2: Definition of parameters is as follows.

tc = 1CLK, th = 1H

Note3: Keep tvp + tvb and thp + thb within the table. If it is out of specification, display position will be shifted to right/left side or up/down.

4.8.10 Timing characteristics of QVGA- display for composite mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency		tcf	-	6.4	-	MHz	157.3 ns (typ.) Note1
	Duty		tcd	0.4	-	0.6	-	Note1
	Rise time, Fall time		tcrf	-	-	10	ns	-
DATA	CLK-DATA	Setup time	tds	10	-	-	ns	
		Hold time	tdh	10	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	
Hsync	Cycle		th	61.7	63.6	65.5	μs	31.4 kHz (typ.)
				404			CLK	Note2
	Display period		thd	320			CLK	
	Front-porch		thf	7			CLK	
	Pulse width		thp	-	38	-	CLK	
	Back-porch		thb	-	39	-	CLK	
	Total of pulse width and back-porch		thp + thb	77			CLK	Note2, Note3
	CLK- Hsync	Setup time	ths	10	-	-	ns	-
		Hold time	thh	10	-	-	ns	
	Rise time, Fall time		thrf	-	-	10	ns	
Vsync	Cycle		tv	15.8	16.7	17.5	ms	59.9 Hz (typ.)
				262			H	Note2
	Display period		tvd	234			H	
	Front-porch		tvf	1			H	
	Pulse width		tvp	2	-	20	H	
	Back-porch		tvb	1	-	19	H	
	Total of pulse width and back-porch		tvp + tvb	21			H	Note2, Note3
	Vsync-Hsync	Setup time	tvhs	10	-	-	ns	Note2
		Hold time	tvhh	1	-	-	CLK	-
	Rise time, Fall time		tvrf	-	-	10	ns	

Note1: Definition of parameters is as follows.

tcf = 1/tc, tcd = tch/tc = tch×tcd

Note2: Definition of parameters is as follows.

tc = 1CLK, th = 1H

Note3: Keep tvp + tvb and thp + thb within the table. If it is out of specification, display position will be shifted to right/left side or up/down.

4.9 OPTICS

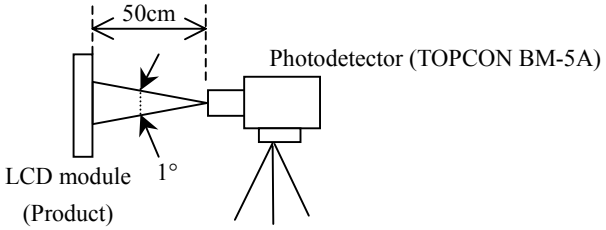
4.9.1 Optical characteristics

Parameter Note1		Condition	Symbol	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	70	85	-	-	Note2
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	200	250	-	cd/m^2	-
Luminance uniformity		-	LU	-	-	1.50	-	Note3
Color gamut		θR = 0°, θL = 0°, θU = 0°, θD = 0° at center, against NTSC color space	C	40	50	-	%	Note4
Response time		White to black	Ton	-	16	60	ms	Note5 Note6
		Black to white	Toff	-	-	100	ms	
Viewing angle	Right	θU = 0°, θD = 0°, CR = 10	θR	-	50	-	°	Note7
	Left	θU = 0°, θD = 0°, CR = 10	θL	-	50	-	°	
	Up	θR = 0°, θL = 0°, CR = 10	θU	-	25	-	°	
	Down	θR = 0°, θL = 0°, CR = 10	θD	-	25	-	°	

Note1: Measurement conditions are as follows.

Ta = 25°C, VCC = 9.5V, VDDB = 9.5V, DPSH = Low, DPSV = Low, PNS = High

Optical characteristics are measured at luminance saturation after 20minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note2: See "4.9.2 Definition of contrast ratio".

Note3: See "4.9.3 Definition of luminance uniformity".

Note4: These coordinates are found on CIE 1931 chromaticity diagram.

Note5: Product surface temperature: TopF = 25°C

Note6: See "4.9.4 Definition of response times".

Note7: See "4.9.5 Definition of viewing angles".

4.9.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

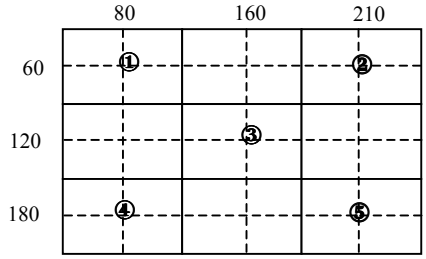
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.9.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

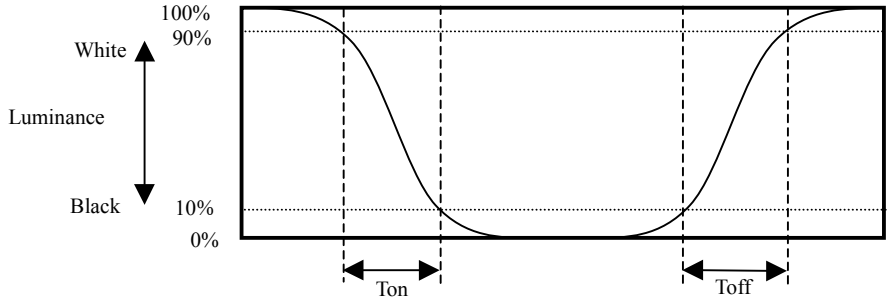
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

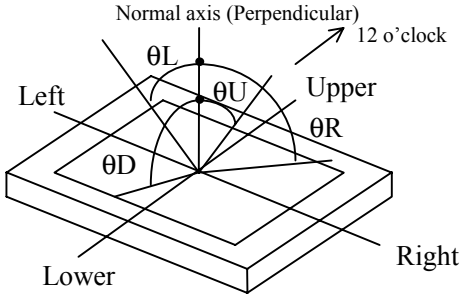


4.9.4 Definition of response times

Response time is measured, the luminance changes from "white" to "black", or "black" to "white" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 90% down to 10%. Also Toff is the time it takes the luminance change from 10% up to 90% (See the following diagram.).



4.9.5 Definition of viewing angles



5. RELIABILITY TESTS

5.1 Test items

Test item	Condition	Judgement
High temperature and humidity (Operation)	① 60 ± 2°C, RH = 90%, 192hours ② Display data is black. ③ Other conditions are by JASO-D001.	No display malfunctions Note2
High temperature (Operation)	① 85 ± 2°C, 192hours ② Display data is black. ③ Other conditions are by JASO-D001.	
High temperature (Non operation)	① 95 ± 2°C, 192hours ② Display data is black. ③ Other conditions are by JASO-D001.	
Low temperature (Operation)	① -30 ± 4°C, 192hours ② Display data is black. ③ Other conditions are by JASO-D001.	
Low temperature (Non operation)	① -40 ± 4°C, 192hours ② Display data is black. ③ Other conditions are by JASO-D001.	
Heat and humidity cycle (Operation) Note1	① 23 ± 2°C, RH = 65 ± 2%…4hours 55 ± 2°C, RH = 97 ± 2%…10hours -40 ± 4°C, RH = 5 ± 2%…2hours 85 ± 2°C, RH = 5 ± 2%…2hours ② 10cycles, 24hours/cycle (with temperature transition times) ③ Display data is black. ④ Other conditions are by JASO-D001.	
Heat cycle (Operation) Note1	① 75 ± 2°C…2hours -30 ± 4°C…2hours ② 35cycles, 8hours/cycle (with temperature transition times) ③ Display data is black. ④ Other conditions are by JASO-D001.	
Thermal shock (Non operation)	① 95 ± 2°C…2hours -40 ± 4°C…2hours ② 50cycles, 4hour/cycle ③ Temperature transition time is within 5 minutes. ④ Other conditions are by JASO-D001.	
ESD (Operation)	① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note3 ③ 10 times each places at 1 sec interval	
Dust (Operation)	① Sample dust: No. 15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Vibration (Non operation)	① 5 to 100Hz, 29.4m/s^2 ② 10 minutes/sweep ③ X, Y directions...2hours ④ Z direction...4hours ⑤ Other conditions are by JASO-D001.	No display malfunctions Note2 No physical damages
Mechanical shock (Non operation)	① 980m/ s^2, 11ms ② ±X, ±Y, ±Z direction ③ 3 times each directions ④ Other conditions are by JASO-D001.	

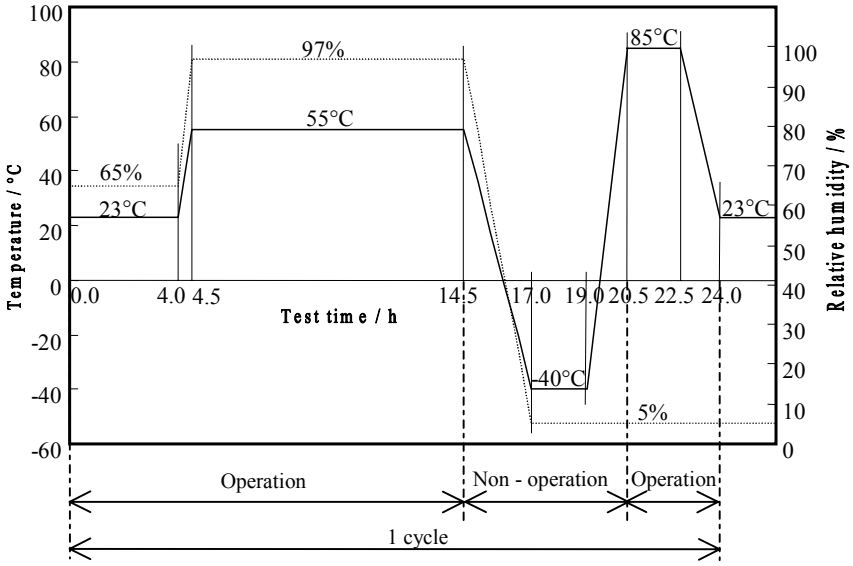
Note1: See "5.2 Test cycle pattern".

Note2: Display functions are checked under the same conditions as product inspection.

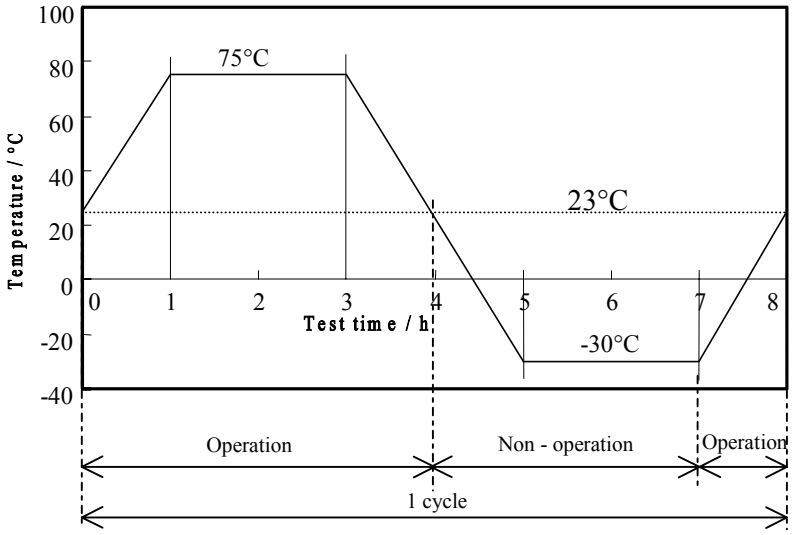
Note3: See "5.3 Discharge points".

5.2 Test cycle pattern

- Heat and humidity cycle

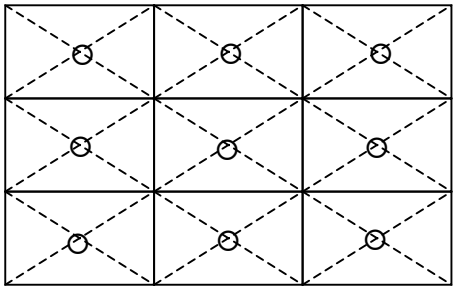


- Heat cycle



5.3 Discharge points

Discharge points are circle parts in the following figure.



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS", after understanding this contents!**

This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.

This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

Do not touch HIGH VOLTAGE PART of the inverter while turned on! Danger of an electrical shock.

∗ Pay attention to burn injury for the working backlight! It may be over 35°C from ambient temperature.

∗ Do not shock and press the LCD panel and the backlight! Danger of breaking, because they are made of glass. (Shock: To be not greater 980m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N)

6.3 ATTENTIONS

6.3.1 Handling of the product

① Take hold of both ends without touch the circuit board when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.

② Do not hook cables nor pull connection cables such as flexible cable and so on, for fear of damage.

③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.

④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.

⑤ The torque for mounting screws must never exceed 0.18N·m. Higher torque values might result in distortion of the bezel.

⑥ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC Corporation recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.

⑦ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.
② Do not operate in high magnetic field. Circuit boards may be broken down by it.
③ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

6.3.3 Characteristics

The following items are neither defects nor failures.

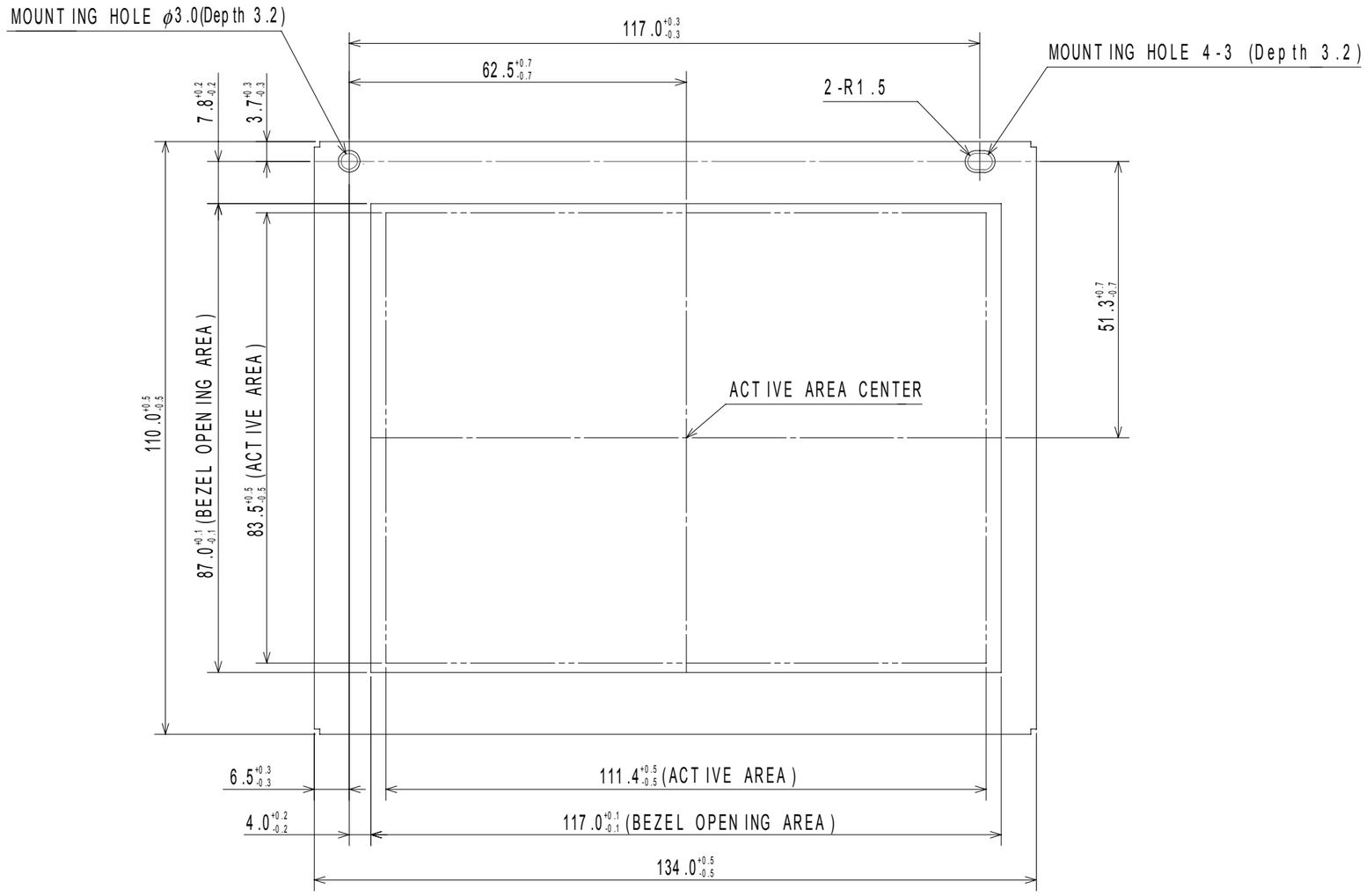
① Response time, luminance and color may be changed by ambient temperature.
② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed by viewing angle because of the use of condenser sheet in the backlight unit.
⑥ The luminance may be changed by voltage variation (voltage drop), even if power source applies recommended voltage to backlight inverter.
⑦ Optical characteristics may be changed by input signal timings.

6.3.4 Other

① All GND, GNDB, VCC and VDDB terminals should be used without a non-connected line.
② Do not disassemble a product or adjust volume without permission of NEC Corporation.
③ See "REPLACEMENT MANUAL FOR BACKLIGHT", if customer would like to replace backlight lamps.
④ Pay attention not to insert waste materials inside of products, if customer uses screwnails.

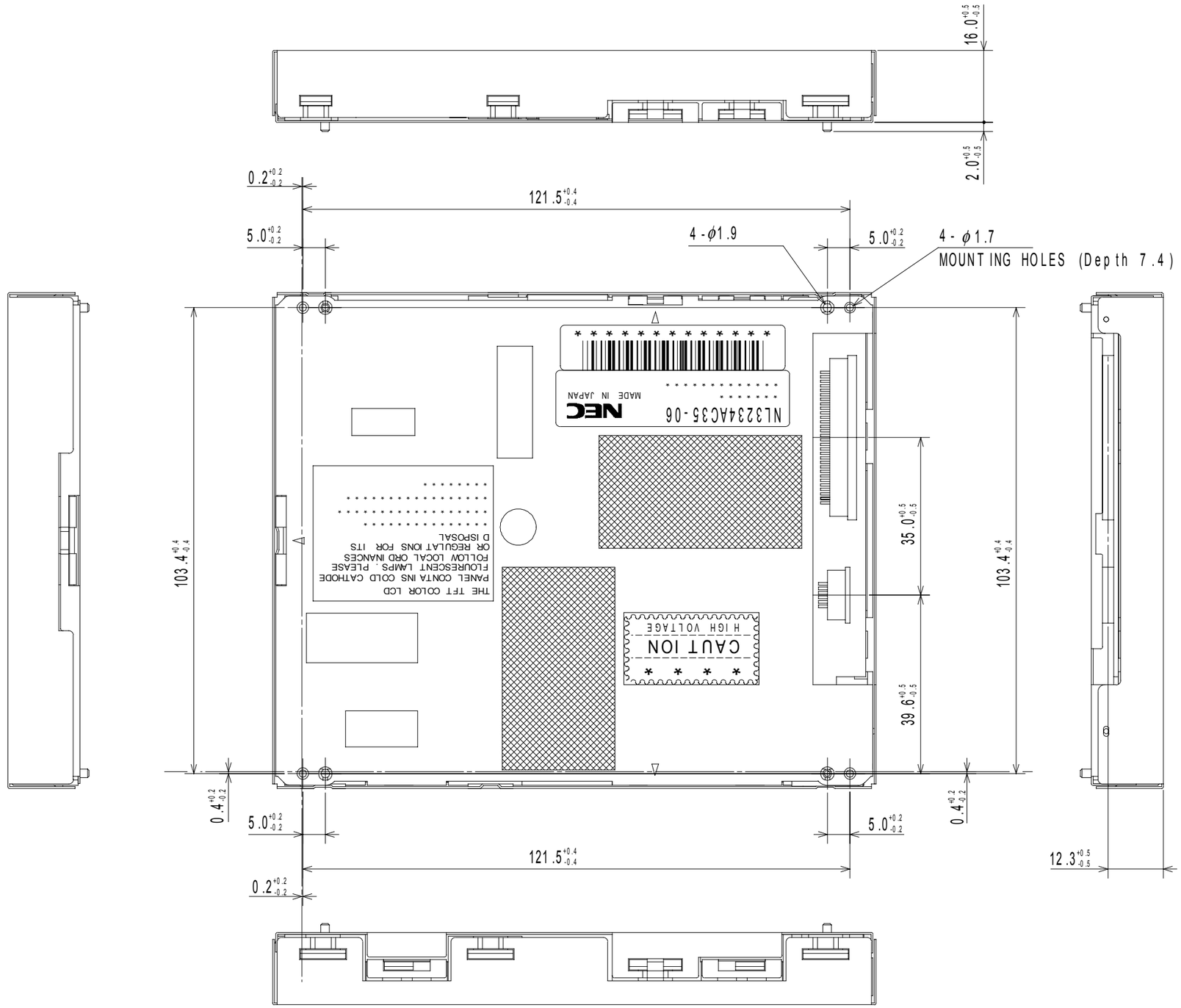
7. OUTLINE DRAWINGS

7.1 FRONT VIEW



Unit: mm

7.2 REAR VIEW



Unit: mm