Bus transceivers (3-State)

~~74F861*~~, ~~74F862*~~, 74F863, ~~74F864*~~

FEATURES

- Provide high performance bus interface buffering for wide data/address paths or buses carrying parity
- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- I_{IL} is 20µA vs. 1000µA for AM29861 series
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- Slim dual In-line (DIP) 300mil package
- Broadside pinout compatible with AMD AM29861–29864
- Outputs sink 64mA

DESCRIPTION

The 74F861 series bus transceivers provide high performance bus interface buffering for wide data/address paths of buses carrying parity. The 74F863/864 9-bit bus transceivers have NOR-ed transmit and receive output enables for maximum control flexibility.

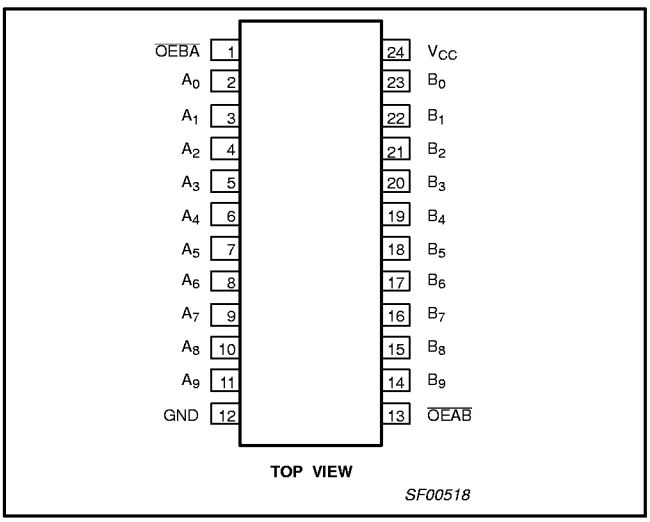
TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F861, 74F862	6.0ns	150mA
74F863, 74F864	6.0ns	115mA

ORDERING INFORMATION

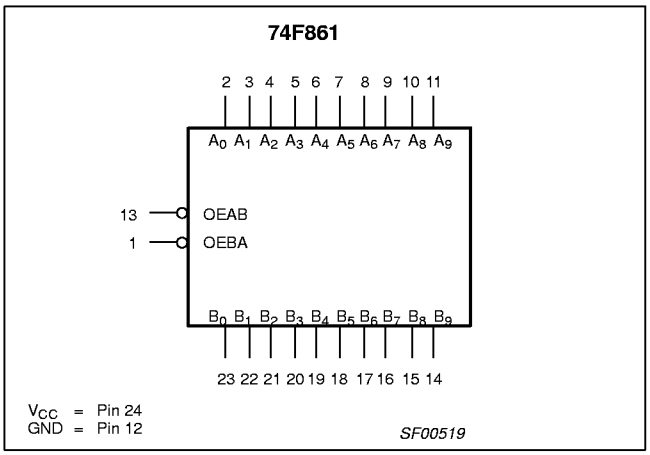
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C	PKG DWG #
24-pin Plastic Slim Dual In-line (300mil) Package	74F863N	SOT222-1
24-pin Plastic Small Outline Large[1]	74F863D	SOT137-1

NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications for a discussion of thermal considerations for surface mounted devices.

PIN CONFIGURATION



LOGIC SYMBOL



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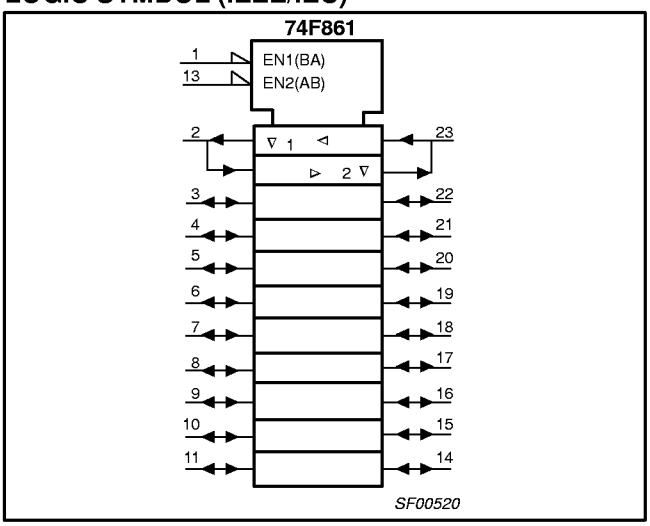

** Discontinued part. Please see the Discontinued Products List.*

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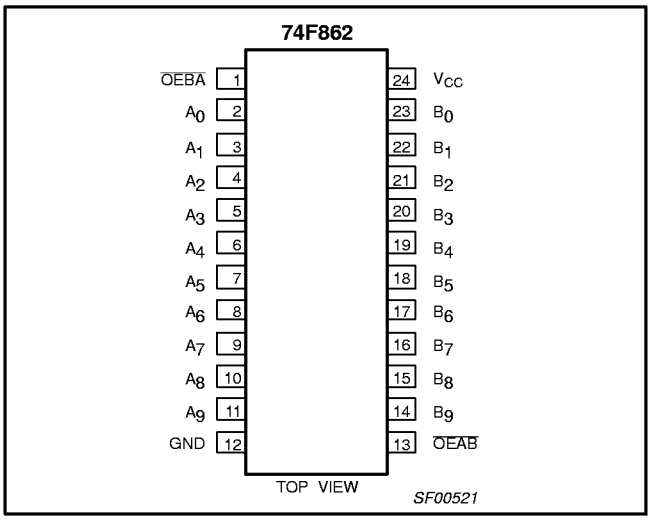

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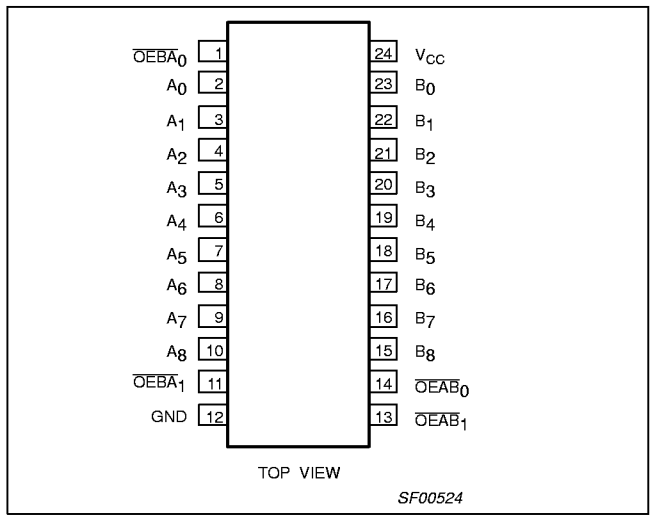

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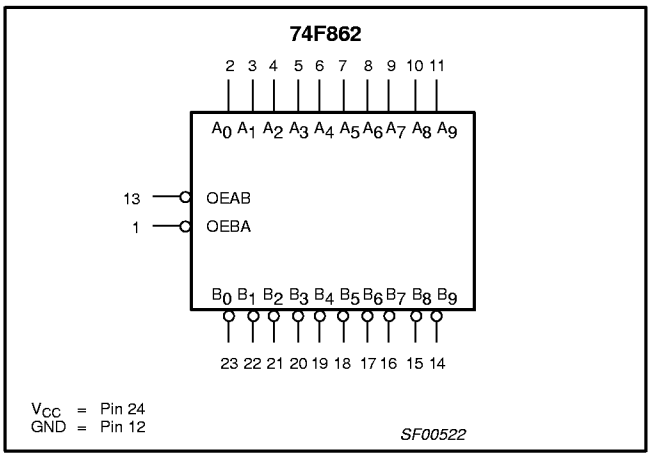

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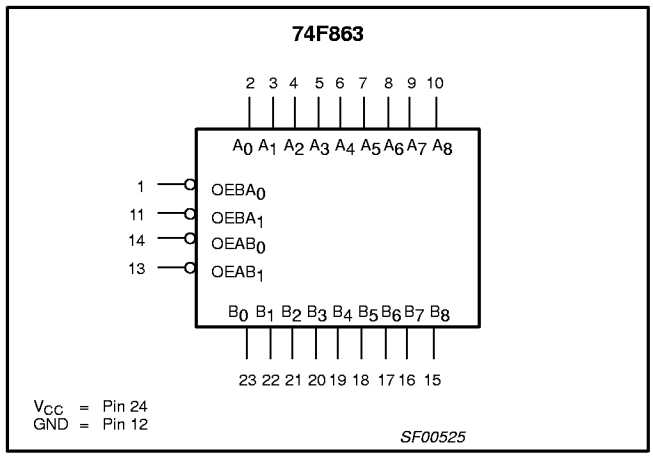

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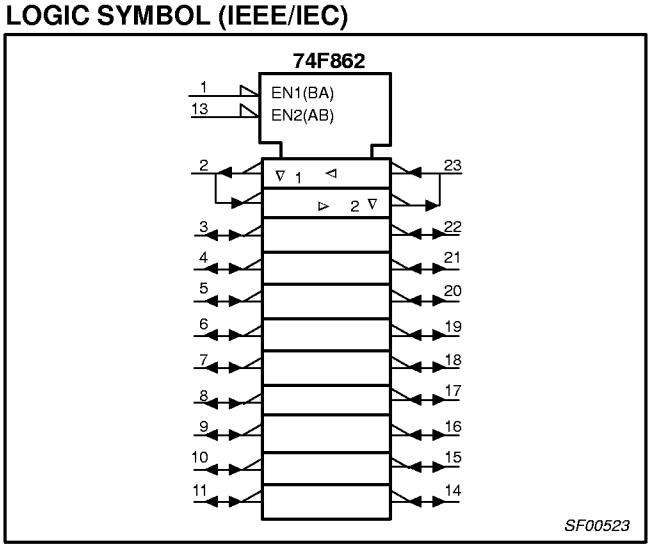

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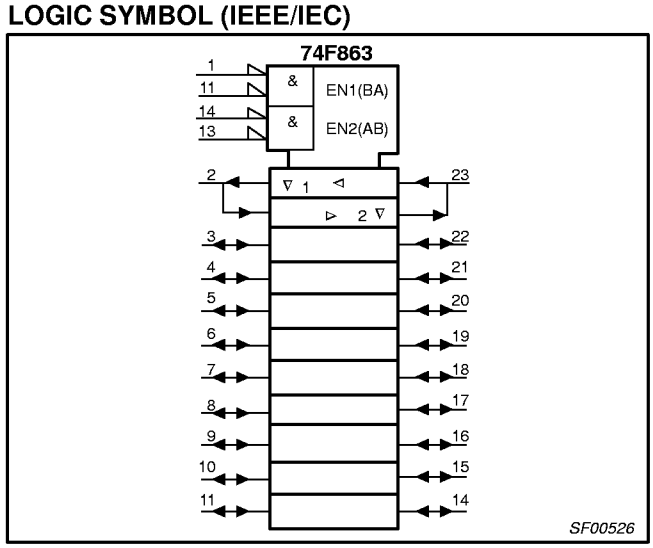
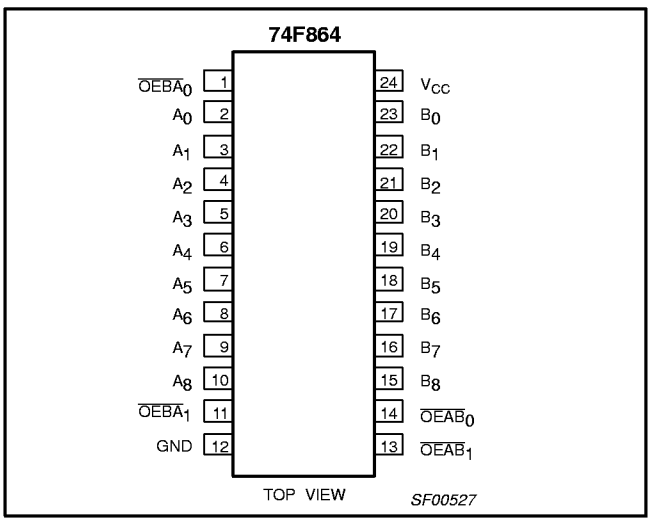


* *Discontinued part. Please see the Discontinued Products List.*

PIN CONFIGURATION



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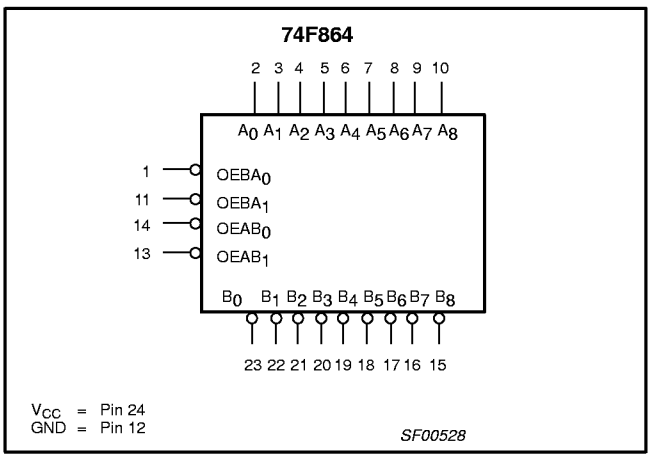

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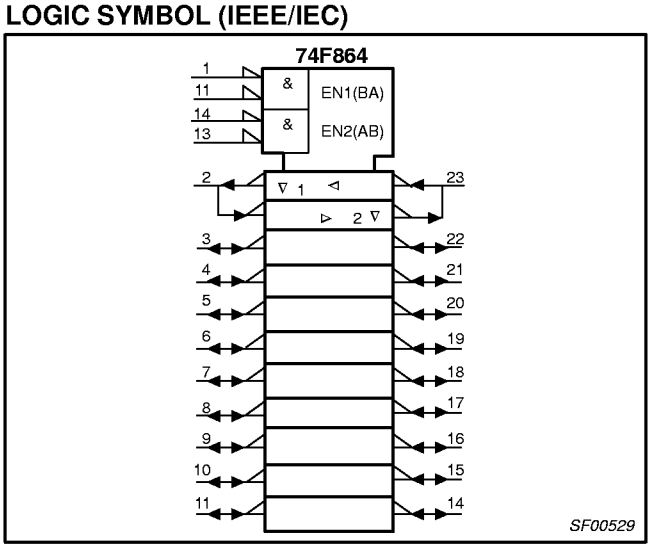
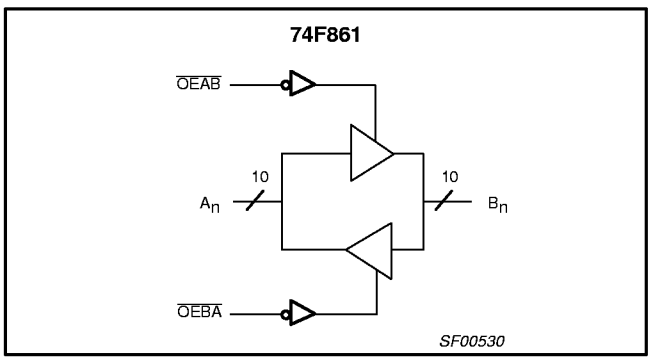
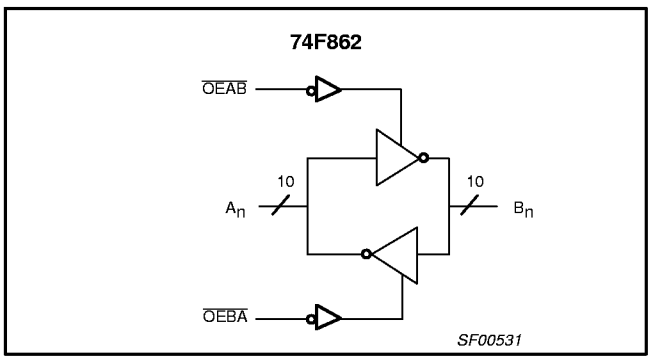
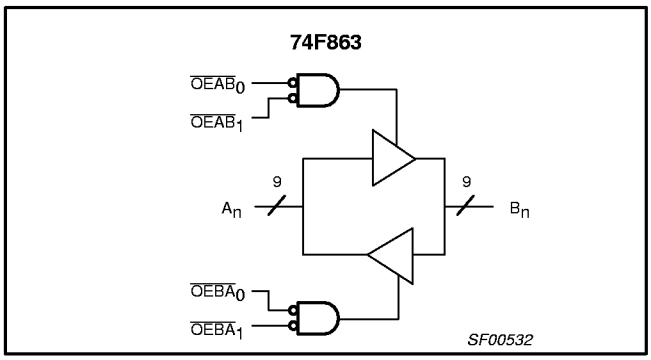
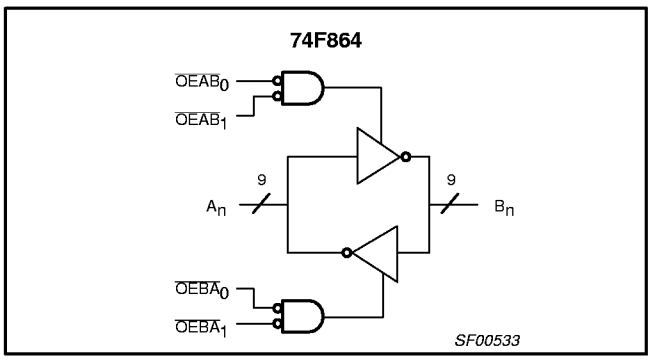


LOGIC DIAGRAM









* *Discontinued part. Please see the Discontinued Products List.*

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F861 74F862	$A_0 - A_9$	Data transmit inputs	3.5/0.117	70µA/70µA
	$B_0 - B_9$	Data receive inputs	3.5/0.117	70µA/70µA
	$\overline{OEBA}$	Transmit output enable input	1.0/0.033	20µA/20µA
	$\overline{OEAB}$	Receive output enable input	1.0/0.033	20µA/20µA
	$A_0 - A_9$	Data transmit outputs	1200/106.7	24mA/64mA
	$B_0 - B_9$	Data receive outputs	1200/106.7	24mA/64mA
74F863 74F864	$A_0 - A_9$	Data transmit inputs	3.5/0.117	70µA/70µA
	$B_0 - B_9$	Data receive inputs	3.5/0.117	70µA/70µA
	$\overline{OEBA}_n$	Transmit output enable input	1.0/0.033	20µA/20µA
	$\overline{OEAB}_n$	Receive output enable input	1.0/0.033	20µA/20µA
	$A_0 - A_9$	Data transmit outputs	1200/106.7	24mA/64mA
	$B_0 - B_9$	Data receive outputs	1200/106.7	24mA/64mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

FUNCTION TABLE FOR 74F861 AND 74F862

INPUTS		OPERATING MODES	
$\overline{OEAB}$	$\overline{OEBA}$	74F861	74F862
L	H	A data to B bus	A data to B bus
H	L	B bus to A data	B bus to A data
H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

FUNCTION TABLE FOR 74F863 AND 74F864

INPUTS				OPERATING MODES	
$\overline{OEAB}_0$	$\overline{OEAB}_1$	$\overline{OEBA}_0$	$\overline{OEBA}_1$	74F863	74F864
L L	L L	H X	X H	A data to B bus	A data to B bus
H X	X H	L L	L L	B bus to A data	B bus to A data
H	H	H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

* *Discontinued part. Please see the Discontinued Products List.*

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

* *Discontinued part. Please see the Discontinued Products List.*

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC}=MIN, V_{IL}=MAX, V_{IH}=MIN	I_{OH}=-15mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.4	3.3		V
				V_{CC}=MIN, V_{IL}=MAX, V_{IH}=MIN	I_{OH}=-24mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC}=MIN, V_{IL}=MAX, V_{IH}=MIN	I_{OL}=-48mA	±10%V_{CC}		0.38	0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$ $\overline{OEAB_n}$, $\overline{OEBA_n}$		V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_n, B_n		V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{IH} + I_{OZH}	Off-state output current High-level voltage applied		A_n, B_n	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL} + I_{OZL}	Off-state output current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	A_n, B_n Supply current total	74F861 74F863	I_{CCH}	V_{CC} = MAX				145	195	mA
			I_{CCL}					140	195	mA
			I_{CCZ}					165	220	mA
		74F862 74F864	I_{CCH}	V_{CC} = MAX				90	130	mA
			I_{CCL}					120	170	mA
			I_{CCZ}					130	160	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

** Discontinued part. Please see the Discontinued Products List.*

AC ELECTRICAL CHARACTERISTICS

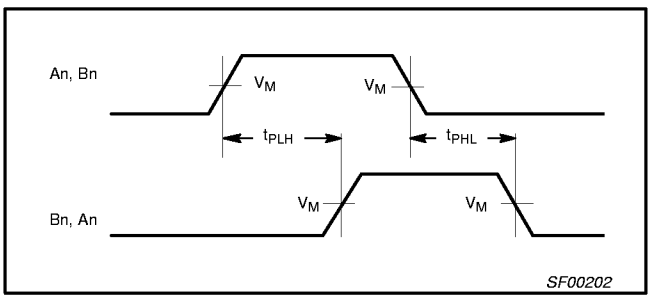
SYMBOL	PARAMETER	TEST CONDITION	74F861, 74F863					UNIT
			T_A = +25°C, V_{CC} = 5V C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n	Waveform 1	4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n or A_n	Waveform 1	4.0 2.5	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.0 4.0	8.0 6.0	11.5 10.0	5.0 4.0	13.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.0 4.0	8.0 6.0	11.0 10.0	5.0 4.0	13.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.5 2.5	5.5 5.0	9.0 8.5	3.0 2.0	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.5 2.5	5.5 4.5	8.5 8.5	3.0 2.0	9.5 9.5	ns

AC ELECTRICAL CHARACTERISTICS

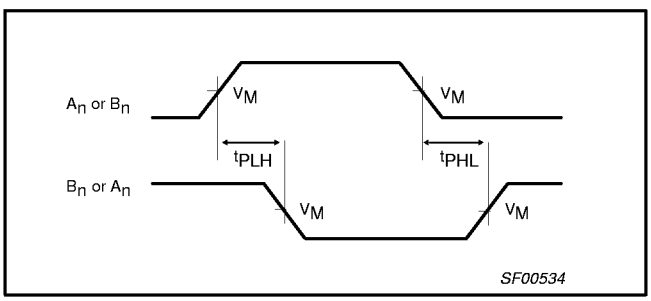
SYMBOL	PARAMETER	TEST CONDITION	74F862, 74F864					UNIT
			T_A = +25°C, V_{CC} = 5V C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n or A_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.5 1.5	10.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.5 6.0	8.5 7.5	12.0 12.0	5.5 5.0	13.5 14.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.5 6.0	8.5 7.5	12.0 12.0	5.5 5.0	13.5 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns

* *Discontinued part. Please see the Discontinued Products List.*

AC WAVEFORMS

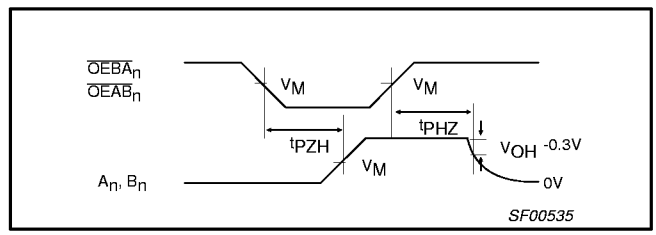


Waveform 1. Propagation Delay for Non-inverting Output

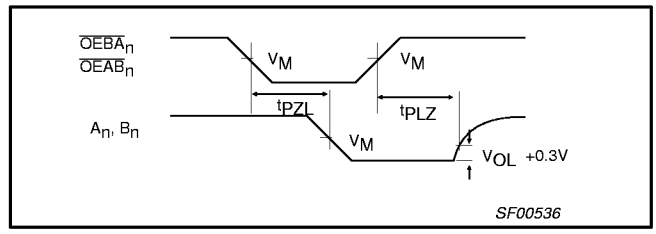


Waveform 2. Propagation Delay for Inverting Output

NOTE: For all waveforms, V_M = 1.5V.

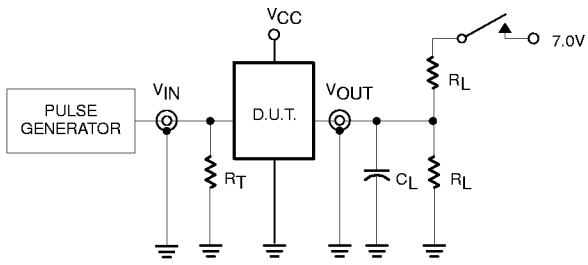


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

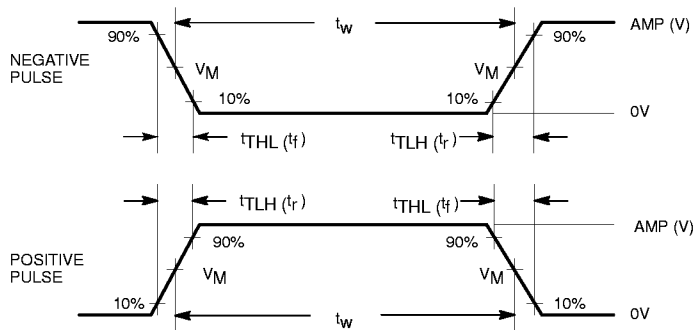
TEST CIRCUITS AND WAVEFORMS



Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



Input Pulse Definition

DEFINITIONS:

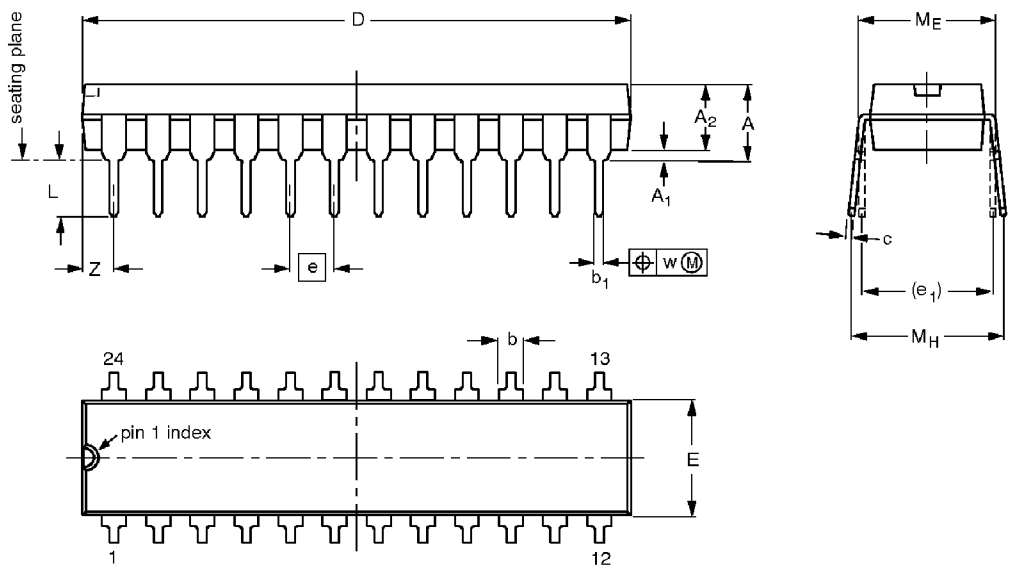
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

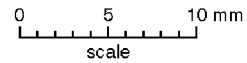
family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

* *Discontinued part. Please see the Discontinued Products List.*

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

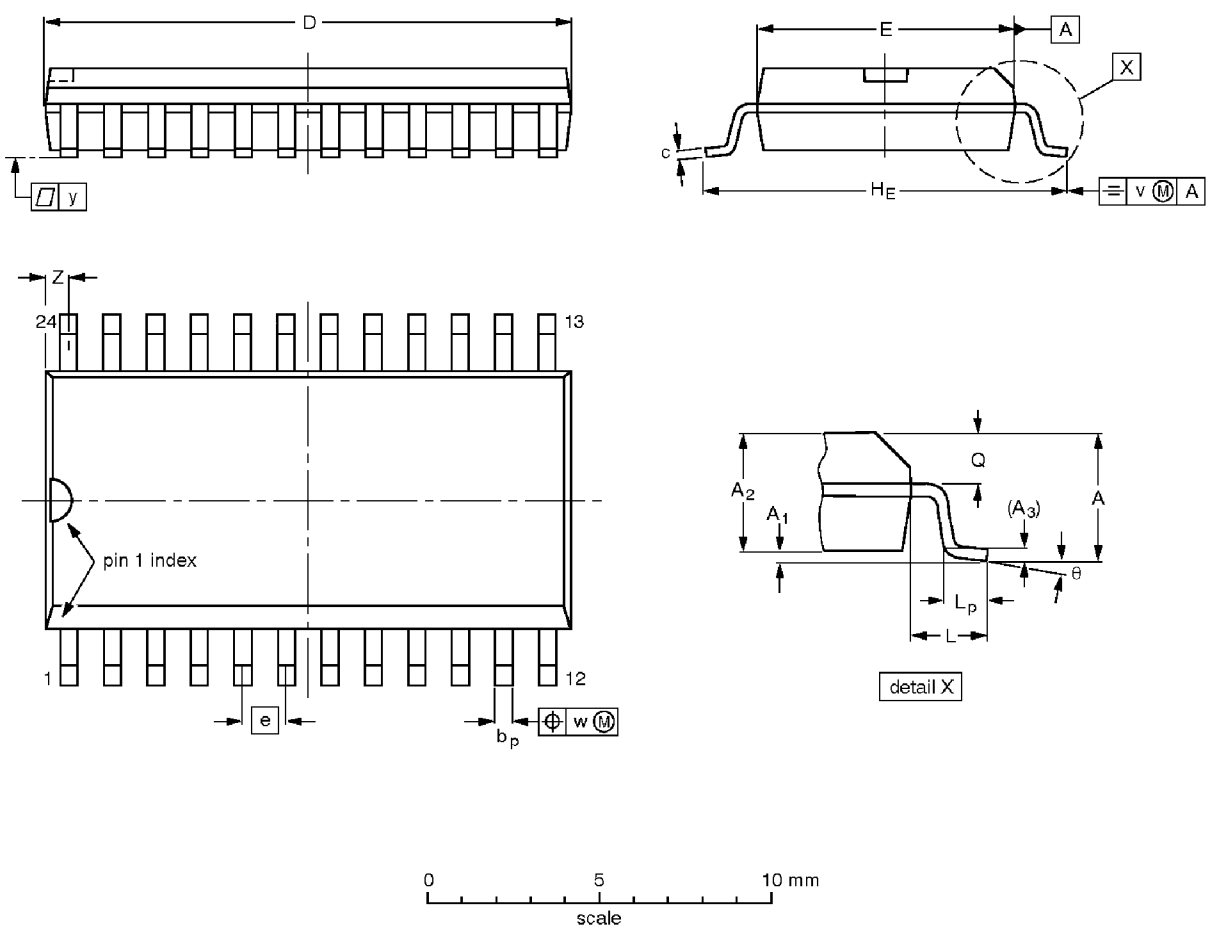
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

** Discontinued part. Please see the Discontinued Product List..*

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

* *Discontinued part. Please see the Discontinued Product List..*

Bus transceivers (3-State)

~~74F861~~*, ~~74F862~~*,
74F863, ~~74F864~~*

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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