Philips Semiconductors-Signetics

Document No.	853-0085
ECN No.	95748
Date of issue	February 4, 1989
Status	Product Specification
FAST Products	

FAST 74F653, 74F654 Transceivers/Registers

'F653 Octal Transceiver/Register, Inverting (3-state +Open Collector)
'F654 Octal Transceiver/Register, Non-Inverting (3-state +Open Collector)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F653	90MHz	140mA
74F654	90MHz	140mA

FEATURES

- **High impedance NPN base inputs for redued loading (70µA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-state outputs (B_0-B_7) or Open-Collector outputs (A_0-A_7)**

DESCRIPTION

The 74F653 and 74F654 Transceivers/Registers consist of bus transceiver circuits with 3-state (B_0-B_7) or open collector (A_0-A_7)outputs , D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

ORDERING INFORMATION

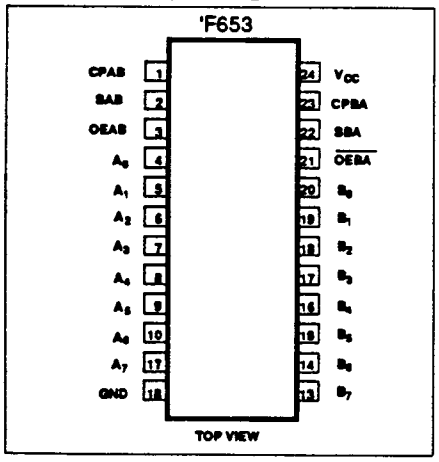
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Cerdip (300mil)	N74F653F, N74F654F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

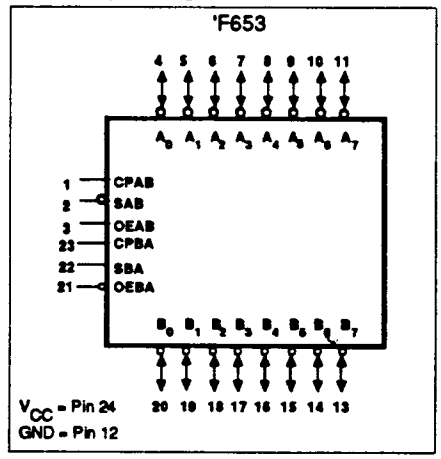
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	1.0/0.033	20µA/20µA
B_0 - B_7	B inputs	3.5/0.116	70µA/70µA
CPAB	A-to-B clock input	1.0/0.033	20µA/20µA
CPBA	B-to-A clock input	1.0/0.033	20µA/20µA
SAB	A-to-B select input	1.0/0.033	20µA/20µA
SBA	B-to-A select input	1.0/0.033	20µA/20µA
OEAB	A-to-B output enable input	1.0/0.033	20µA/20µA
$\overline{OEBA}$	B-to-A output enable input	1.0/0.033	20µA/20µA
A_0 - A_7	A outputs	OC /106.7	OC /64mA
B_0 - B_7	B outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

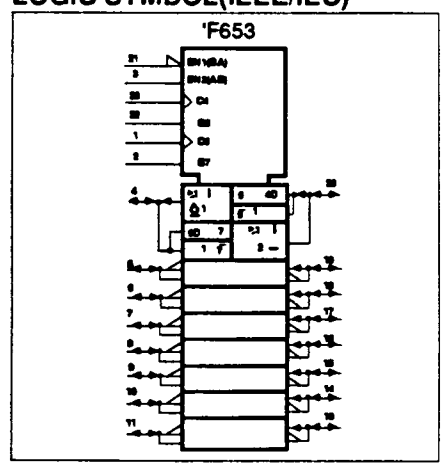
PIN CONFIGURATION



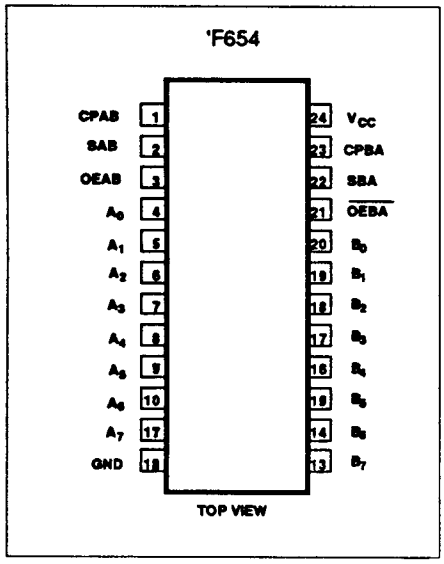
LOGIC SYMBOL



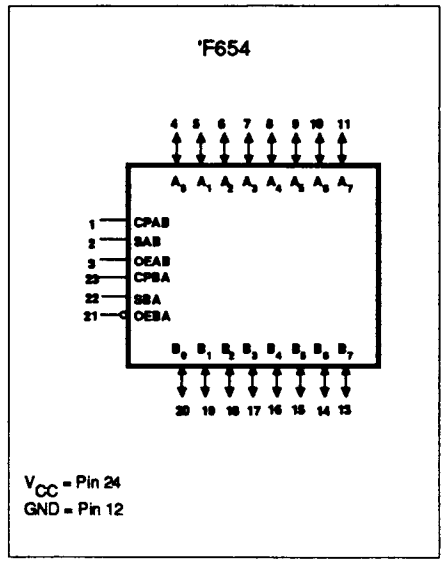
LOGIC SYMBOL(IEEE/IEC)



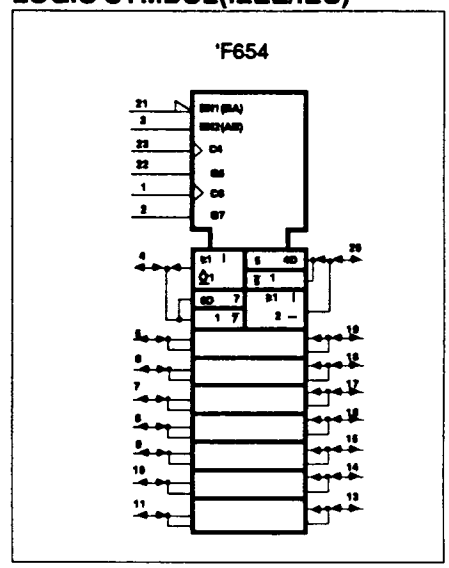
PIN CONFIGURATION



LOGIC SYMBOL

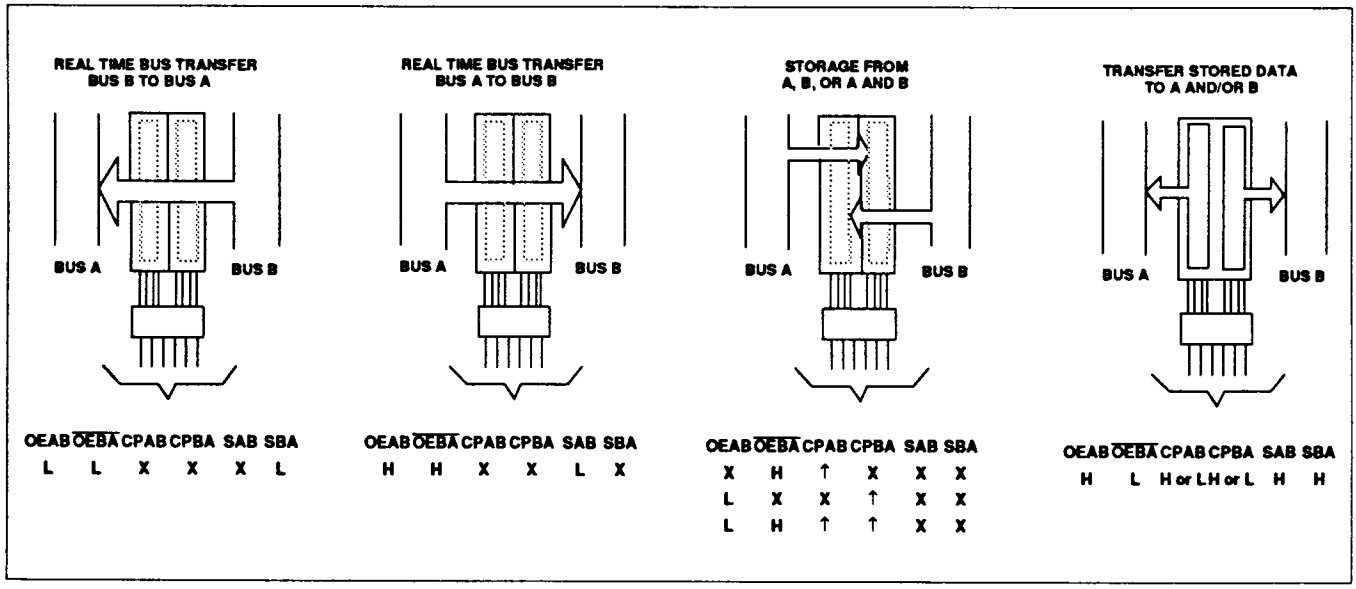


LOGIC SYMBOL(IEEE/IEC)



The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F653 and 'F654.The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.

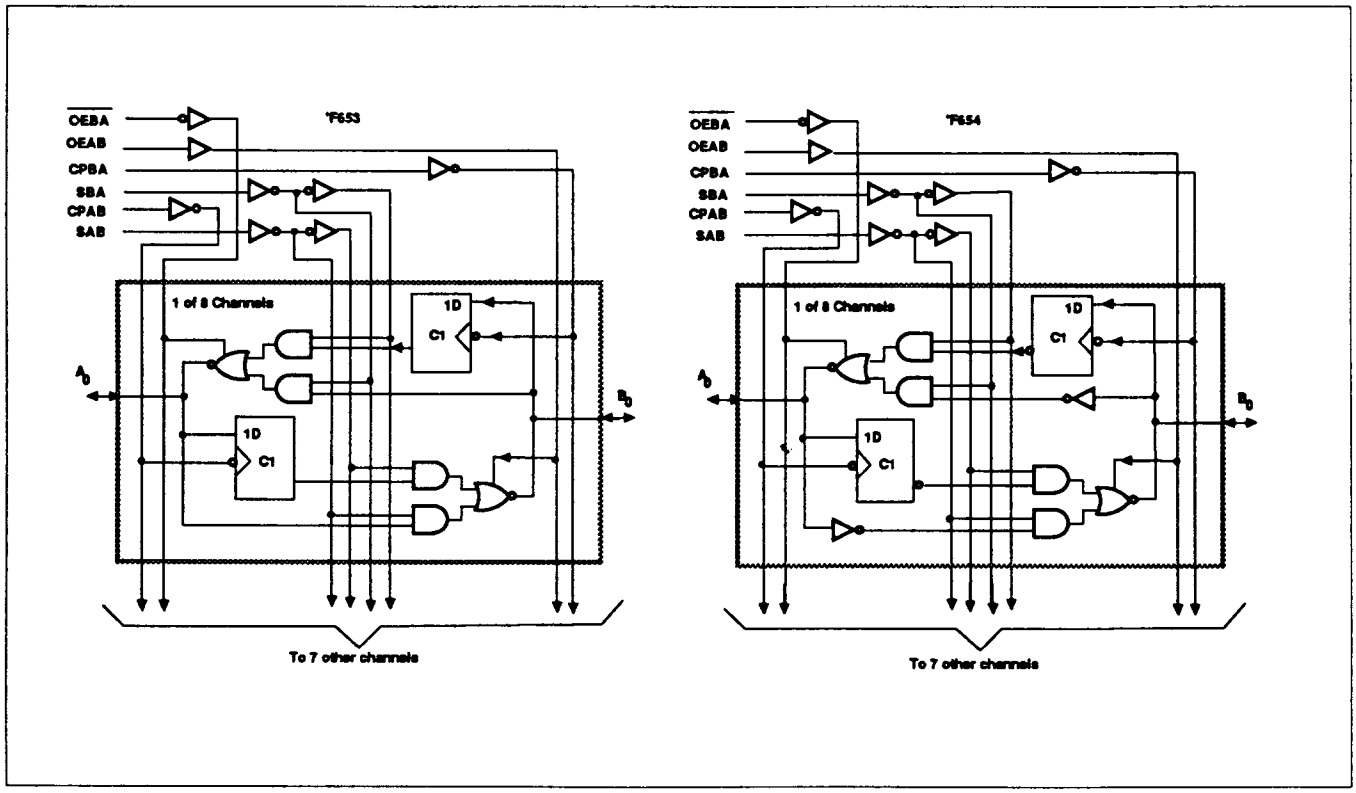


FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_n	B_n	'F653	'F654
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data	Isolation Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, Hold B	Store A, Hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time $\overline{A}$ data to B bus Stored $\overline{A}$ data to B bus	Real time A data to B bus Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus Stored $\overline{B}$ data to A bus	Stored A data to B bus Stored B data to A bus

H= High voltage level
L= Low voltage level
*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ =Low-to-High clock transition
X=Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage	A_0 - A_7			4.5	V
I_{OH}	High-level output current				-3	mA
		B_0 - B_7			-15	mA
I_{OL}	Low-level output current				64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA SAB, SBA A_0-A_7	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
$I_{IH}+I_{OZH}$	Off-state current High-level voltage applied	B_0-B_7	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]	B_0-B_7	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				110 140[4]	160 185[4]	mA
		I_{CCL}					140 160[4]	210 240[4]	mA
		I_{CCZ}					130	175	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. When using worst case conditions thermal mounting is required.

AC ELECTRICAL CHARACTERISTICS

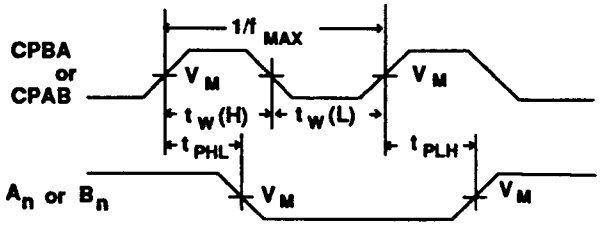
SYMBOL	PARAMETER		TEST CONDITION	74F653, 74F654					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	A_0-A_7	Waveform 1	55	70		45		MHz
		B_0-B_7		100	115		85		
t_{PLH} t_{PHL}	Propagation delay CPBA to A_n		Waveform 1	6.0 6.0	14.5 8.0	19.0 11.0	5.5 5.5	21.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to B_n		Waveform 1	5.5 5.5	7.5 8.0	10.5 10.5	5.0 5.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 3, 4	4.5 4.5	14.0 7.0	18.5 10.0	4.0 4.0	20.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n		Waveform 3, 4	4.0 4.0	6.0 6.5	9.5 9.5	3.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n		Waveform 3, 4	5.0 5.0	15.0 7.5	18.5 10.5	4.5 4.5	21.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB to B_n		Waveform 3, 4	5.0 5.0	7.0 7.0	10.0 10.0	4.5 4.5	12.0 10.5	ns
t_{PLH} t_{PHL}	Output Enable and Disable time $\overline{OEBA}$ to A_n		Waveform 2	6.5 6.5	16.0 10.0	20.0 12.5	6.0 6.0	23.0 14.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB to B_n		Waveform 8 Waveform 9	4.5 6.0	6.5 8.0	9.5 11.0	4.0 5.5	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB to B_n		Waveform 8 Waveform 9	6.5 6.0	9.5 9.0	13.0 12.0	6.0 5.5	14.5 14.5	ns

AC SETUP REQUIREMENTS

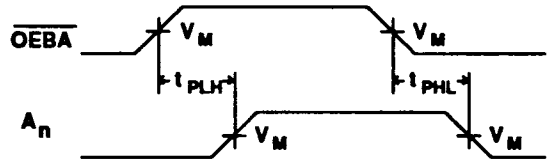
SYMBOL	PARAMETER	TEST CONDITION	74F653, 74F654					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 5	4.5 4.5			5.5 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 5	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low [1] $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 6, 7	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 6, 7	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	W aveform 1	4.5 6.5			4.5 6.5		ns

Note : 1. Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

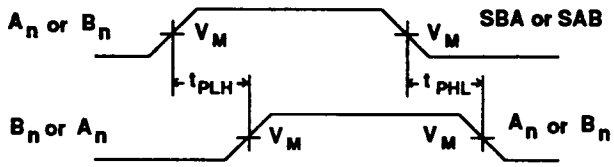
AC WAVEFORMS



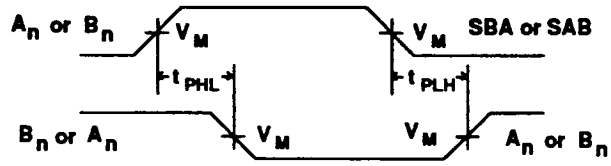
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



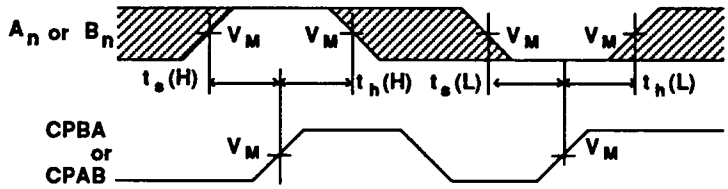
Waveform 2. Enable and Disable Times for Open Collector Outputs



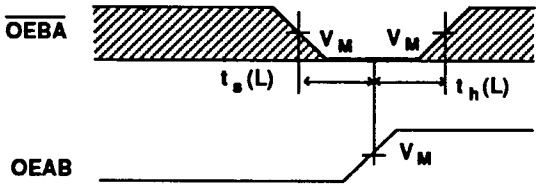
Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



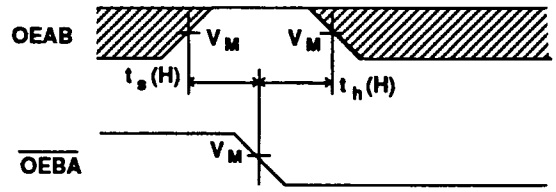
Waveform 4. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



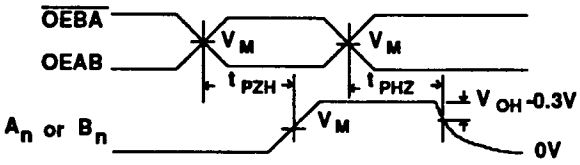
Waveform 5. Data Setup And Hold Times



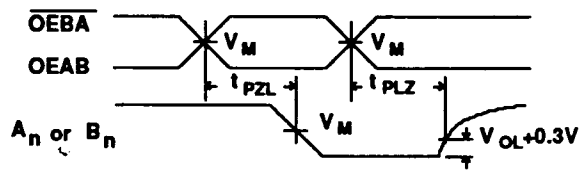
Waveform 6. $\overline{OEBA}$ to OEAB Setup And Hold Times



Waveform 7. OEAB to $\overline{OEBA}$ Setup And Hold Times



Waveform 8. 3-State Output Enable Time To High Level And Output Disable Time From High Level

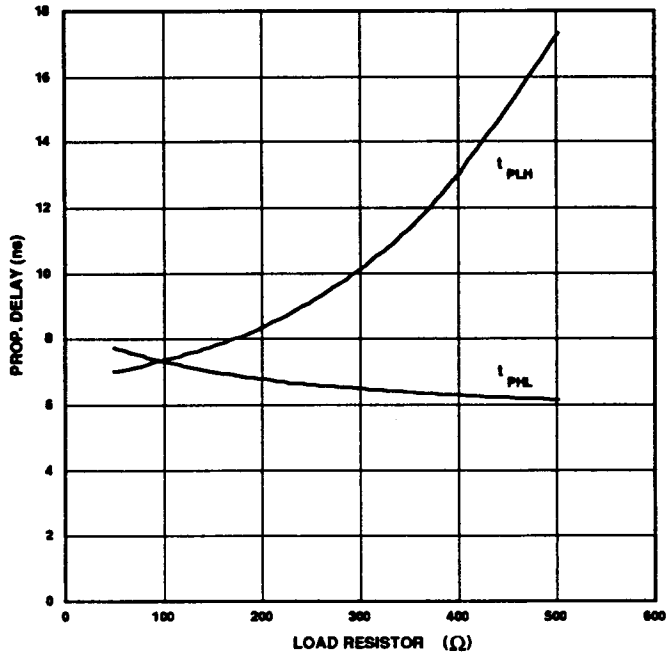


Waveform 9. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

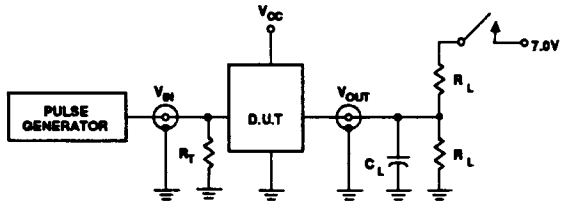
The shaded areas indicate when the input is permitted to change for predictable output performance.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

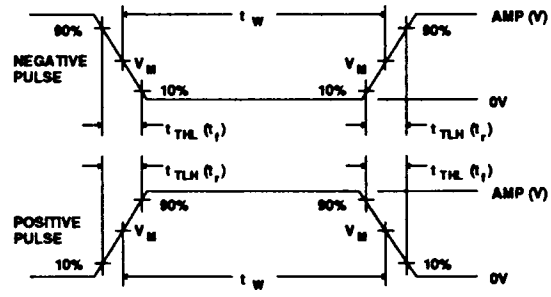


NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State and Open Collector Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns