



Ordering Information

MFT62340-JO	MPO/MTP Connector
MFT62340-JOS	With EMI shield
MFT62340-JX	MPX Connector

Applications

- High-speed interconnects
- Switches, Routers, Transport equipment
- Interconnects within and between equipment
- Rack-to-rack
- Shelf-to-shelf
- Board-to-board
- Board-to-optical backplane

Features

- Data rate 155Mbps to 2.5Gbps per channel
- 12 parallel channels, total 30Gbps capacity
- Differential CML (Current-Mode Logic) interface
- Link length up to 300m (with 500MHz·km fiber)
- Channel BER 10^{-12} when used with MFR62340
- Designed for multimode fiber ribbon
- MPO/MTP or MPX connector options
- Surface-mount package
- Pick-and-placeable, reflow soldering
- Relaxed Class 1 IEC 60825-1 Amd. 2 compliant
- Matches the MFR62340 Receiver
- EMI shield available

Description

The MFT62340 and MFR62340 is a very high speed transmitter and receiver pair for parallel fiber applications. This pair, together with a multimode parallel fiber ribbon cable, constitute a complete parallel fiber link. The link provides high-speed interconnects for use within and between large capacity switches, routers and data transport equipment. The transmitter and receiver have a differential CML interface and support MPO/MTP and MPX fiber connectors. An EMI shield is available for the MPO/MTP connector for use in front panel applications.

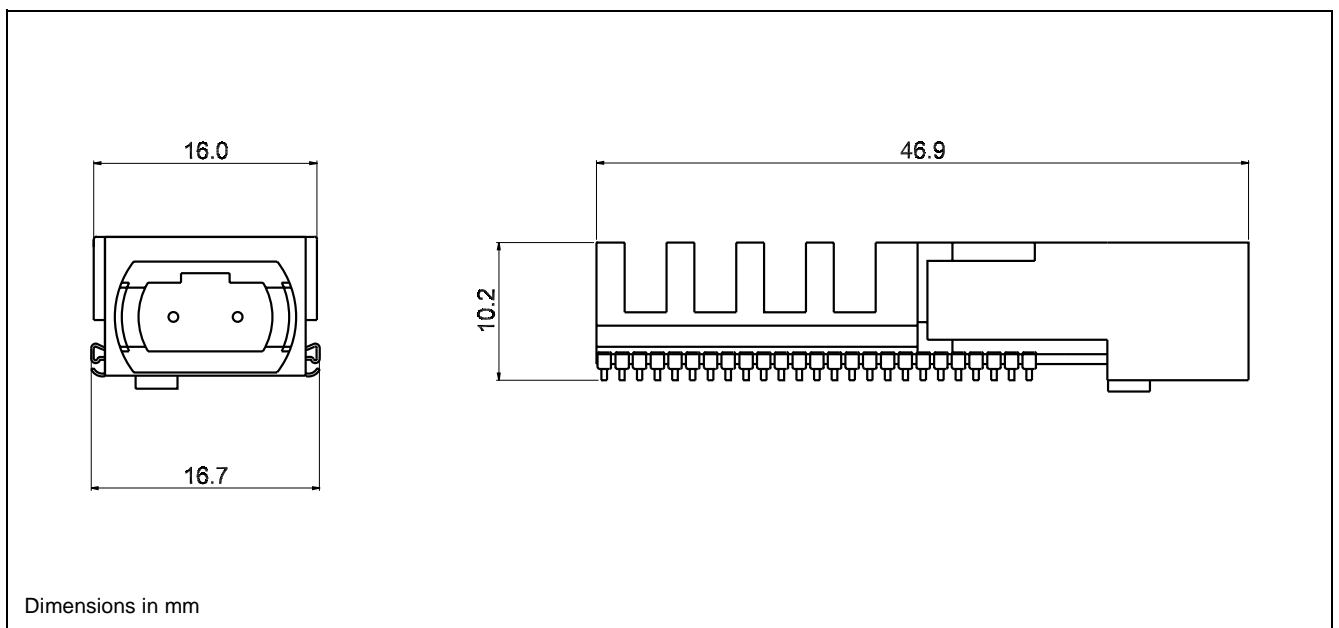


Figure 1 - MFT62340-JO: MPO/MTP Connector Option

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Unit
1	Supply voltage	V_{CC}	-0.3	3.6	V
2	Voltage on any pin	V_{PIN}	-0.3	$V_{CC}+0.3$	V
3	Operating and storage moisture	M_{OS}	20	85	%
4	Storage temperature	T_{STG}	-20	100	°C
5	ESD resistance all I/O except CML**	V_E	-2	2	kV
6	ESD resistance CML I/O**	V_{EC}	-500	500	V

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

** Human body model.

Recommended Operating Conditions*

	Parameter	Symbol	Min	Max	Unit
1	Case temperature	T_{CASE}	0	80	°C
2	Supply voltage	V_{CC}	3.3-5%	3.3+5%	V
3	CML differential input voltage (Fig. 2,3)	V_{ICML}	200	800	mV
4	Data rate per channel	f_D	0.155	2.5	Gbps
5	CML differential input rise/fall time (20-80%, Fig. 3)	t_{RC}, t_{FC}		160	ps
6	CMOS input voltage low	V_{LCMOS}	0	30% V_{CC}	V
7	CMOS input voltage high	V_{HCMOS}	70% V_{CC}	V_{CC}	V
8	Power supply noise (1MHz to 2GHz)	V_{NPS}		100	mV _{p-p}

* Maximum run length: 72 consecutive 1's or 0's; DC balance to be maintained within 144 bits. Fiber: 50/125 μ m or 62.5/125 μ m.

Characteristics*

	Parameter	Symbol	Min	Typ	Max	Unit
1	Power consumption (2.5 Gbps, Fig. 4)	P_D		1.8	2.4	W
2	Power supply current	I_{CC}		580		mA
3	CML differential input impedance (Fig. 2)	Z_{IN}	80	100	120	Ω
4	Optical rise/fall time (20-80%)	t_{RO}, t_{FO}			130	ps
5	Average fiber output power per channel	P_F	-7		-3	dBm
6	Deterministic jitter	DJ			50	ps _{p-p}
7	Random jitter (ER = 6dB)	RJ			5.2	ps _{rms}
8	Optical wavelength	λ	830	840	860	nm
9	Spectral width	$\Delta\lambda$			0.85	nm
10	Extinction ratio	ER	6			dB
11	NMOS output voltage low ($I_{sink} = 3mA$)	V_{LNMOS}			0.4	V
12	NMOS output voltage high	V_{HNMOS}	2.4			V
13	Channel skew	t_{SK}			175	ps
14	Relative intensity noise	RIN			-118	dB/Hz

* Operating conditions are as per Recommended Operating Conditions. Test pattern PRBS 2³¹-1 at 2.5Gbps and 50% duty cycle unless otherwise specified.

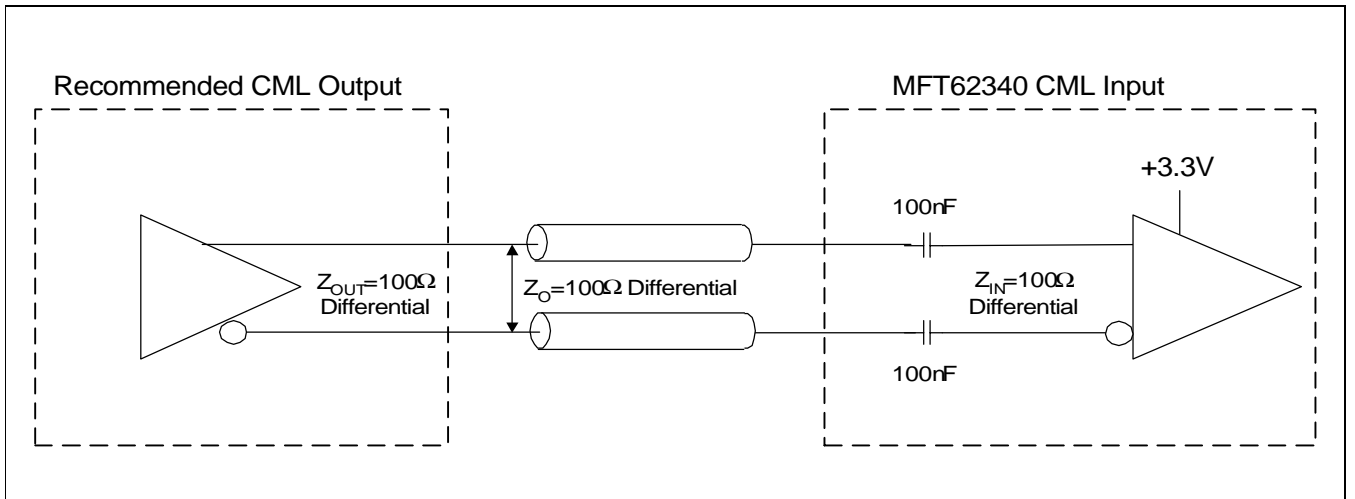


Figure 2 - Differential CML Interface

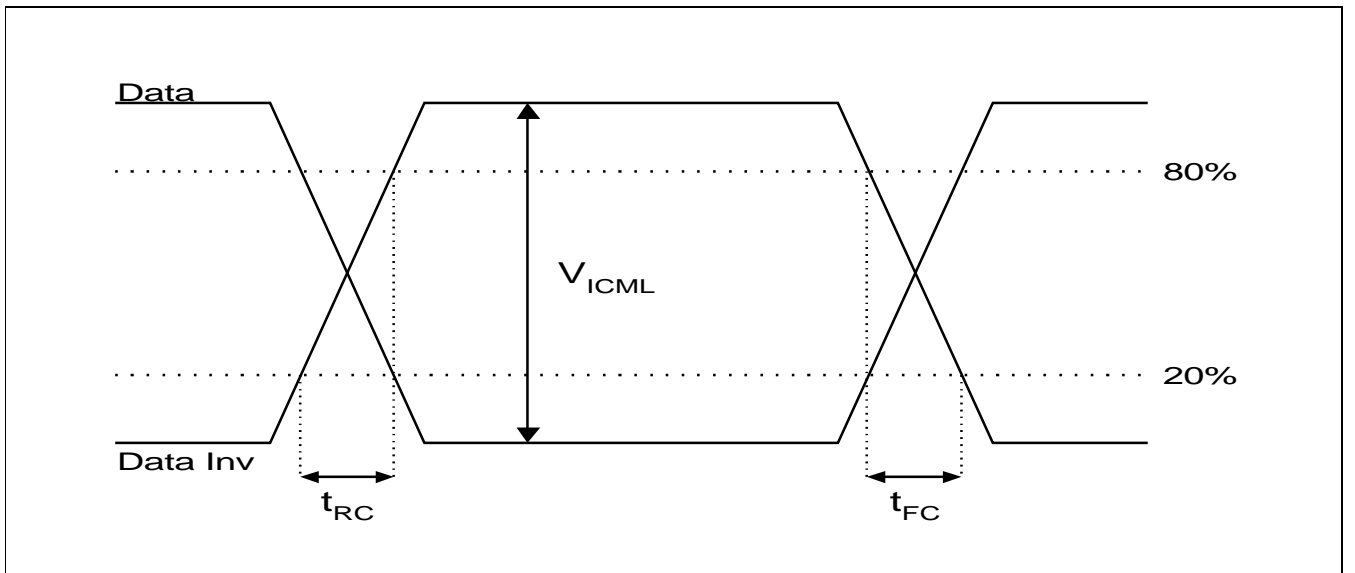


Figure 3 - Differential CML Timing Diagram

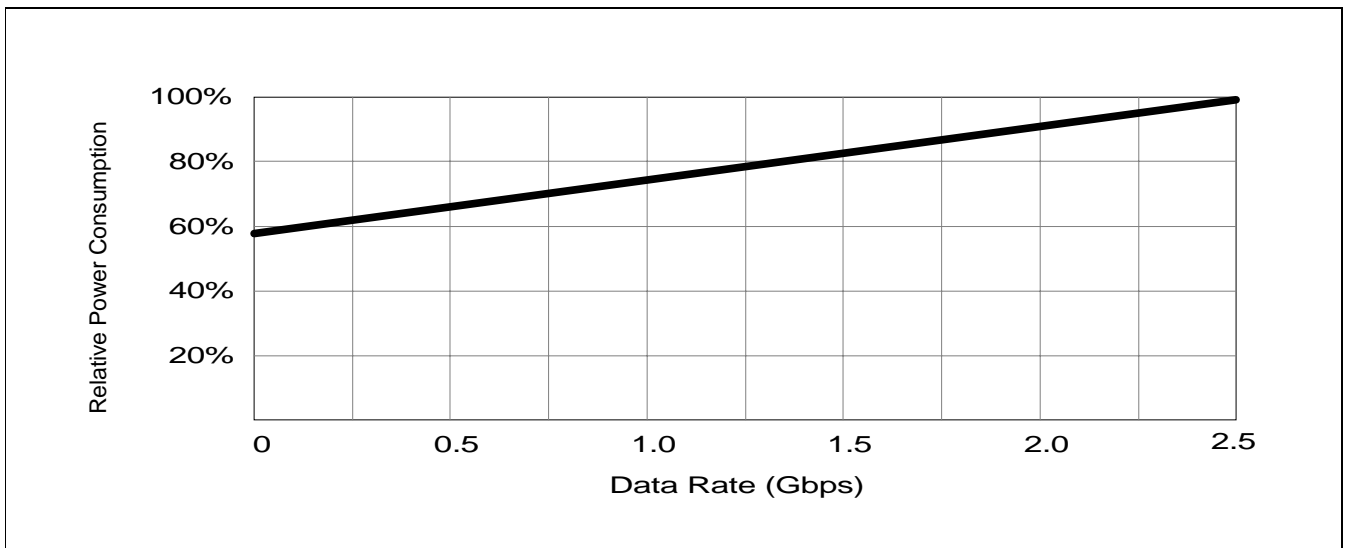


Figure 4 - Relative Power Consumption vs. Data Rate

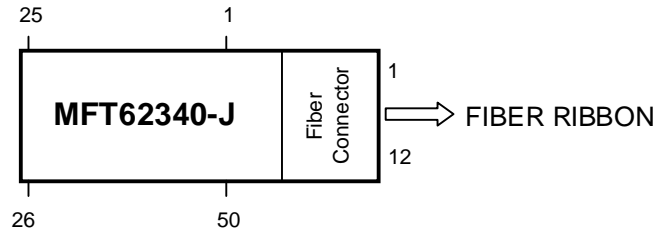


Figure 5 - Pin Assignment (Top View)

Pin Description

No	Name	Logic	Description
1	Gnd		Ground
2	V _{CC}		Positive power supply
3	V _{CC}		Positive power supply
4	V _{EN1-4}	CMOS	VCSELs enable ch. 1-4 ¹
5	V _{EN5-8}	CMOS	VCSELs enable ch. 5-8 ¹
6	V _{EN9-12}	CMOS	VCSELs enable ch. 9-12 ¹
7	Gnd		Ground
8	DI1C	CML	Data input No 1, inv.
9	DI1	CML	Data input No 1.
10	Gnd		Ground
11	DI2C	CML	Data input No 2, inv.
12	DI2	CML	Data input No 2.
13	Gnd		Ground
14	DI3C	CML	Data input No 3, inv.
15	DI3	CML	Data input No 3.
16	Gnd		Ground
17	DI4C	CML	Data input No 4, inv.
18	DI4	CML	Data input No 4.
19	Gnd		Ground
20	DI5C	CML	Data input No 5, inv.
21	DI5	CML	Data input No 5.
22	Gnd		Ground
23	DI6C	CML	Data input No 6, inv.
24	DI6	CML	Data input No 6.
25	Gnd		Ground
26	Gnd		Ground
27	DI7C	CML	Data input No 7, inv.
28	DI7	CML	Data input No 7.
29	Gnd		Ground
30	DI8C	CML	Data input No 8, inv.
31	DI8	CML	Data input No 8.
32	Gnd		Ground
33	DI9C	CML	Data input No 9, inv.
34	DI9	CML	Data input No 9.
35	Gnd		Ground
36	DI10C	CML	Data input No 10, inv.
37	DI10	CML	Data input No 10.
38	Gnd		Ground
39	DI11C	CML	Data input No 11, inv.
40	DI11	CML	Data input No 11.
41	Gnd		Ground
42	DI12C	CML	Data input No 12, inv.
43	DI12	CML	Data input No 12.
44	Gnd		Ground
45			Not Connected
46			Not Connected
47	NFLT	NMOS	Fault detection ²
48	V _{CC}		Positive power supply
49	V _{CC}		Positive power supply
50	Gnd		Ground

¹High = Lasers active. Internal pull-down resistor 50kΩ.
²Low = Driver not ready. Open drain with internal pull-up resistor 10kΩ.

Mechanical Drawings

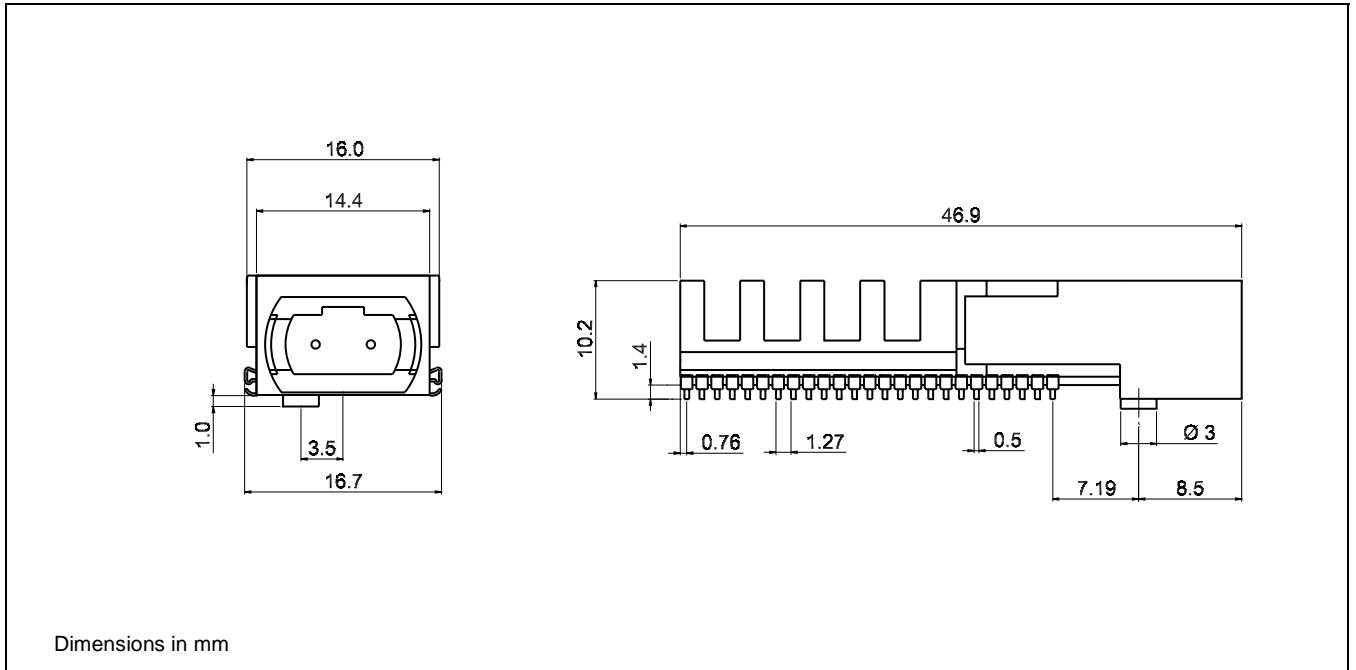


Figure 6 - MFT62340-JO: MPO/MTP Connector Option

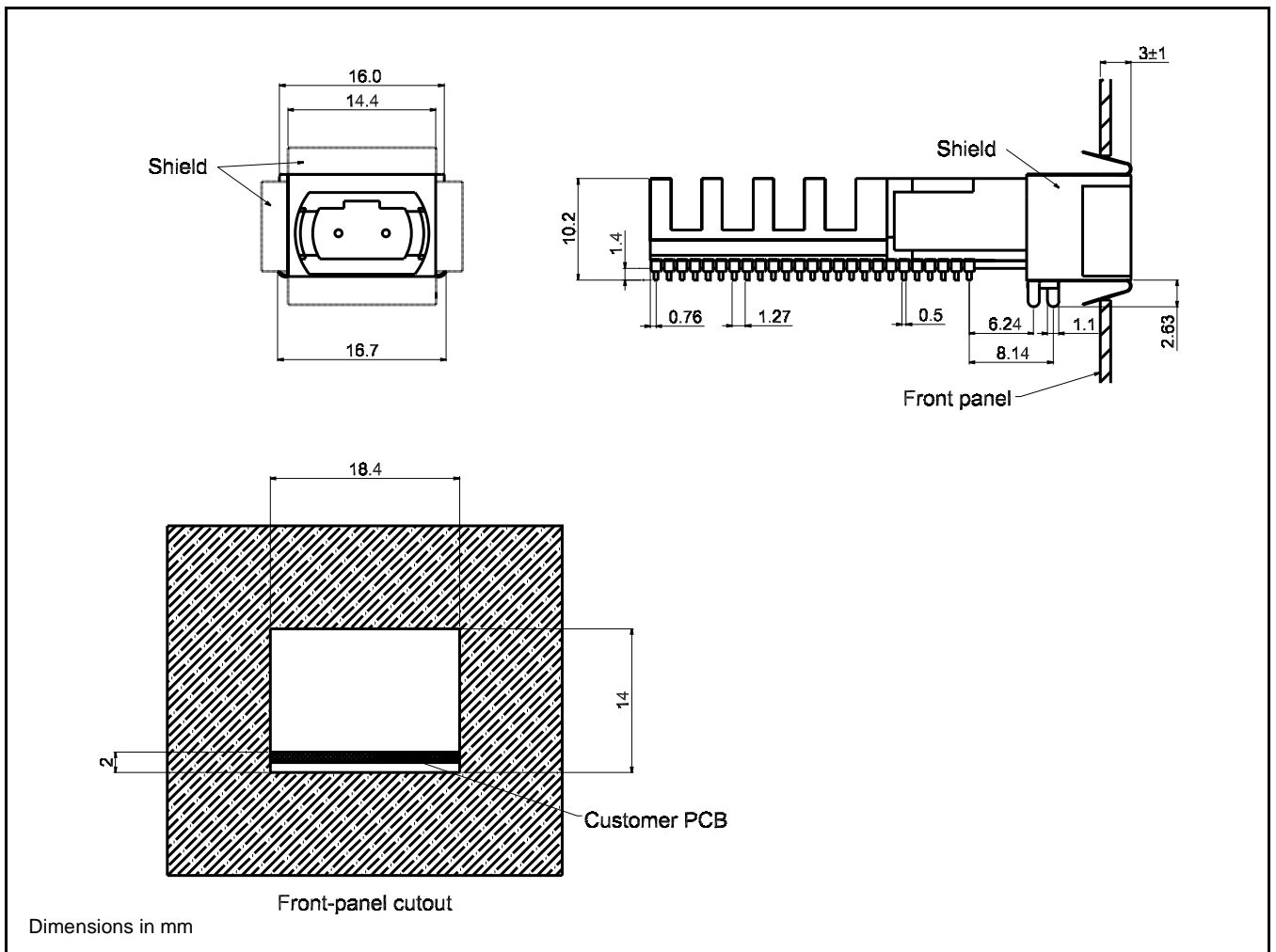


Figure 7 - MFT62340-JOS: MPO/MTP Connector Option With EMI Shield

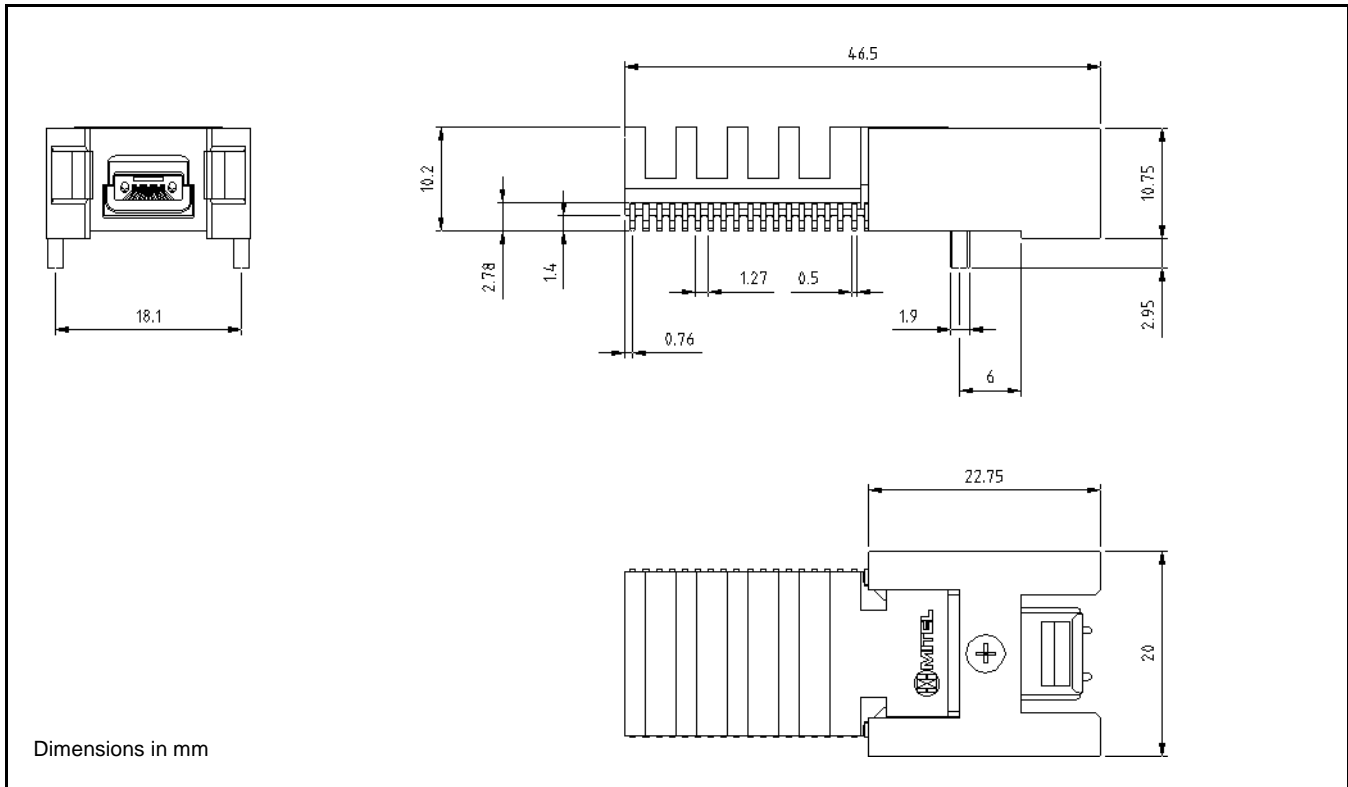


Figure 8 - MFT62340-JX: MPX Connector Option

PCB Footprints

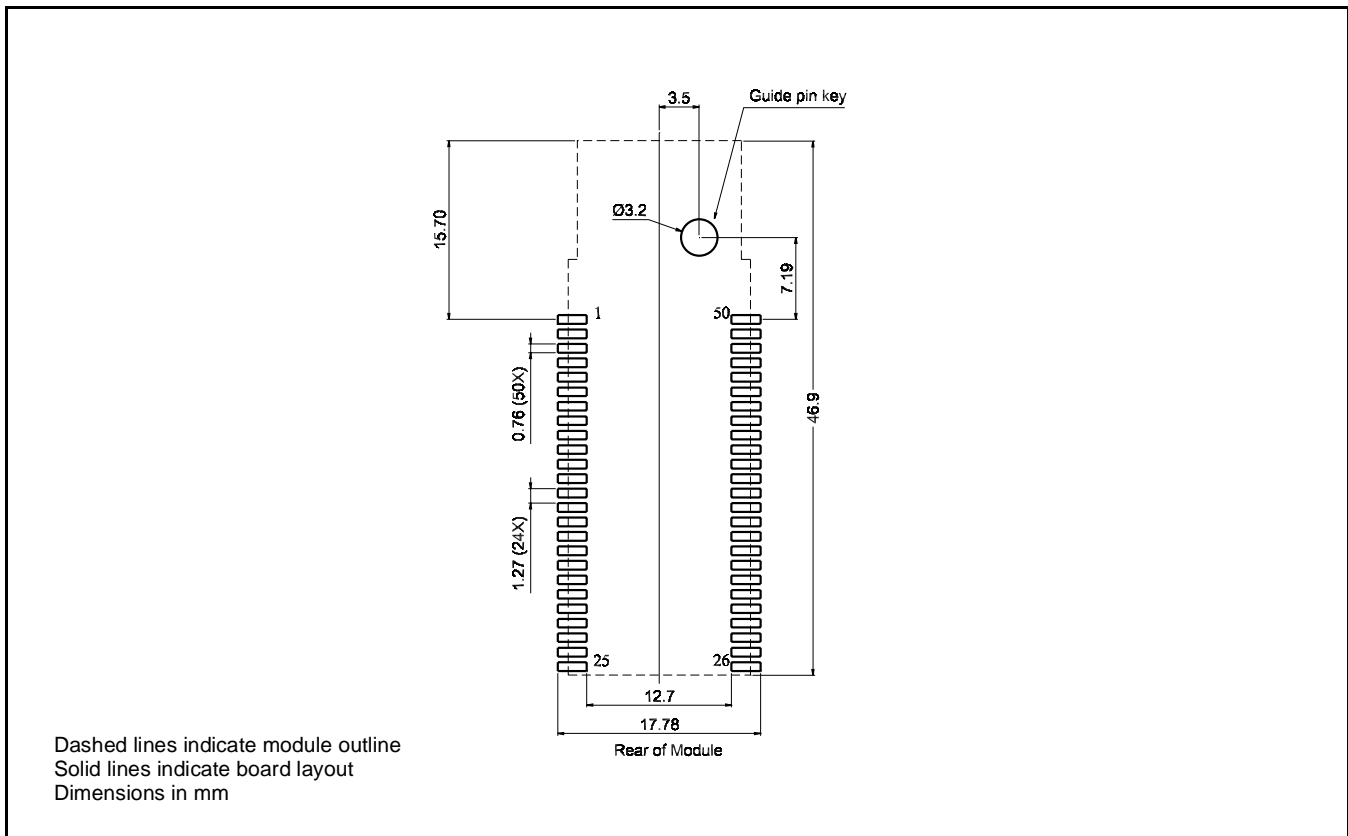


Figure 9 - MFT62340-JO: MPO/MTP Connector Option (Top View)

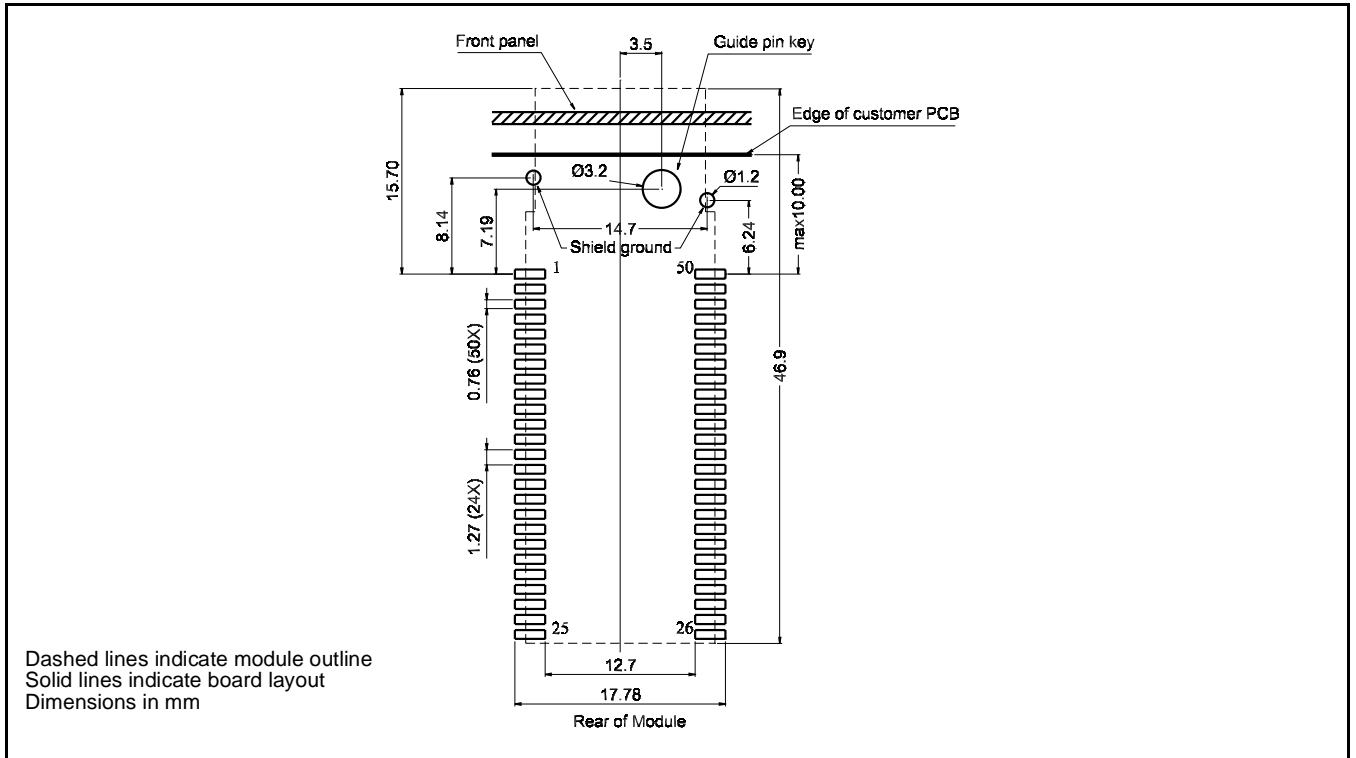


Figure 10 - MFT62340-JOS: MPO/MTP Connector Option With EMI Shield (Top View)

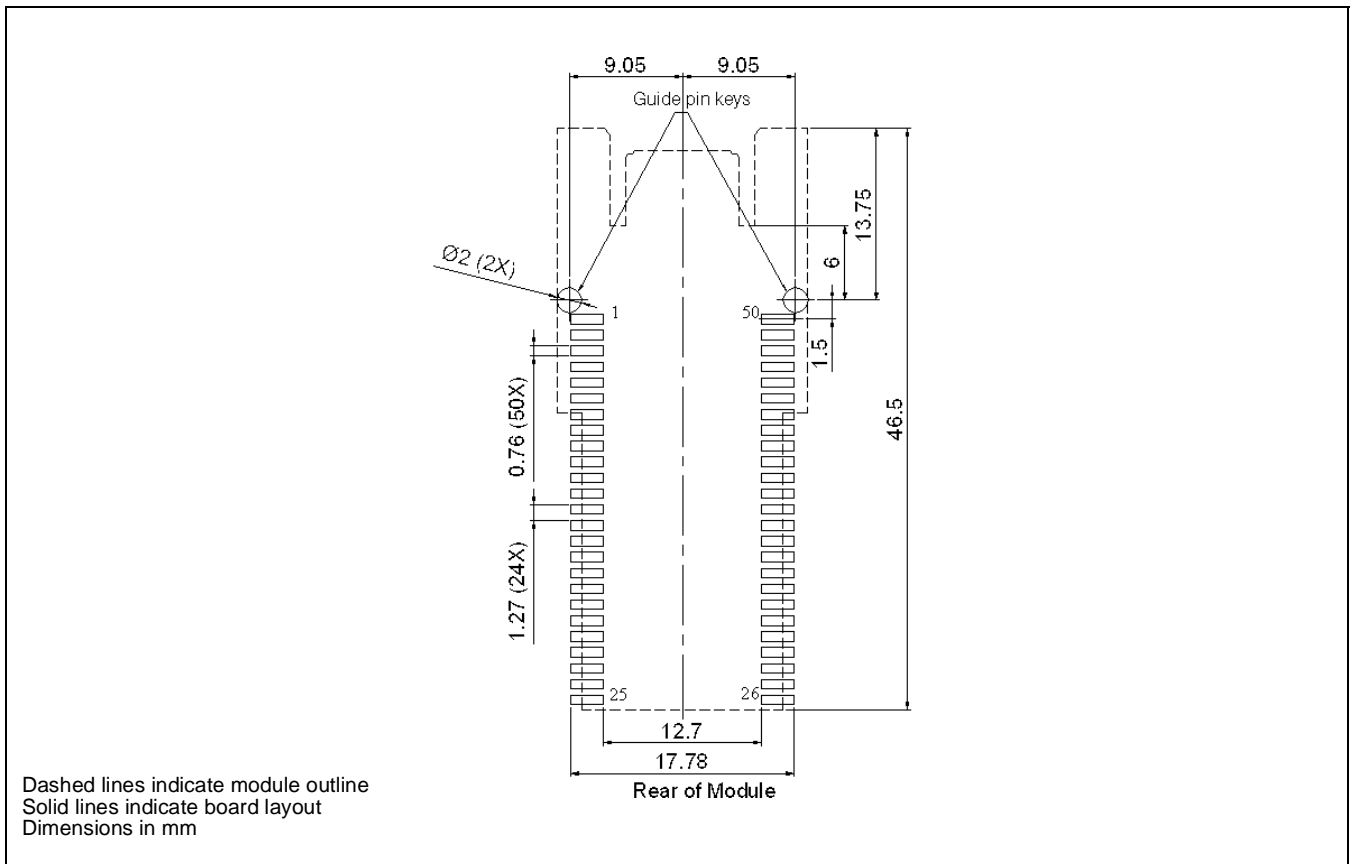


Figure 11 - MFT62340-JX: MPX Connector Option (Top View)

Electrical Connections

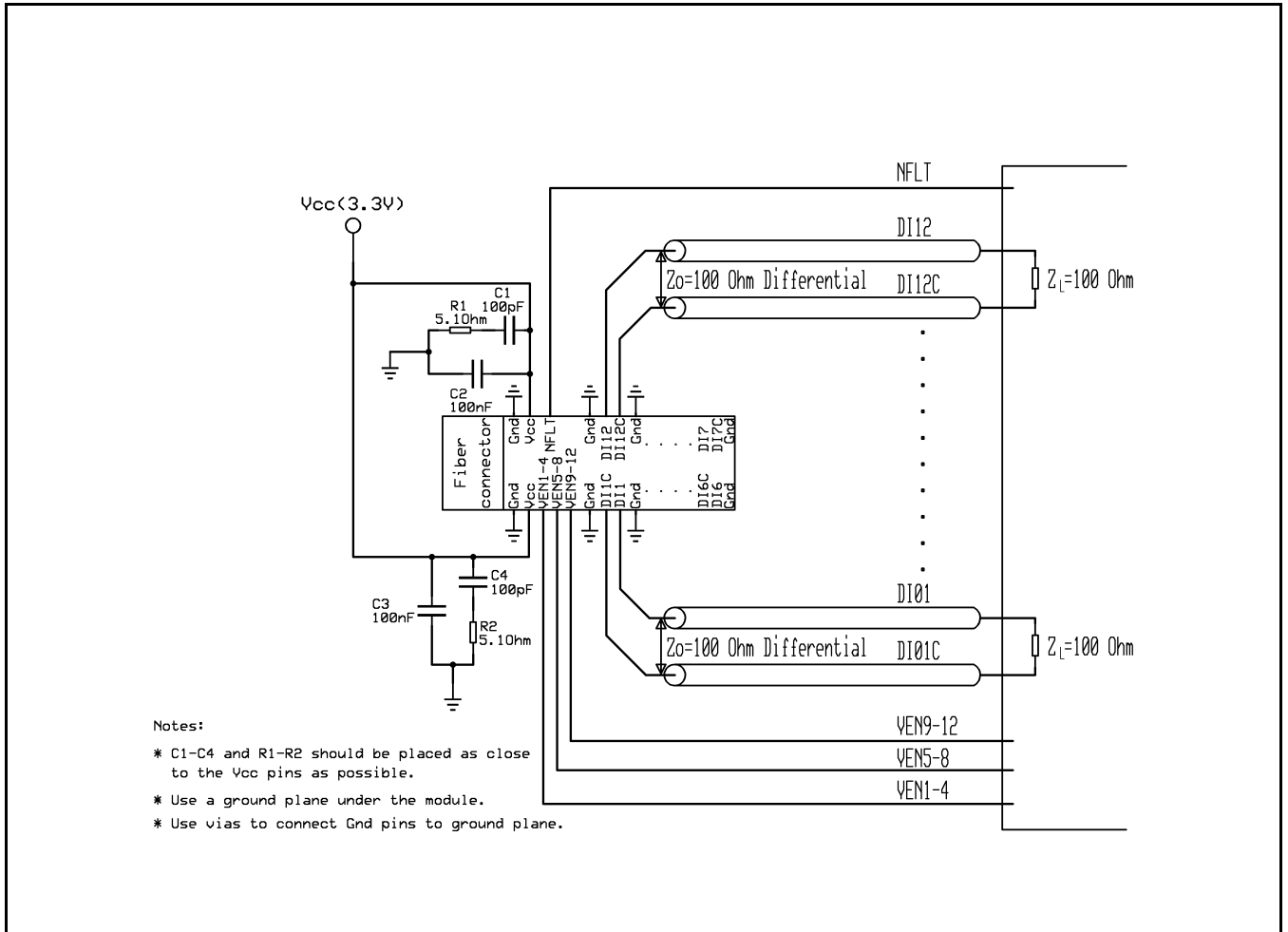


Figure 12 - Recommended Electrical Connections



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