

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
 μ PD16302

40 BIT ROW DRIVER FOR EL PANEL

DESCRIPTION

The μ PD16302 is a ROW driver utilized high voltage CMOS for EL Panel. It consists of a 40bit bidirectional shift register and high voltage CMOS drivers.

It operates at 5 V (CMOS input level) and provides low power dissipation because the driver is full CMOS construction, 250 V and 100 mA max.

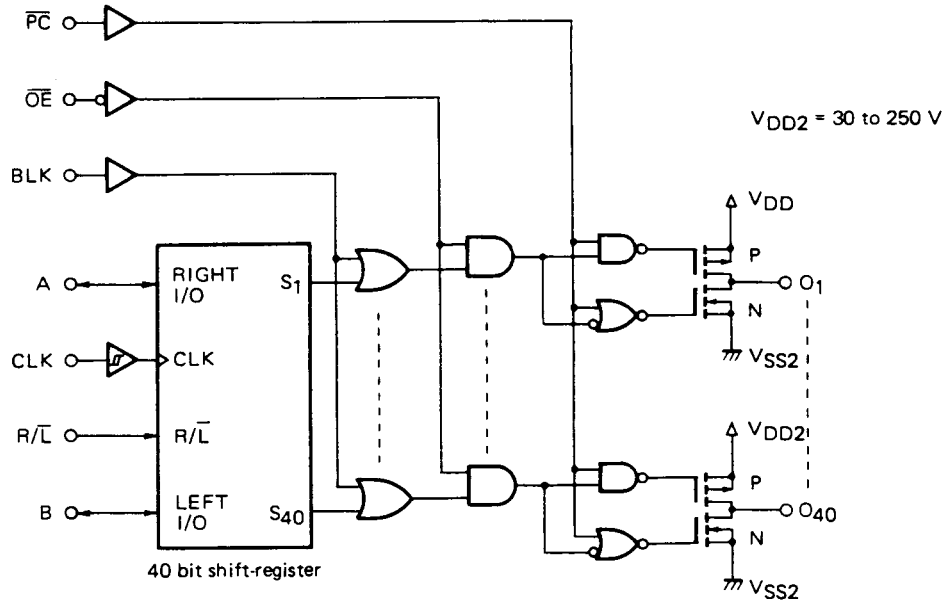
FEATURES

- High voltage CMOS construction
- High voltage Output (250 V, 100 mA max.)
- Built-in 40bit bidirectional shift register
- Capable of reversing a driver output polarity by PC terminal
- Low power dissipation (1 mA max., $T_a = -40$ to $+85$ °C)
- Symmetry pin configuration by tridirectional lead quad flat package

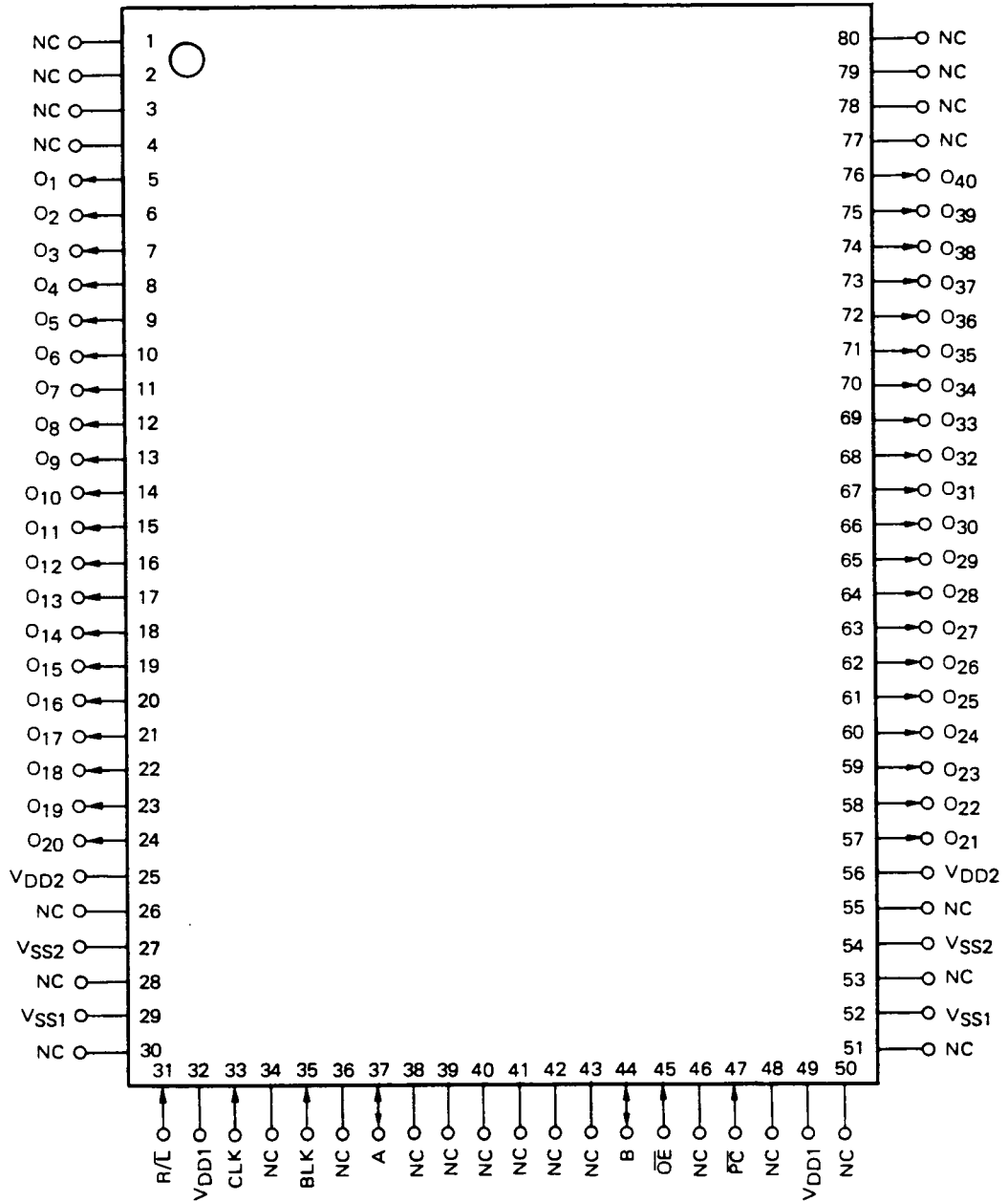
ORDERING INFORMATION

Part No.	Package
μ PD16302GF-3LA	100pin Plastic QFP (3 direction lead)

BLOCK DIAGRAM



PIN CONNECTION (Top View)



- Please open No. 40 pin to be connected with lead frame.
- The all power supply terminals (ex VDD1, VDD2, VSS1, and VSS2) should be used. VSS1 and VSS2 should be respectively connected with themselves outside.

PIN CONFIGURATION

SYMBOL	PIN NAME	PIN NO.	FUNCTION
BLK	Blank Input	35	Refer to below Table 2
\overline{OE}	Output Enable Input	45	Refer to below Table 2
\overline{PC}	Polarity Change Input	47	$\overline{PC} = L$: All driver output invert
A	Right Data I/O	37	R/ \overline{L} = H: A = IN, B = OUT R/ \overline{L} = L: B = IN, A = OUT
B	Left Data I/O	44	
CLK	Shift Clock Input	33	Positive edge active
R/ \overline{L}	Shift Direction Control Input	31	H: Right shift mode A → O ₁ to O ₄₀ → B L: Left shift mode B → O ₄₀ to O ₁ → A
O ₁ to O ₄₀	High Voltage Output	5-24, 57-76	250 V 100 mA max.
V _{DD1}	Logic Power Supply	32, 49	5 V ± 10 %
V _{DD2}	Driver Power Supply	25, 56	30 to 240 V
V _{SS1}	Ground (Logic)	29, 52	—
V _{SS2}	Ground (Driver)	27, 54	—
NC	No Connection	1-4, 26, 28, 30, 34, 36, 38-43, 46, 48, 50, 51, 53, 55, 77-80	No connection Please open No. 40 pin.

TRUTH TABLE 1 (Shift Register)

R/L	CLK	A	B	SHIFT REGISTER
H	↑	S ₁ input	S ₄₀ output	Data are shifted (to Right)
H	H or L			No change
L	↑	S ₁ output	S ₄₀ input	Data are shifted (to Left)
L	H or L			No change

TRUTH TABLE 2 (Driver)

DATA	BLK	\overline{OE}	PC	O _n	NOTE
X	H	L	H	H	All drivers = H
X	H	L	L	L	All drivers = L
X	X	H	X	Z	All drivers = Z
L	L	L	X	Z	
H	L	L	H	H	
H	L	L	L	L	

H = High level, L = Low level, X = H or L, Z = High Impedance, DATA = Contents of Shift Register

ABSOLUTE MAXIMUM RATINGS ($T_s = 25\text{ }^\circ\text{C}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Logic Power Supply	V_{DD1}	-0.5 to +7.0	V
Input Voltage	V_I	-0.5 to $V_{DD1} + 0.5$	V
Logic Output Voltage	V_{O1}	-0.5 to $V_{DD1} + 0.5$	V
Driver Power Supply	V_{DD2}	-0.5 to 250	V
Driver Output Voltage	V_{O2}	-0.5 to $V_{DD2} + 0.5$	V
Driver Output Current	I_{O2}	± 100	mA
Power Dissipation/Package	P_D	1000	mW
Operating Temperature	T_{opt}	-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($V_{SS1} = V_{SS2} = 0\text{ V}$)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT.
Logic Power Supply	V_{DD1}	4.5	5	5.5	V
High Level Input Voltage	V_{IH}	$0.7 V_{DD1}$		V_{DD1}	V
Low Level Input Voltage	V_{IL}	0		$0.2 V_{DD1}$	V
Driver Power Supply	V_{DD2}	80		250	V
Driver Output Current	I_{O2}			± 70	mA

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 250\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Output Voltage	V_{OH1}	$0.9 V_{DD1}$			V	Logic $I_{OH1} = 1\text{ mA}$
Low Level Output Voltage	V_{OL1}			$0.1 V_{DD1}$	V	Logic $I_{OL1} = 1\text{ mA}$
High Level Output Voltage	V_{OH21}	230	248		V	O1-40, $I_{OH2} = -10\text{ mA}$
	V_{OH22}	200	240		V	O1-40, $I_{OH2} = -70\text{ mA}$
Low Level Output Voltage	V_{OL21}		2	20	V	O1-40, $I_{OL2} = 10\text{ mA}$
	V_{OL22}		35	50	V	O1-40, $I_{OL2} = 70\text{ mA}$
3 State Output Current	I_{TL}			± 10	μA	$V_{O2} = V_{DD2}$ or V_{SS2}
3 State Input Current	I_I			± 1	μA	$V_I = V_{DD1}$ or V_{SS1}
High Level Input Voltage	V_{IH}	$0.7 V_{DD1}$			V	
Low Level Input Voltage	V_{IL}			$0.2 V_{DD1}$	V	
Stand by Current	I_{DD1}			100	μA	Logic
	I_{DD1}			1.0	mA	Logic: $T_a = -40$ to $+85^\circ\text{C}$
	I_{DD2}			100	μA	Driver
	I_{DD2}			1.0	mA	Driver: $T_a = -40$ to $+85^\circ\text{C}$

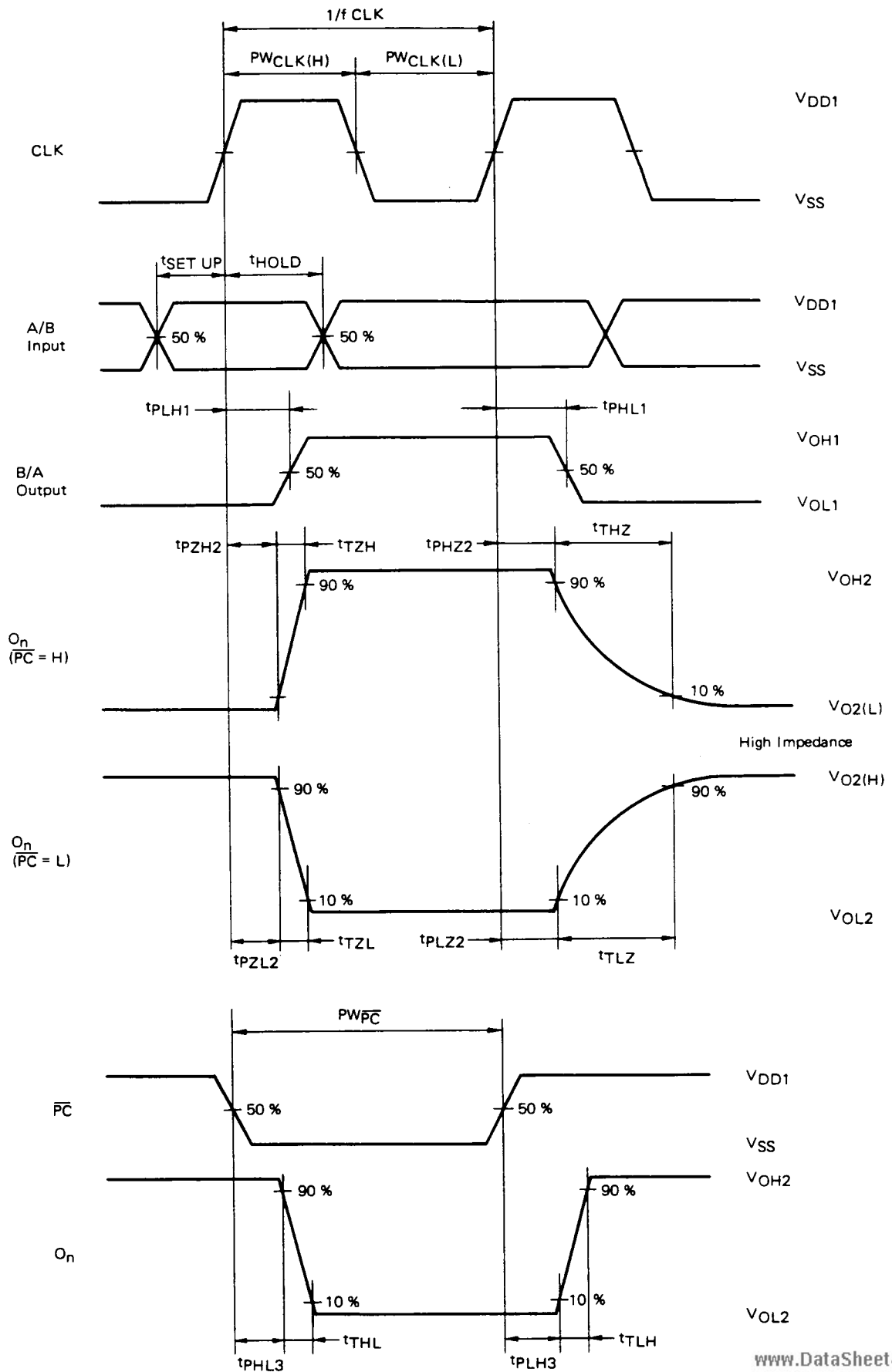
SWITCHING CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{DD1} = 5\text{V}$, $V_{DD2} = 250\text{V}$, $V_{SS} = 0\text{V}$,
 C_L (LOGIC) = 15 pF, C_L (DRIVER) = 330 pF, $R_L = 10\text{k}\Omega$)

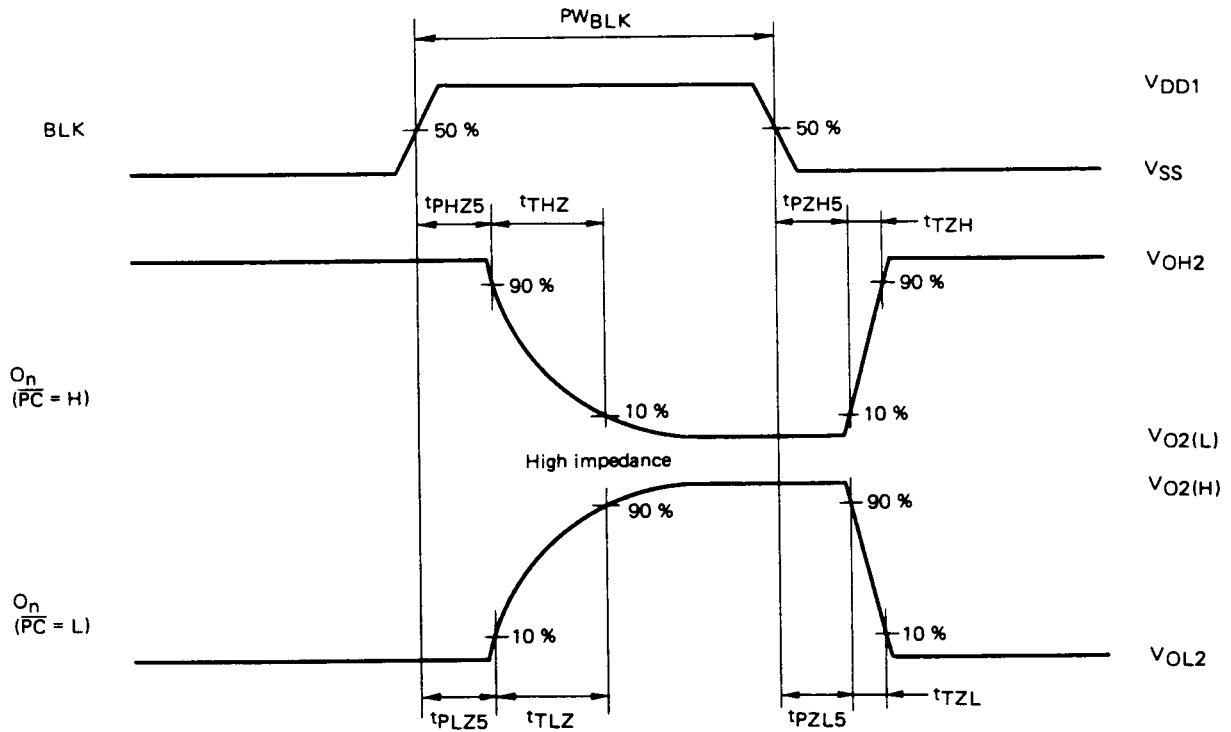
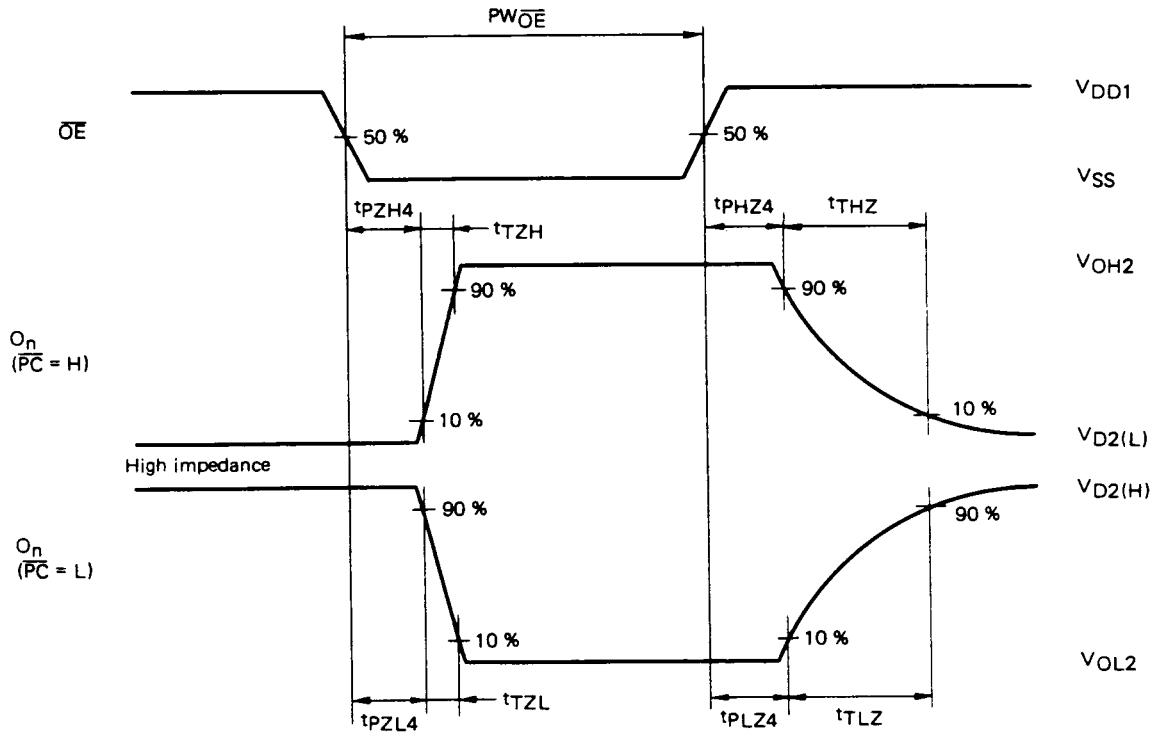
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Output Delay Time	t _{PHL1}		60	100	ns	CLK → A/B
	t _{PLH1}		60	100	ns	
	t _{PZH2}			500	ns	CLK → O ₁ to O ₄₀
	t _{PZL2}			500	ns	
	t _{PHZ2}			1	μs	
	t _{PLZ2}			1	μs	
	t _{PHL3}			1	μs	$\overline{\text{PC}}$ → O ₁ to O ₄₀
	t _{PLH3}			1	μs	
	t _{PZH4}			500	ns	$\overline{\text{OE}}$ → O ₁ to O ₄₀
	t _{PZL4}			500	ns	
	t _{PHZ4}			1	μs	
	t _{PLZ4}			1	μs	
	t _{PZH5}			500	ns	BLK → O ₁ to O ₄₀
	t _{PZL5}			500	ns	
	t _{PHZ5}			1	μs	
t _{PLZ5}			1	μs		
Output Rise Time	t _{TZH}			2	μs	O ₁ to O ₄₀
	t _{TLH}			2	μs	
	t _{TLZ}			15	μs	
Output Fall Time	t _{TZL}			2	μs	O ₁ to O ₄₀
	t _{THL}			2	μs	
	t _{THZ}			15	μs	
Maximum Clock Frequency	f _{max}	10	15		MHz	Duty = 50 %
Input Capacitance	C _I		10	15	pF	

AC TIMING REQUIREMENT ($T_a = -40$ to $+85^\circ\text{C}$, $V_{DD1} = 4.5\text{V}$ to 5.5V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Clock Pulse Width	PW _{CLK}	50			ns	
Blank Pulse Width	PW _{BLK}	3			μs	
$\overline{\text{PC}}$ Pulse Width	PW $\overline{\text{PC}}$	3			μs	
Enable Pulse Width	PW $\overline{\text{OE}}$	3			μs	
Data Setup Time	t _{SETUP}	50			ns	
Data Hold Time	t _{HOLD}	50			ns	

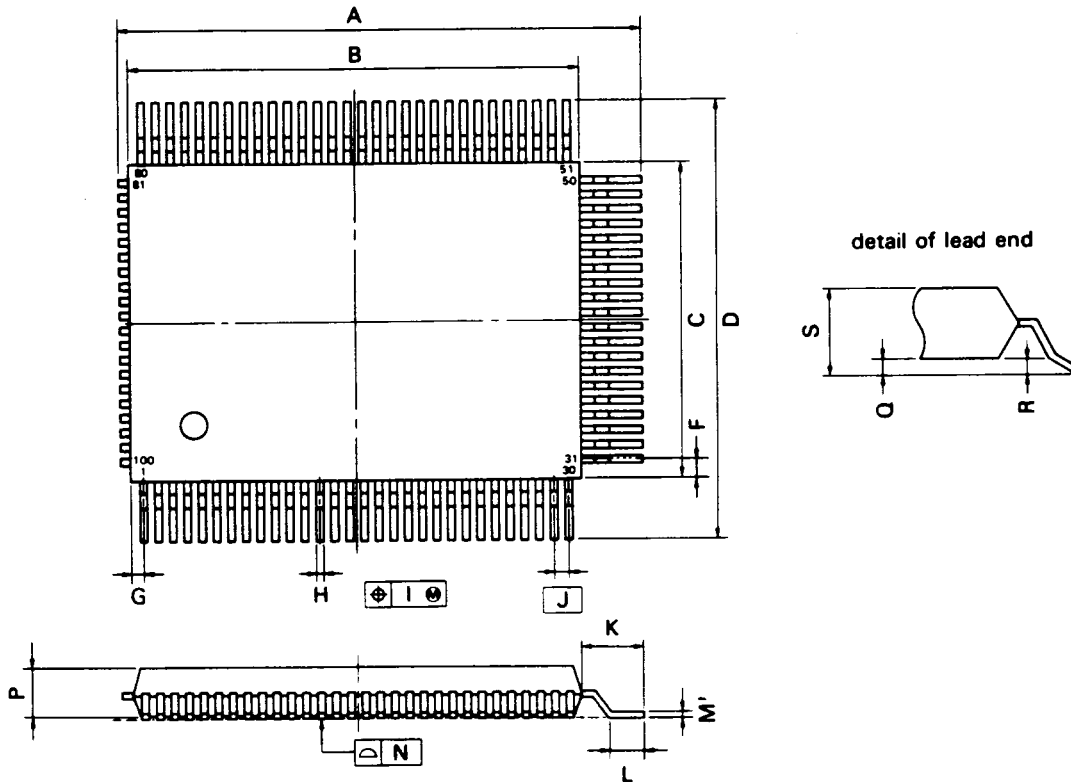
AC CHARACTERISTICS WAVEFORM





PACKAGE DIMENSION

100 pin plastic QFP (3 directions leads)



P100GF-65-3LA

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.3 ^{±0.4}	0.878 ^{±0.016}
B	20.0 ^{±0.2}	0.795 ^{±0.008}
C	14.0 ^{±0.2}	0.551 ^{±0.008}
D	17.6 ^{±0.4}	0.693 ^{±0.016}
F	0.8	0.031
G	0.6	0.024
H	0.30 ^{±0.10}	0.012 ^{±0.004}
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8 ^{±0.2}	0.071 ^{±0.008}
L	0.8 ^{±0.2}	0.031 ^{±0.008}
M	0.15 ^{±0.08}	0.006 ^{±0.003}
N	0.15	0.006
P	2.7	0.106
Q	0.1 ^{±0.1}	0.004 ^{±0.004}
R	0.1 ^{±0.1}	0.004 ^{±0.004}
S	3.0 MAX.	0.119 MAX.